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Ragh Kuttappa

Summary

I am a PhD student focusing on low power VLSI, with a strong background in nano-scale circuits and systems, device physics and low power design methodologies.

Education

2015-present **PhD Student**, *Drexel University, Philadelphia*, PA, GPA-**3.8/4**.

2013-2015 **Master Degree**, *San Francisco State University, San Francisco*, CA, GPA-**3.8/4**.

2008-2012 **Bachelor of Engineering**, *Visvesvaraya Technological University (VTU)*, Karnataka, India.

Experience

Sept 2015 - present **Research Assistant, Drexel VLSI and Architecture Laboratory**, *Drexel University*.

- **Advisor**: Dr. Baris Taskin, Associate Professor, Electrical and Computer Engineering
- Design of transistor level and gate level low power circuits using cadence suite.
- Implementation of Verilog-A models for emerging optoelectronic components for CMOS integration.
- Exploring energy efficient circuits using near threshold voltage (NTV) and threshold logic.

Aug 2013 - Aug 2015 **Research Assistant, NECRL**, *San Francisco State University*.

- **Advisor**: Dr. Hamid Mahmoodi, Associate Professor, Computer Engineering
- Reliability Analysis of Spin Transfer Torque (STT) based circuits.
- Low power design methodologies for reconfigurable logic using Look Up Tables (LUT).
- Thesis: Circuit Reliability Analysis under Variations in Nano-Scale CMOS.

Publications

- Ragh Kuttappa, Houman Homayoun, Hassan Salmani and Hamid Mahmoodi, "Comparative Analysis of Robustness of Spin Transfer Torque based Look Up Tables under Process Variations," (to appear) *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016.
- Ragh Kuttappa, Houman Homayoun, Hassan Salmani and Hamid Mahmoodi, "Reliability Analysis of Spin Transfer Torque based Look up Tables under Process Variations and NBTI Aging," *Elsevier Microelectronics Reliability Journal*, September 2015.

Graduate Level Coursework

Custom VLSI Design I/II, Advanced VLSI Design, Digital VLSI Design, Nano-Scale Circuits and Systems, Advanced Microprocessor Architecture, Parallel Computer Architecture.

Selected Projects

Sept 2014 **VLSI Design**, *Design of 64x32 bit SRAM memory block*.

- Design of full custom 64x32 bit SRAM schematic and layout.
- Optimizing the design for speed, area, stability, dynamic and static power consumption.
- Optimized the circuit by smart controller logic design resulting in 1.8GHz clock frequency and 23% area reduction.

Feb 2014 **Nano-scale Circuits and Systems**, *Spin Transfer Torque (STT) based Look up Tables (LUT) in Nano-scale CMOS*.

- Lookup table with 16nm CMOS technology using linear resistor model and characterized LUT in terms of standby power, read delay and power delay product (PDP).
- The highlights included implementing various power reduction techniques like Dual Vt and reducing gate level voltage.

Sept 2013 **Digital Design**, *Design of full search motion estimator used in Low power H.264 Video Compression Architectures*.

- The aim of this project is to find motion vectors between two successive motion frames by motion estimation.
- Bottom-up design approach is followed and each module is tested before top level integration with memory modules resulting in stable efficient design.
- Verilog RTL design, simulation, synthesis and timing analysis.

Technical Skills

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- **EDA Tools** Cadence Virtuoso, Synopsys Custom Designer,Synopsys Design Compiler, Synopsys ICC, Cadence Encounter, Synopsys PrimeTime
- **Languages** C, C++, Perl,Matlab, LaTeX