Vinayak Honkote

Ph.D. Candidate
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Research Interests

Resonant Clocking, Electronic Design Automation (EDA) of VLSI Circuits, Statistical Timing, Low power VLSI Circuits, Physical Design in general including Clock Network Design, High Frequency Circuit Design, Adiabatic Circuits, Large-Scale Optimization including LP and ILP, Emerging Technologies including Quantum-Dot Cellular Automata (QCA) and Post-CMOS Interconnects.

Education

- **Ph.D, Electrical Engineering**, (09/2006 – current, expected 2010).
  Drexel University, Philadelphia, PA.
  Topic: High Performance Circuit Design Using Resonant Rotary Clocking Technology
  GPA: 3.8/4.0
- **M.S., Electrical Engineering**, (09/2004 – 06/2006).
  Drexel University, Philadelphia, PA.
  GPA: 3.5/4.0
- **B.E., Electronics and Communications Engineering**, (09/1999 – 06/2003).
  Bangalore Institute of Technology,
  Visvesvaraya Technological University, Bangalore, India.
  GPA: 3.9/4.0

Professional Experience

- **Teaching Fellow**, (06/2009 – current)
  ECE C304 Design with Micro-controllers, undergraduate level,
  Richard C. Goodwin College of Professional Studies, Drexel University, Philadelphia, PA
- **Teaching Fellow**, (06/2008 – 09/2008)
  ECE C394 Computer Structures, undergraduate level,
  Richard C. Goodwin College of Professional Studies, Drexel University, Philadelphia, PA
- **Research Assistant**, (08/2006 – current)
  High Performance Circuit Design Using Resonant Rotary Clocking Technology
  Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
- **Teaching Assistant**, (03/2005 – current)
  ECE C302 Digital Systems Projects, undergraduate level,
  ECE C304 Design with Micro-controllers, undergraduate level,
  ECE 200 Fundamentals of Intelligent Systems, undergraduate level,
  ECE C301 Advanced Programming for Engineers, undergraduate level,
  ECE C356 Embedded Systems, undergraduate level,
  Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
- **Internship - Junior Project Manager**, (06/2005 – 12/2005)
  Siemens Medical Solutions, Malvern, PA, USA
- **Full-time Engineer**, (07/2003 – 08/2004)
  Larsen & Toubro Infotech Ltd., Bangalore, India

PUBLICATIONS

Journal Publications

3 Vinayak Honkote and Baris Taskin, *Skew Analysis and Design Methodologies for Improved Performance of Resonant Clocking Technologies* , IEEE Transactions on Very Large Scale Integration (VLSI) Systems (to submit).

2 Vinayak Honkote and Baris Taskin, *Capacitive Load Balancing on Rotary Oscillatory Array*, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD) (submitted).

1 Vinayak Honkote and Baris Taskin, *CROA: Design and Analysis of the Custom Rotary Oscillatory Array*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems (submitted).

Conference Publications

10 Vinayak Honkote and Baris Taskin, *Skew Analysis and Methodologies for Improved Performance of Resonant Clocking Technologies*, IEEE International SoC Design Conference (ISOCC), November 2009 (invited to special session).

9 Vinayak Honkote and Baris Taskin, *Design and Analysis of Custom Rotary Oscillatory Array*, IEEE International Symposium on Circuits and Systems (ISCAS),May/June 2010 (in review).

8 Vinayak Honkote and Baris Taskin, *Optimal and Practical Capacitive Load Balancing for Zero Clock Skew Rotary Oscillatory Array*, IEEE Design Automation and Test in Europe (DATE),March 2010 (in review).

7 Vinayak Honkote and Baris Taskin, *Skew Analysis and Methodologies for Improved Rotary Clocking Performance*, IEEE Asia and South Pacific Design Automation Conference (ASPDAC), January 2010 (in review).

6 Vinayak Honkote and Baris Taskin, *Analysis, Design and Simulation of Capacitive Load Balanced Rotary Oscillatory Array*, 23^{rd} International Conference on VLSI Design, January 2010 (in review).

5 Vinayak Honkote and Baris Taskin, *Capacitive Load Balancing for Mobius Implementation of Standing Wave Oscillator*, Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS), August 2009.

4 Vinayak Honkote and Baris Taskin, *Design Automation Scheme for Wirelength Analysis of Resonant Clocking Technologies*, Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS), August 2009.

3 Vinayak Honkote and Baris Taskin, *Zero Clock Skew Synchronization with Rotary Clocking Technology*, Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED), March 2009, pp. 588–593.

2 Vinayak Honkote and Baris Taskin, *Custom Rotary Clock Router*, Proceedings of the IEEE International Conference on Computer Design (ICCD), October 2008, pp. 114–119.

1 Vinayak Honkote and Baris Taskin, *Maze Router Based Scheme for Rotary Clock Router*, Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS), August 2008, pp. 442–445.

ACADEMIC HONORS AND AWARDS

- ◇ Selected to participate in ACM/SIGDA Ph.D. forum at DAC 2009.
- ◇ Participated in ACM/SIGDA CADathlon programming contest at ICCAD 2008.
- ◇ Recipient of "Richard A. Newton Graduate Scholarship" at ACM/IEEE Design Automation Conference (DAC) 2007, for the *Routing for Resonant Clocking Technology in Multi-GHz range* project.
- ◇ Awarded a fellowship to attend the Design Automation Summer School (DASS) held at DAC 2007, San Diego, CA, on June 23, 2007
- ◇ Awarded a travel grant to *NANOARCH 2006* held in Boston, MA, on June 17, 2006.
- ◇ Awarded the Dean Fellowship for graduate study at Drexel University (September 2004 onwards).
- ◇ Secured 14th rank in 10th grade out of 600000 students, Karnataka, India in 1997.

RELEVANT COURSEWORK
- VLSI Design, Computer Architecture, Microprocessors and Embedded controllers, VHDL, CAD for VLSI Design, Deep SubMicron IC Design, Digital IC and CMOS Technology, Stochastic Systems, DSP.

RELATED SKILLS
- C, C++, Perl, VHDL, Spice, Cadence, Synopsys, Matlab, Xilinx, Modelsim, Labview.