Vinayak Honkote

Ph.D. Candidate Department of Electrical and Computer Engineering Drexel University, Bossone 324, 3141 Chestnut Street Philadelphia, PA 19104-2875 Phone: 215-421-9149 Fax: 215-895-1695 E-mail: vh32@drexel.edu Url: http://vlsi.ece.drexel.edu

Research Interests	VLSI Physical Design in general including Clock Network Design, Resonant Clocking, Electronic Design Automation (EDA) of VLSI Circuits, Digital Integrated Circuits, Low Power VLSI Circuits, Emerging Technologies, 3-D ICs, NanoCMOS, High Frequency Circuit Design and Post-CMOS Interconnects.
EDUCATION <	 Ph.D., Electrical and Computer Engineering, (09/2006 – current, expected 2010). Drexel University, Philadelphia, PA. Topic: High Performance Circuit Design Using Resonant Rotary Clocking Technology Advisor: Dr. Baris Taskin
<	M.S., Electrical Engineering, (09/2004 – 06/2006). Drexel University, Philadelphia, PA.
<	 B.E., Electronics and Communications Engineering, (09/1999 – 06/2003). Bangalore Institute of Technology, Visvesvaraya Technological University, Bangalore, India.
PROFESSIONAL < Experience	 Research Assistant, (09/2006 – current) VLSI Laboratory Department of Electrical and Computer Engineering Drexel University, Philadelphia, PA
<	 Internship - Junior Project Manager, (06/2005 – 12/2005) Siemens Medical Solutions, Malvern, PA, USA
<	Full-time Engineer, (07/2003 – 08/2004) Larsen & Toubro Infotech Ltd., Bangalore, India
TEACHING < Experience	 Freshman Design Fellow, (09/2009 – current) Co-teaching (with a faculty instructor) the engineering design laboratory sequence, Drexel University, Philadelphia, PA
<	 Adjunct Primary Instructor, (Summer 2009) ECE C304 Design with Micro-controllers, undergraduate level, Richard C. Goodwin College of Professional Studies, Drexel University, Philadelphia, PA
<	 Adjunct Primary Instructor, (Summer 2008) ECE C394 Computer Structures, undergraduate level, Richard C. Goodwin College of Professional Studies, Drexel University, Philadelphia, PA
<	 Teaching Assistant, (03/2005 – current) ECE C302 Digital Systems Projects, undergraduate level, ECE C304 Design with Micro-controllers, undergraduate level, ECE 200 Fundamentals of Intelligent Systems, undergraduate level, ECE C301 Advanced Programming for Engineers, undergraduate level, ECE C356 Embedded Systems, undergraduate level, Department of Electrical and Computer Engineering Drexel University, Philadelphia, PA

PUBLICATIONS Refereed Journal Publications and Submissions

- 4 Vinayak Honkote and Baris Taskin, *Power Analysis on Custom Rotary Oscillatory Array*, IEEE Transactions on Very Large Scale Integration (TVLSI) Systems (in preparation).
- 3 Vinayak Honkote and Baris Taskin, *Design of Zero Clock Skew Rotary Oscillatory Array with Load Balancing*, ACM Transactions on Design Automation of Electronic Systems (TODAES) (in preparation).
- 2 Vinayak Honkote and Baris Taskin, Simultaneous Skew Control and Capacitive Load Balancing on Rotary Oscillatory Array, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD) (submitted).
- 1 Vinayak Honkote and Baris Taskin, *CROA: Design and Analysis of the Custom Rotary Oscillatory Array*, IEEE Transactions on Very Large Scale Integration (TVLSI) Systems (in review, March 2010).

Refereed Conference Publications

- 8 Vinayak Honkote and Baris Taskin, Skew Analysis and Bounded Skew Constraint Methodology for Rotary Clocking Technology, to appear in IEEE International Symposium on Quality Electronic Design (ISQED), March 2010.
- 7 Vinayak Honkote and Baris Taskin, *Analysis, Design and Simulation of Load Balancing*, Proceedings of the IEEE International Conference on VLSI Design (VLSID), January 2010, pp. 218–223.
- 6 Vinayak Honkote and Baris Taskin, Skew Analysis and Design Methodologies for Improved Performance of Resonant Clocking, Proceedings of the IEEE International SoC Design Conference (ISOCC), November 2009, pp. 165–168 (invited to special session).
- 5 Vinayak Honkote and Baris Taskin, Capacitive Load Balancing for Mobius Implementation of Standing Wave Oscillator, Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS), August 2009, pp. 232–235.
- 4 Vinayak Honkote and Baris Taskin, Design Automation Scheme for Wirelength Analysis of Resonant Clocking Technologies, Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS), August 2009, pp. 1147–1150.
- 3 Vinayak Honkote and Baris Taskin, Zero Clock Skew Synchronization with Rotary Clocking Technology, Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED), March 2009, pp. 588–593.
- 2 Vinayak Honkote and Baris Taskin, *Custom Rotary Clock Router*, Proceedings of the IEEE International Conference on Computer Design (ICCD), October 2008, pp. 114–119.
- Vinayak Honkote and Baris Taskin, *Maze Router Based Scheme for Rotary Clock Router*, Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS), August 2008, pp. 442– 445.

Academic <	Awarded one of the nine (9) Freshman Design Fellowships (2009-10) by the College of Engineering,
HONORS AND	covering full tuition and stipend, including career development for academic/research positions.
Awards <	Awarded the fellowship to attend VLSID 2010 held in Bangalore, India between 4-7 Jan, 2010.

- ◊ Participated in ACM/SIGDA Ph.D. forum at DAC 2009.
- ◊ Participated in ACM/SIGDA CADathlon programming contest at ICCAD 2009, 2008.
- ◊ Recipient of "Richard A. Newton Graduate Scholarship" at ACM/IEEE Design Automation Conference (DAC) 2007, for the *Routing for Resonant Clocking Technology in Multi-GHz range* project.
- Awarded a fellowship to attend the Design Automation Summer School (DASS) held at DAC 2007.
- ♦ Awarded a travel grant to attend NANOARCH 2006 held in Boston, MA, on June 17, 2006.
- ♦ Awarded the Dean Fellowship for graduate study at Drexel University (September 2004 onwards).
- ♦ Secured 14th rank in 10th grade out of 600,000 students, Karnataka, India in 1997.

- SKILLS & C, C++, Perl, Unix Shell Scripting, Basic Java
 - Cadence Virtuoso Suite, Spectre Mentor – HDL Designer, Modelsim, Leonardo Spectrum Synopsys – Design Compiler, HSPICE Xilinx – Spartan 3, Virtex 5
 - ◊ VHDL, SystemC, Matlab, Maple, Labview
 - ◊ Cplex, Glpk, Lp Solve
 - ◊ LATEX, XEmacs, vi, Office Suites
 - ◊ Unix, Linux, Mac OS, MS Windows, DOS

RELEVANT VLSI Design, Computer Architecture, Microprocessors and Embedded controllers, VHDL, CAD for VLSICOURSEWORKDesign, Deep SubMicron IC Design, Algorithms and Datastructures, Digital IC and CMOS Technology,
Stochastic Systems, DSP.