$\approx$
$_{m}esh_{v}2.pdf[ProposedMulti-VoltageDomainClockMeshTopology.][width=0.95]mesh_{p}ic_{v}3.pdfClockMeshTopologie$

$\alpha f V_{dd} c_{total}$

$c_{mesh} c_{stub} c_{pmt}$
αf

$t_{skew}^{pmt} t_{skew}^{mesh} t_{skew}^{stub} t_{skew}^{mesh} t_{skew}^{stub} t_{skew}^{pmt}$
$_{e}xamp.pdfSimple2-levelClockTreewith16Sinks$
SAED90nm EDK librarySynopsysIC CompilerSynopsysCustomSim XASynopsys

$\approx\approx$*on purpose*
$slew_{const}$
$slew_{const} slew_{max}^{i} slew_{max}^{i} < slew_{const} slew_{max}^{i}$
$slew_{const} slew_{max} > slew_{const} + slew_{margin} N \times NNN$*max insertion delay is in the same domain for all casesmax insert*
$\times$
SAED 90nm EDK Library
Design CompilerSynopsysIC CompilerSynopsysCustomSim XASynopsys
V_{dd}
V_{dd}
V_{dd}
IC Compiler$slew_{const} \times$
$\approx\approx$
$_{c}ompare.pdfSkewComparisonvs.TypicalSkewBudgets$

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