SNACKNOC: PROCESSING IN THE COMMUNICATION LAYER

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Feb 25th 2020

VLSI and Architecture Lab

Opportunistic Resources for Graduate Students

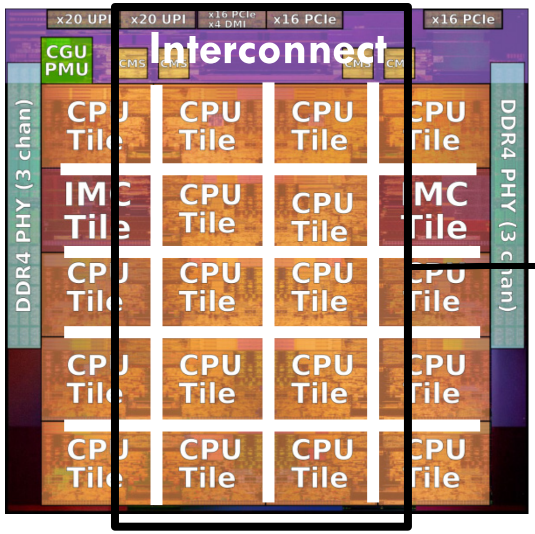
Free leftovers

toward

Steak dinner

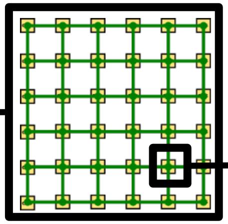
Opportunistically collecting snacks towards a meal.

Opportunistic Resources in the CMP

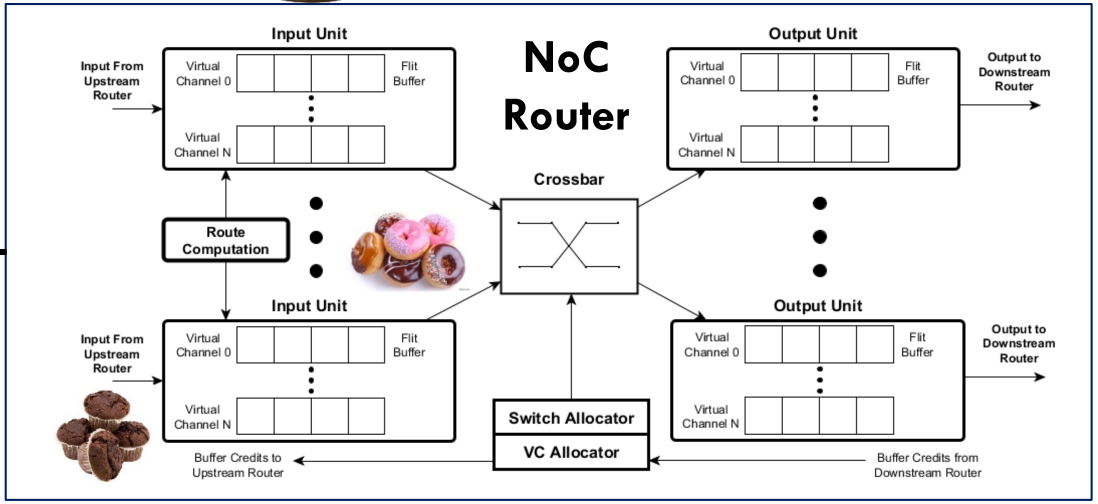


Intel Skylake 8180 HCC [1]

Communication Interconnect



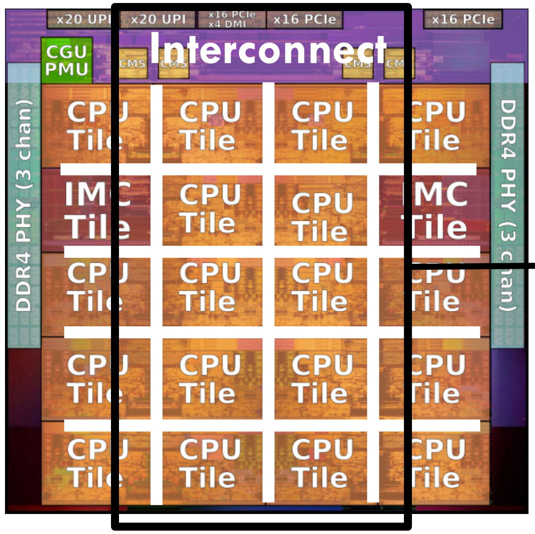
"Free leftovers"



Opportunistically collecting "snacks" to make a "meal".

[1] Intel Skylake SP HCC, Wikichip.

Opportunistic Resources in the CMP



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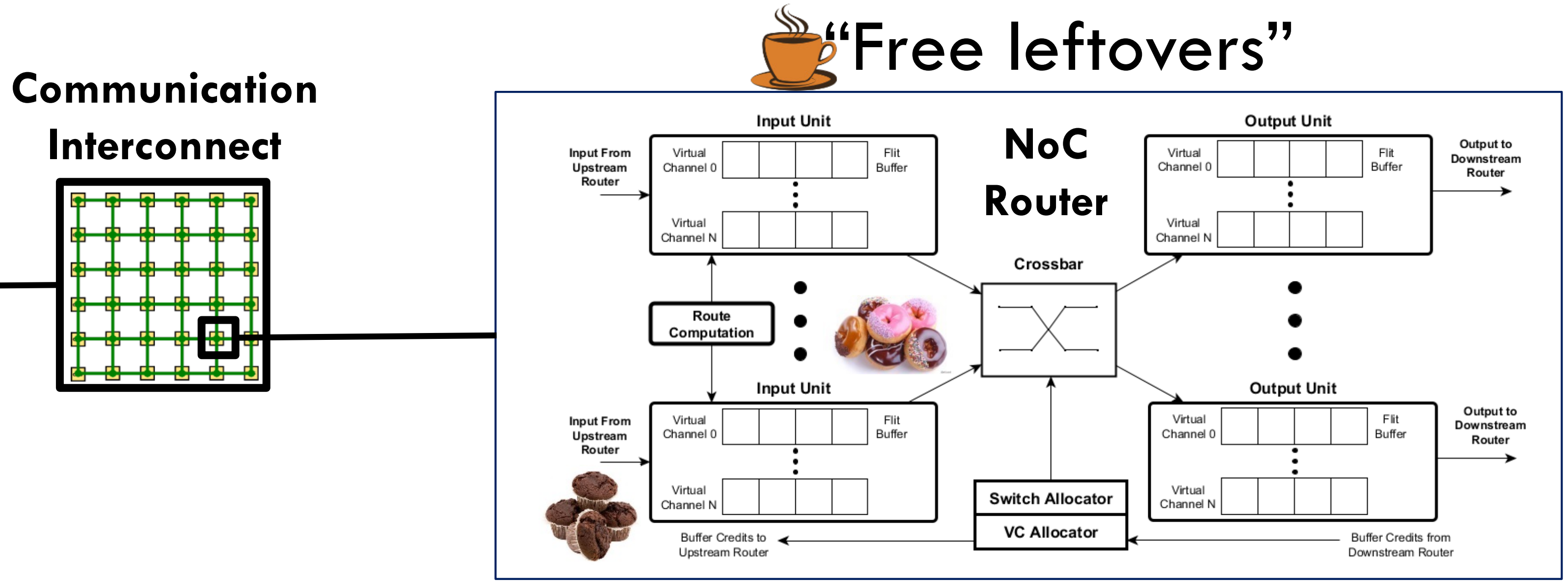

What is the performance gain we add by opportunistically "snacking" on CMP resources?

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Quantifying Design Slack in the NoC

- NoC designed to minimize latency during **heavy** traffic
  - NoC implementation can account for 60% to 75% of the miss latency[2]

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  - 3 selected best paper nominated NoCs have similar performance:
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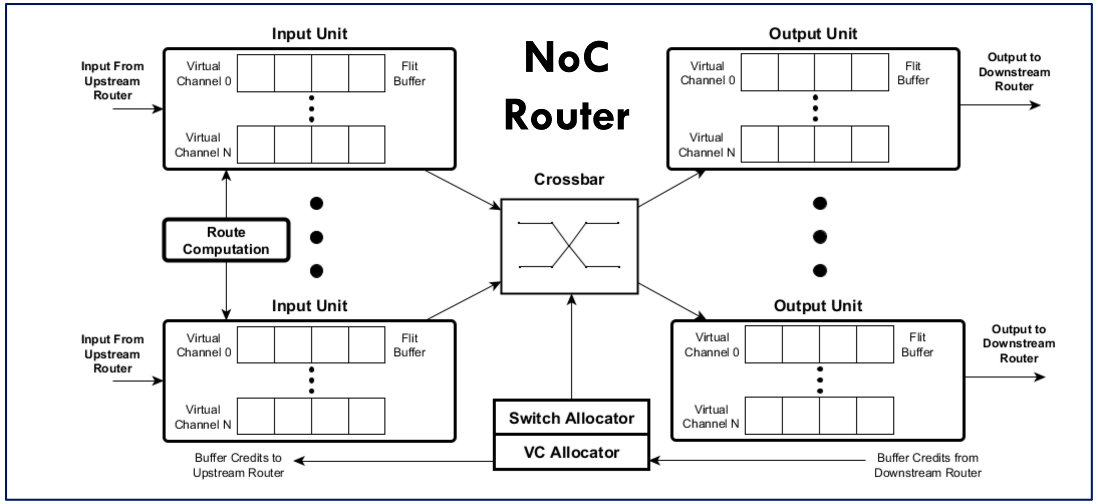
- Opportunities in Network-on-Chip Slack



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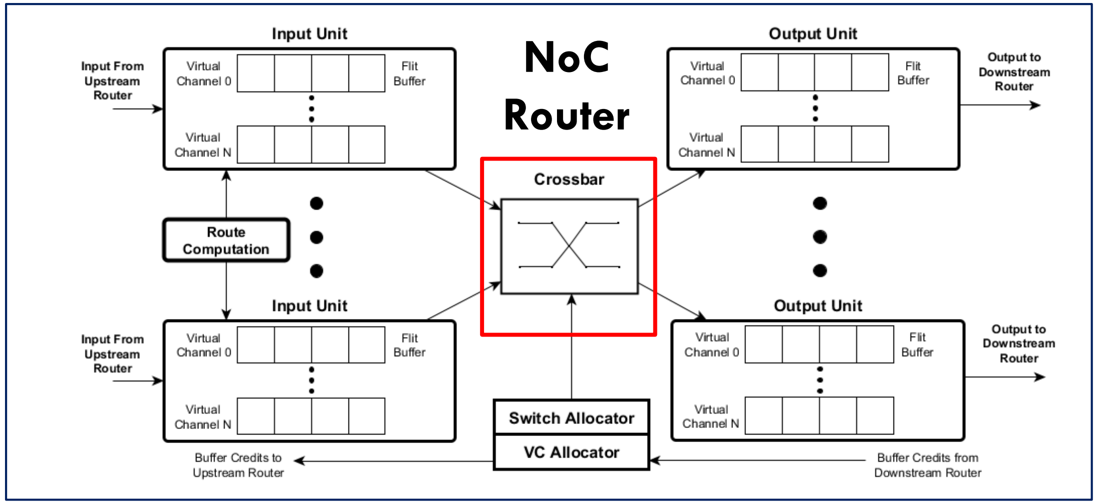
  - Crossbar



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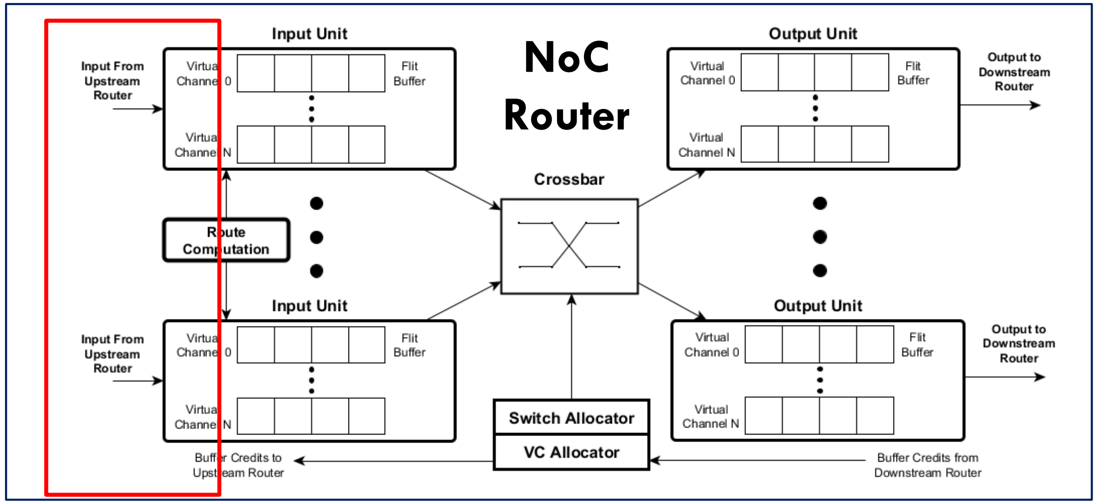

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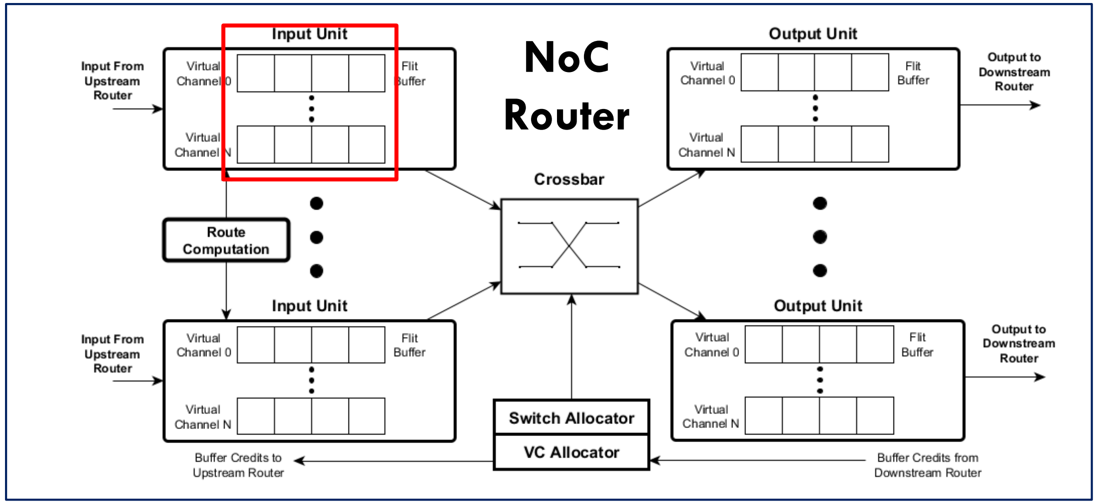
  - Internal Buffers



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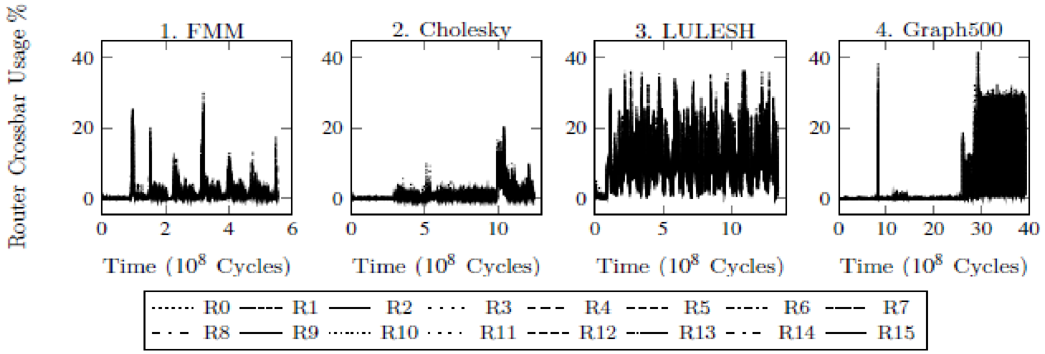
Quantifying Design Slack in the NoC

Crossbar Utilization



- Simulated 16 core CMP with 4 benchmarks representing "low", "medium", "medium-high", "high" traffic
- Crossbar Utilization:
  - Peak utilization (Graph 500): 42% utilization
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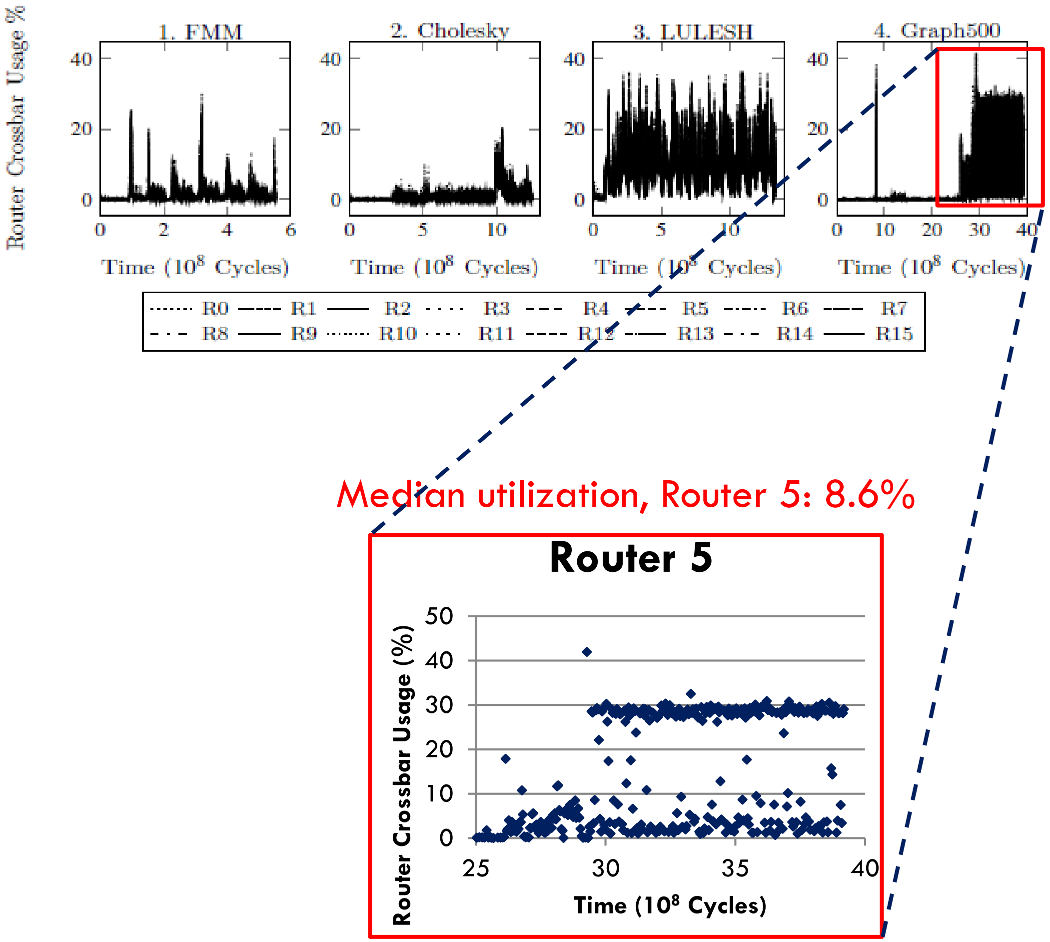

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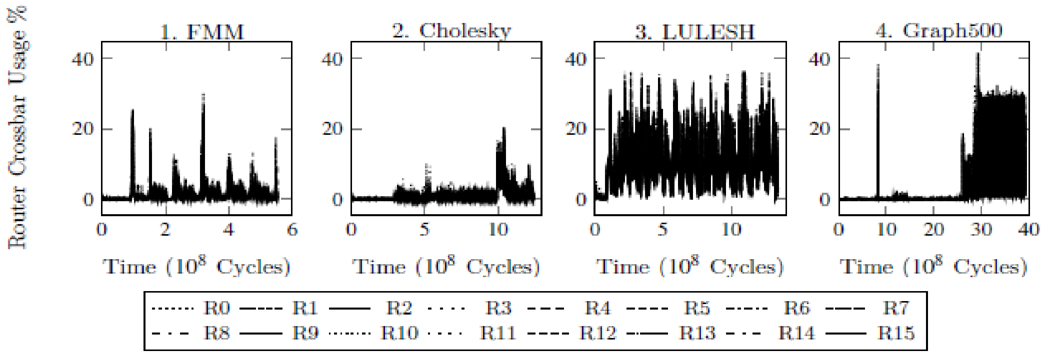

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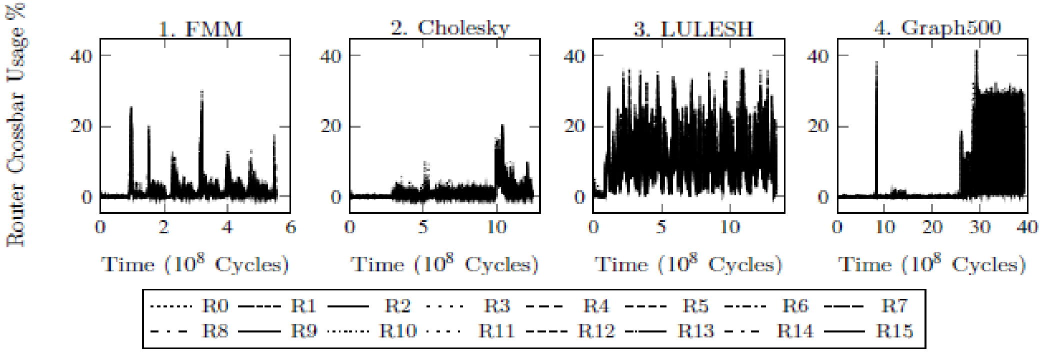
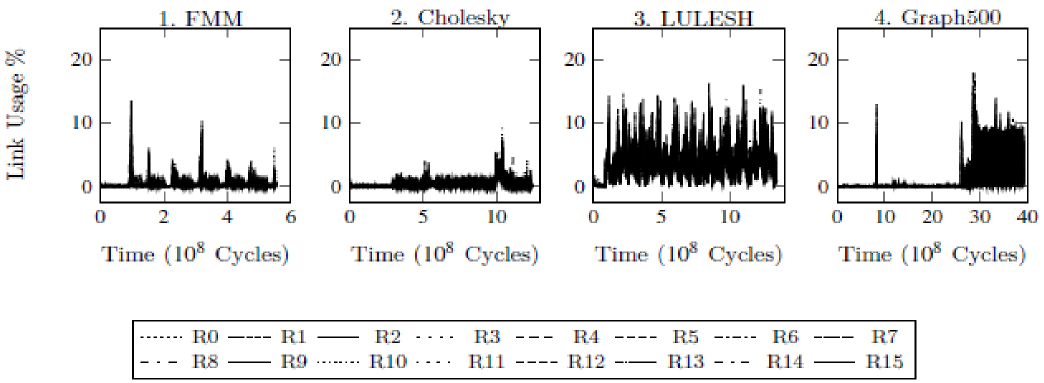


Link Utilization



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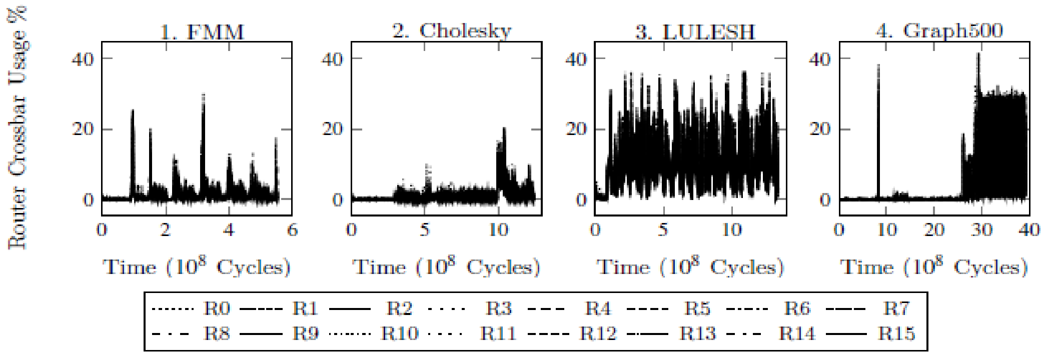

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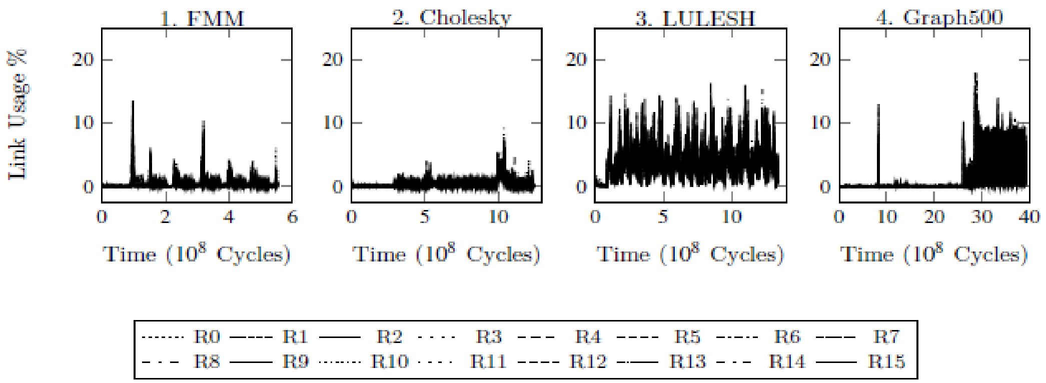

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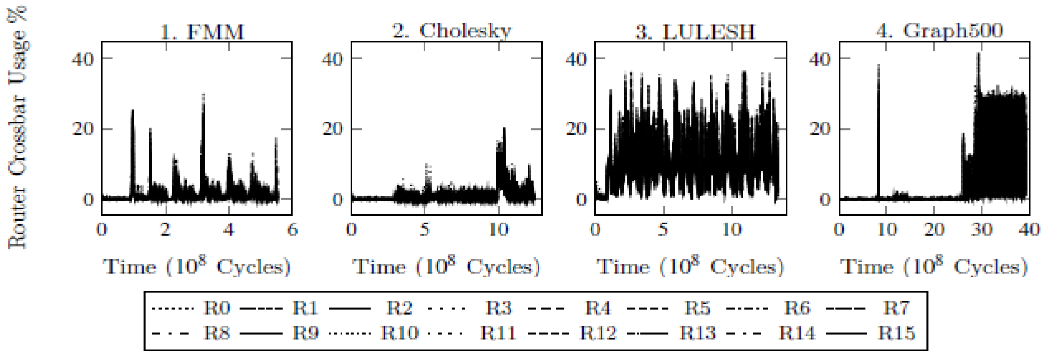
- Buffer Utilization
  - Raytrace : 4% of cycles have localized contention
  - 10% utilization during contention
  - 3M flits of the 2.4T flits forwarded: buffer utilization reaches 30-55% of the total capacity

Quantifying Design Slack in the NoC

Crossbar Utilization



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The SnackNoC platform improves **efficiency** and **performance** of the CMP by offloading data-parallel workloads and “snacking” on network resources.

Overview

- “Slack” of the Communication Fabric
- **The SnackNoC Platform**
- Experimental Results
- Conclusion and Future Considerations

SnackNoC Platform Overview

- Goals:
  - Opportunistically “Snack” on existing network resources for additional performance
  - Limited additional overhead to uncore
  - Minimal or zero interference to CMP traffic

- Opportunistic NoC-based compute platform
  - Limited dataflow engine
  - Applications:
    - Data-parallel workloads used in scientific computing, graph analytics, and machine learning

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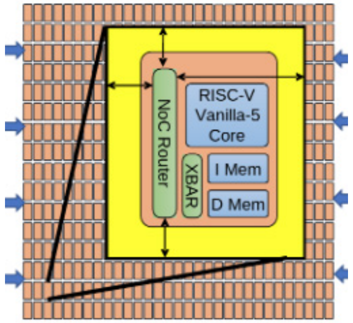

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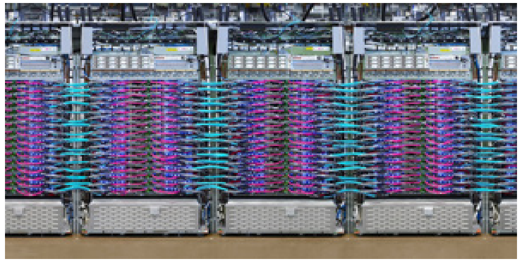

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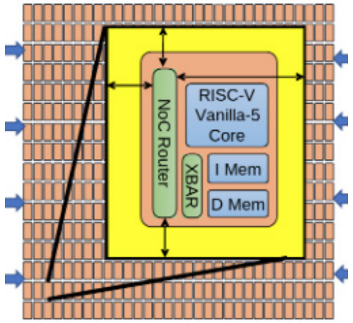

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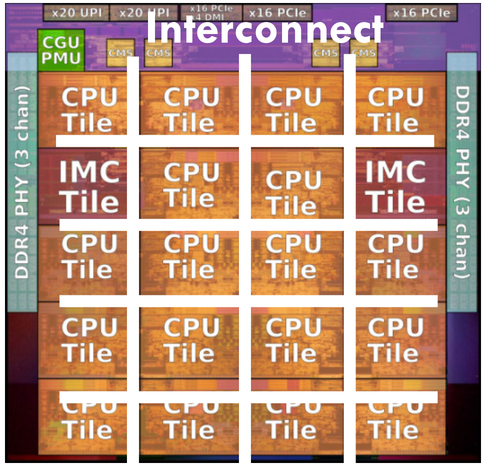

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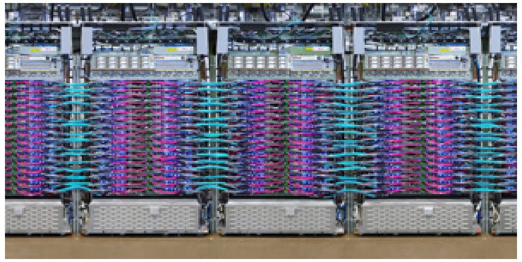

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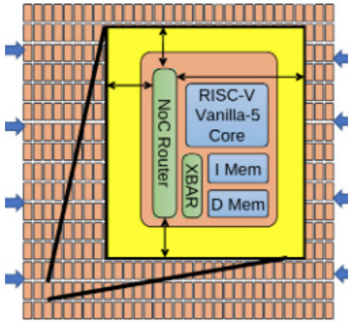

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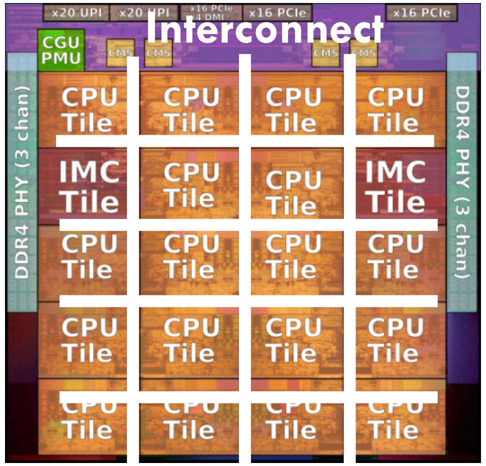

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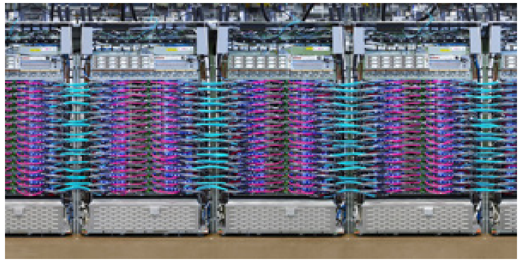

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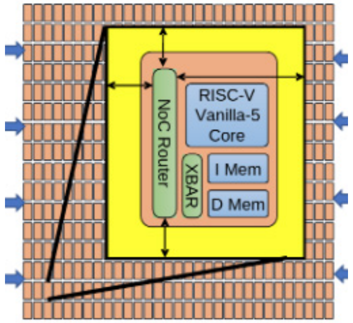

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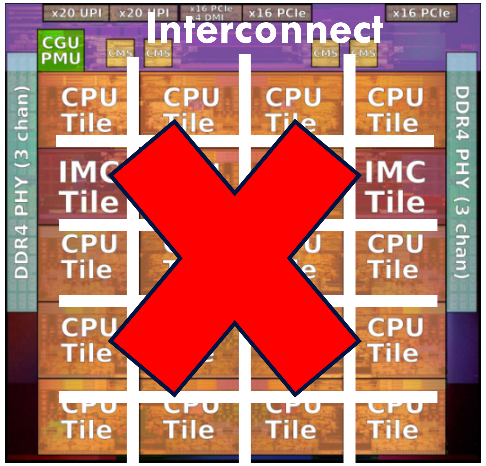

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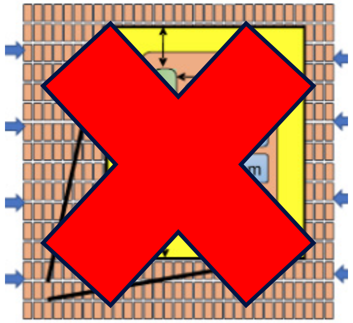

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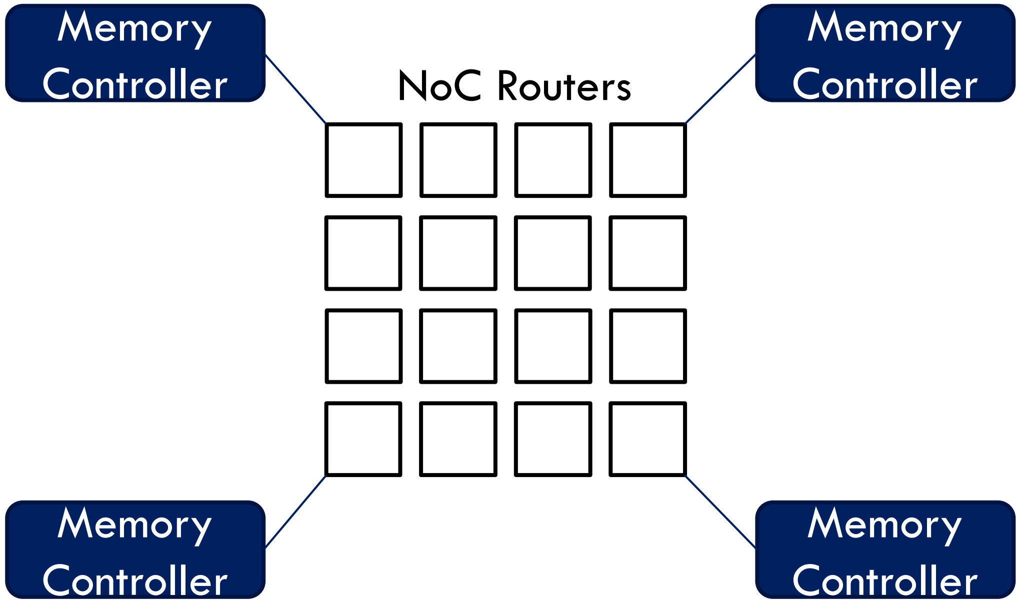

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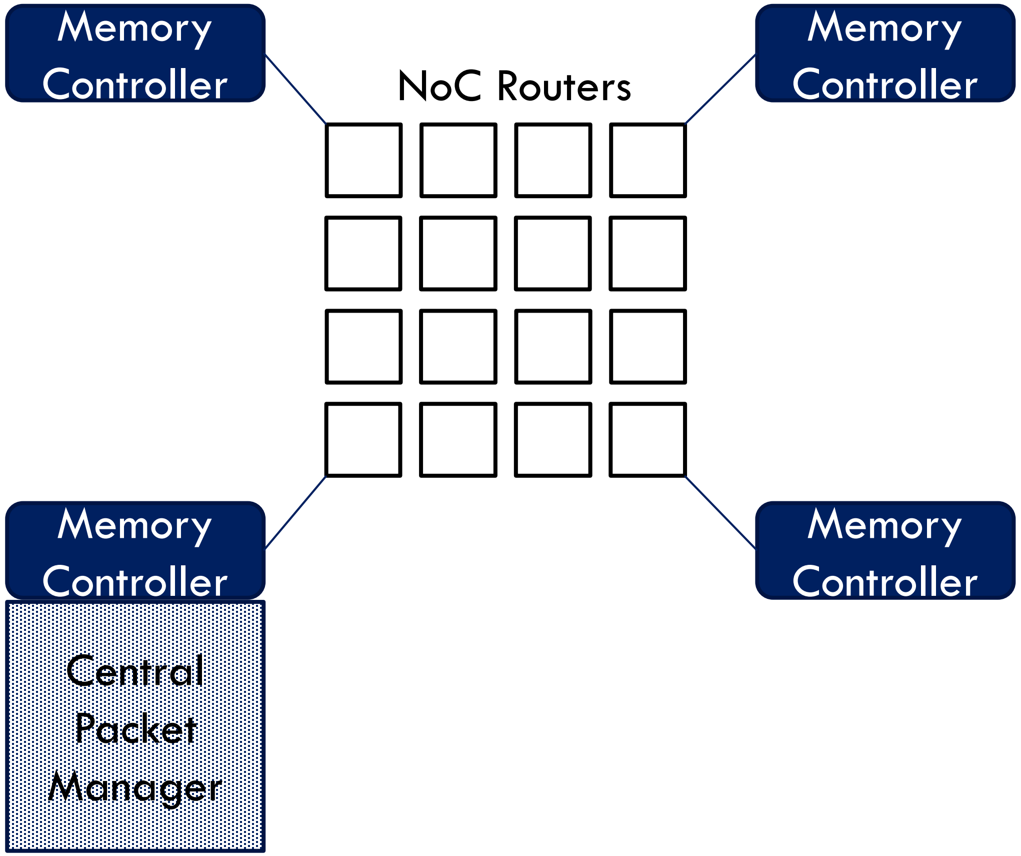

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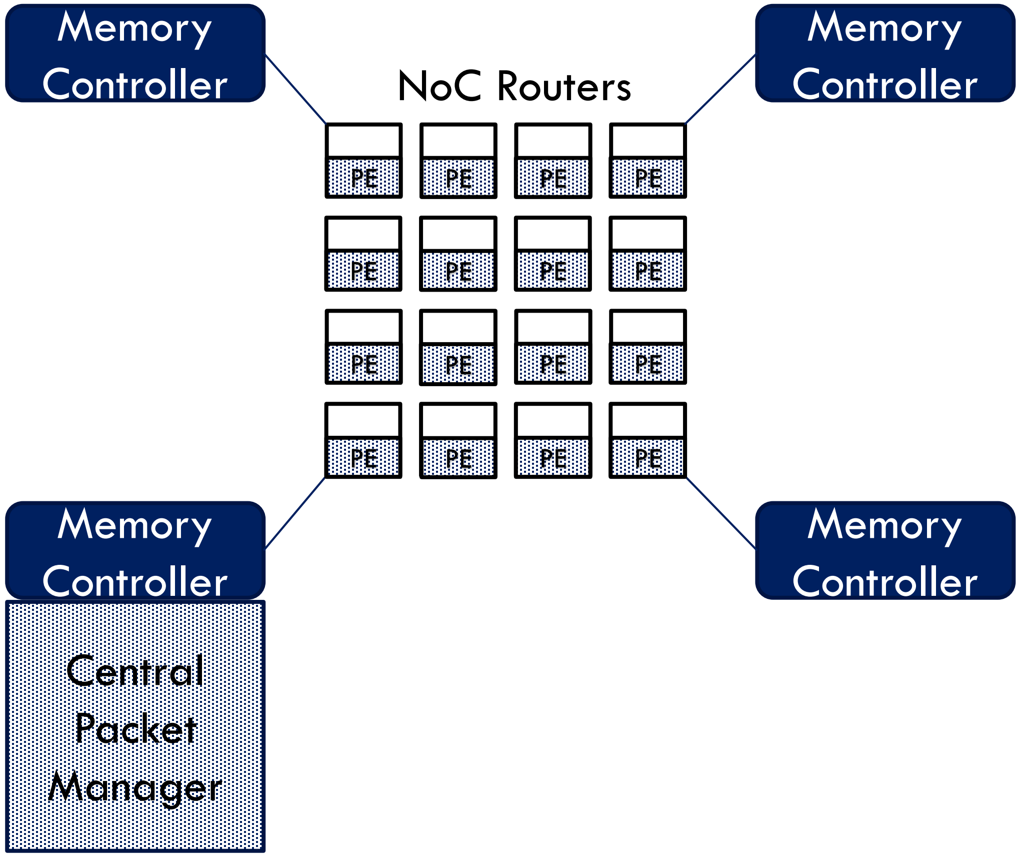

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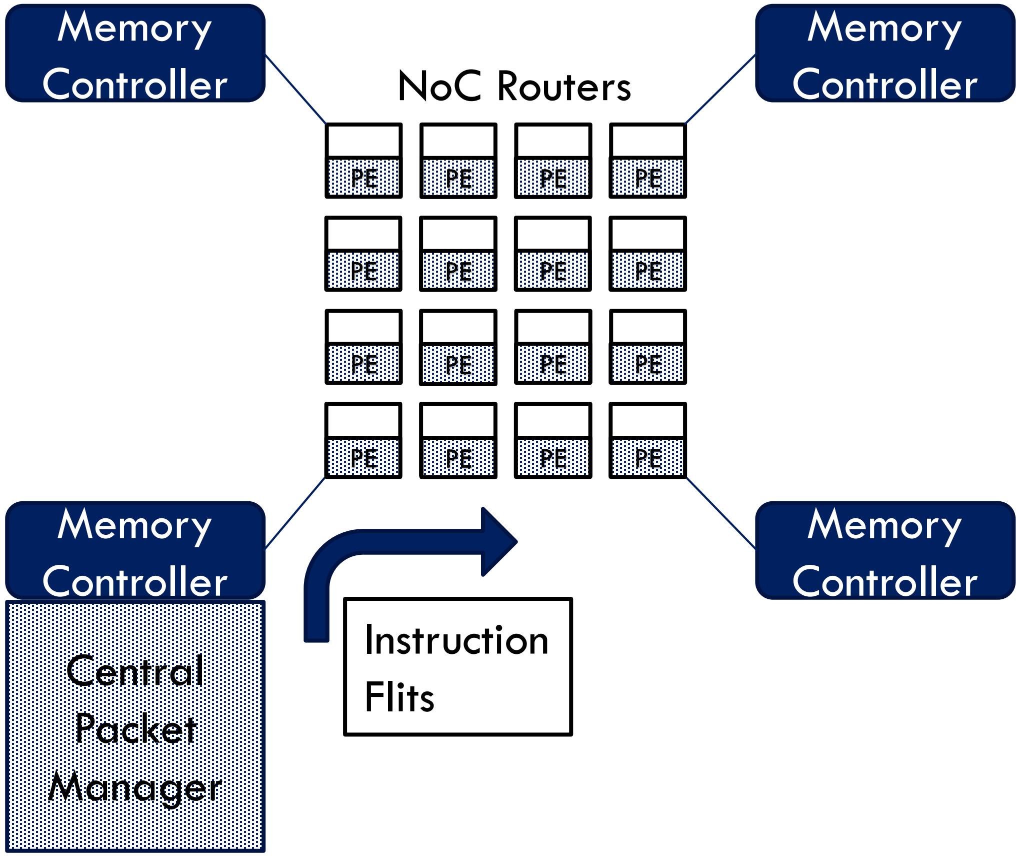

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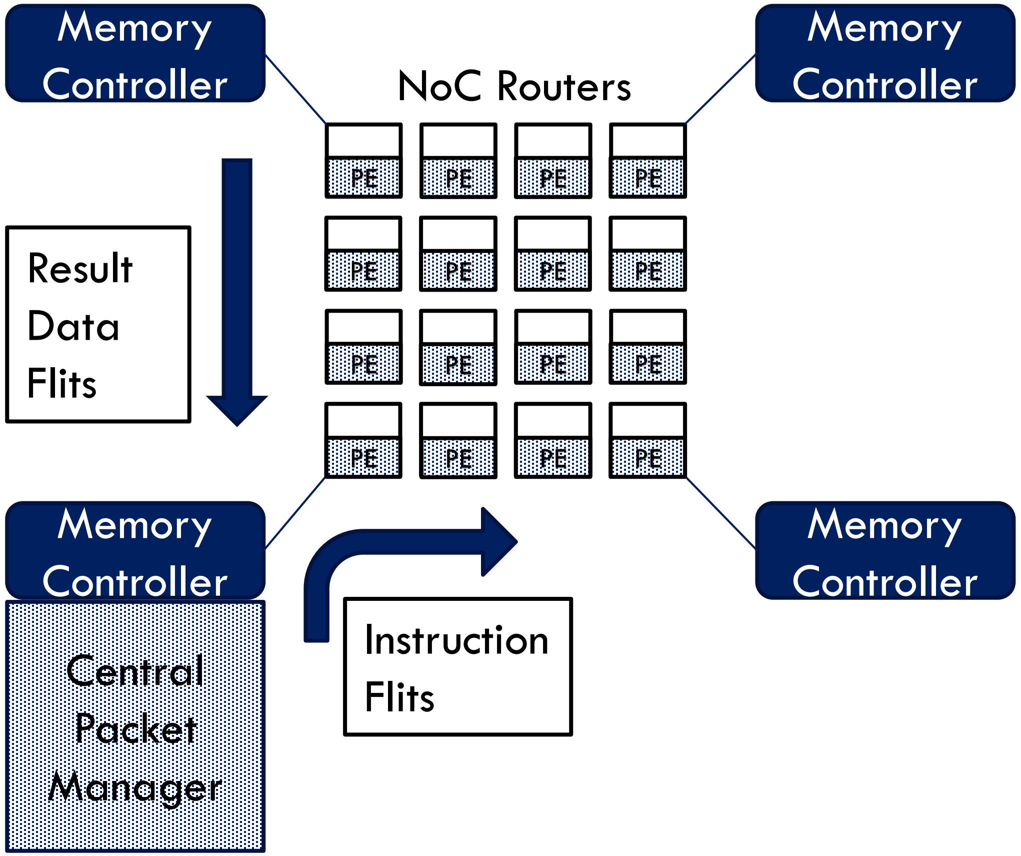

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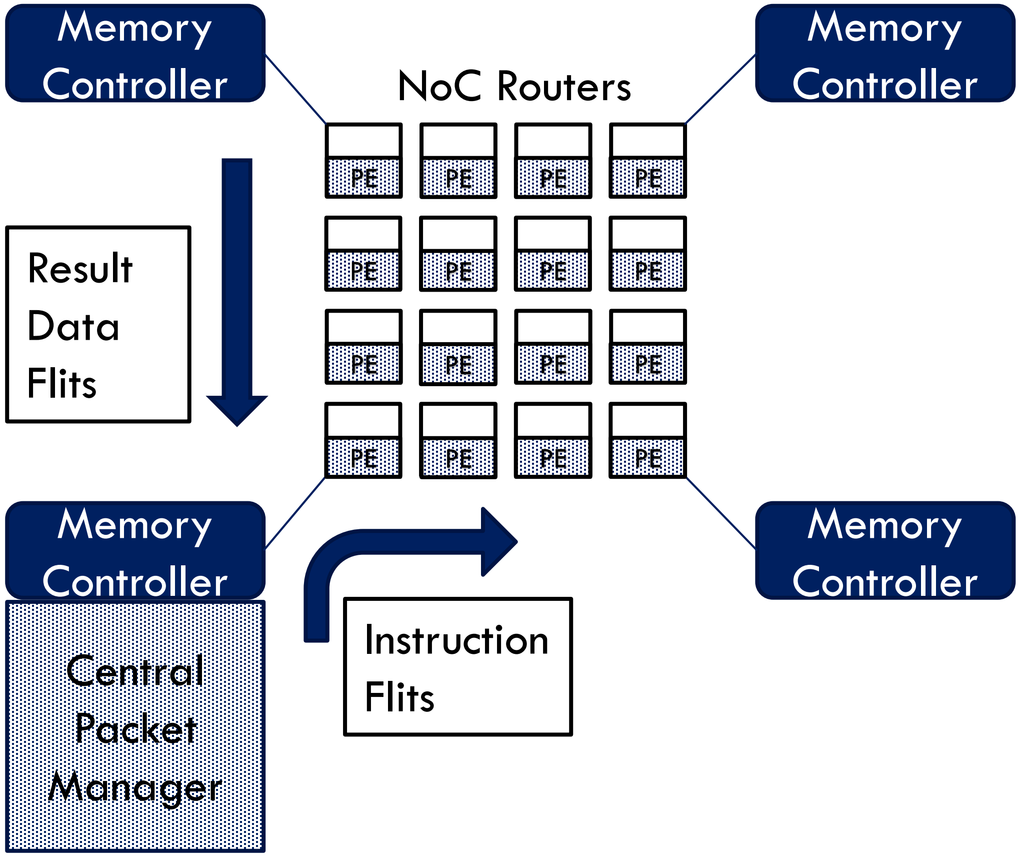
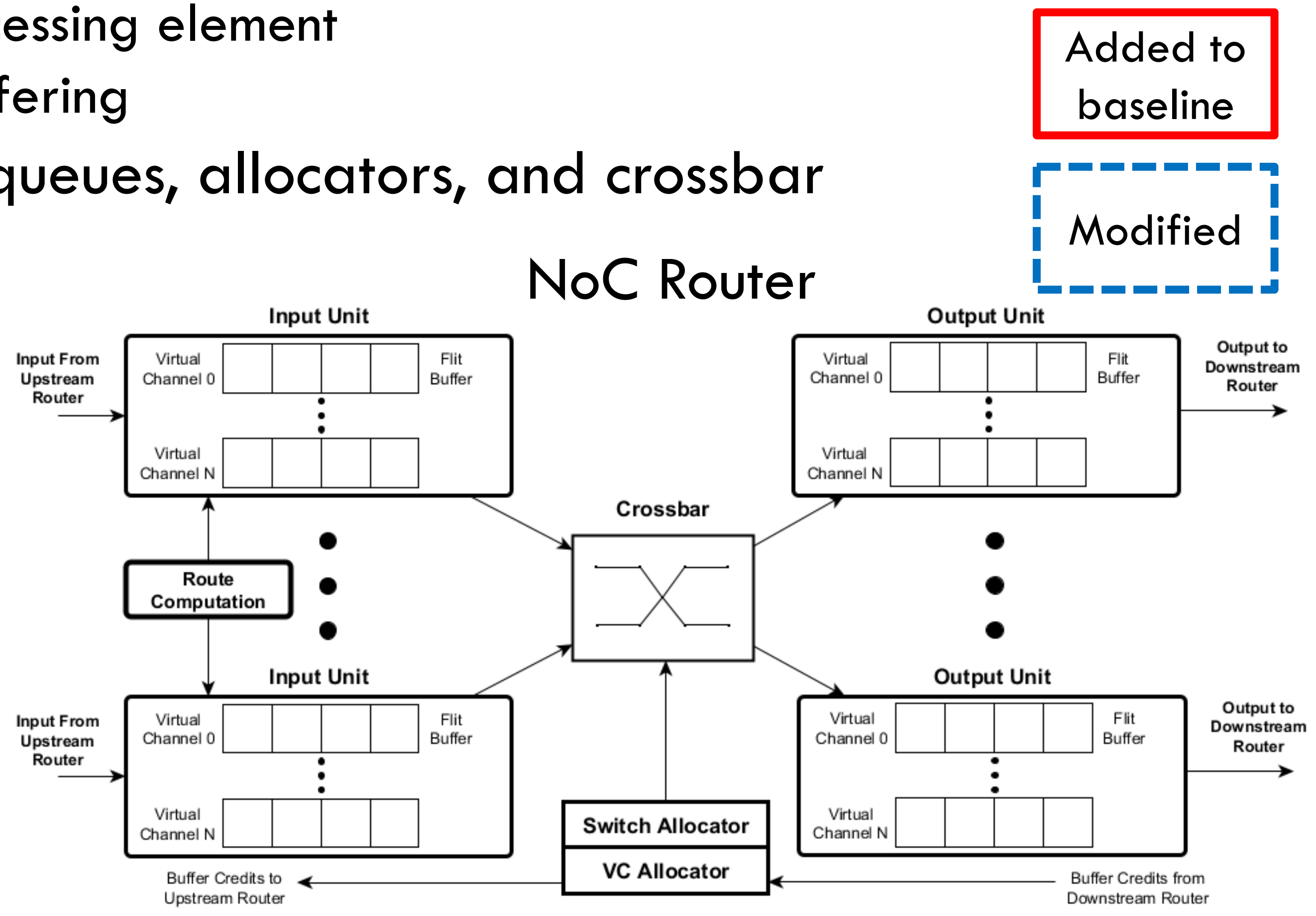
- Added features to a traditional NoC:
  - CPU traffic priority arbitration
  - Available NoC buffers as transient data storage



NoC Router Modification and RCU Additions

- Router Compute Units (RCUs)
  - 32-bit accumulator-based processing element
  - Instruction re-ordering and buffering
- Modifications to input buffer queues, allocators, and crossbar



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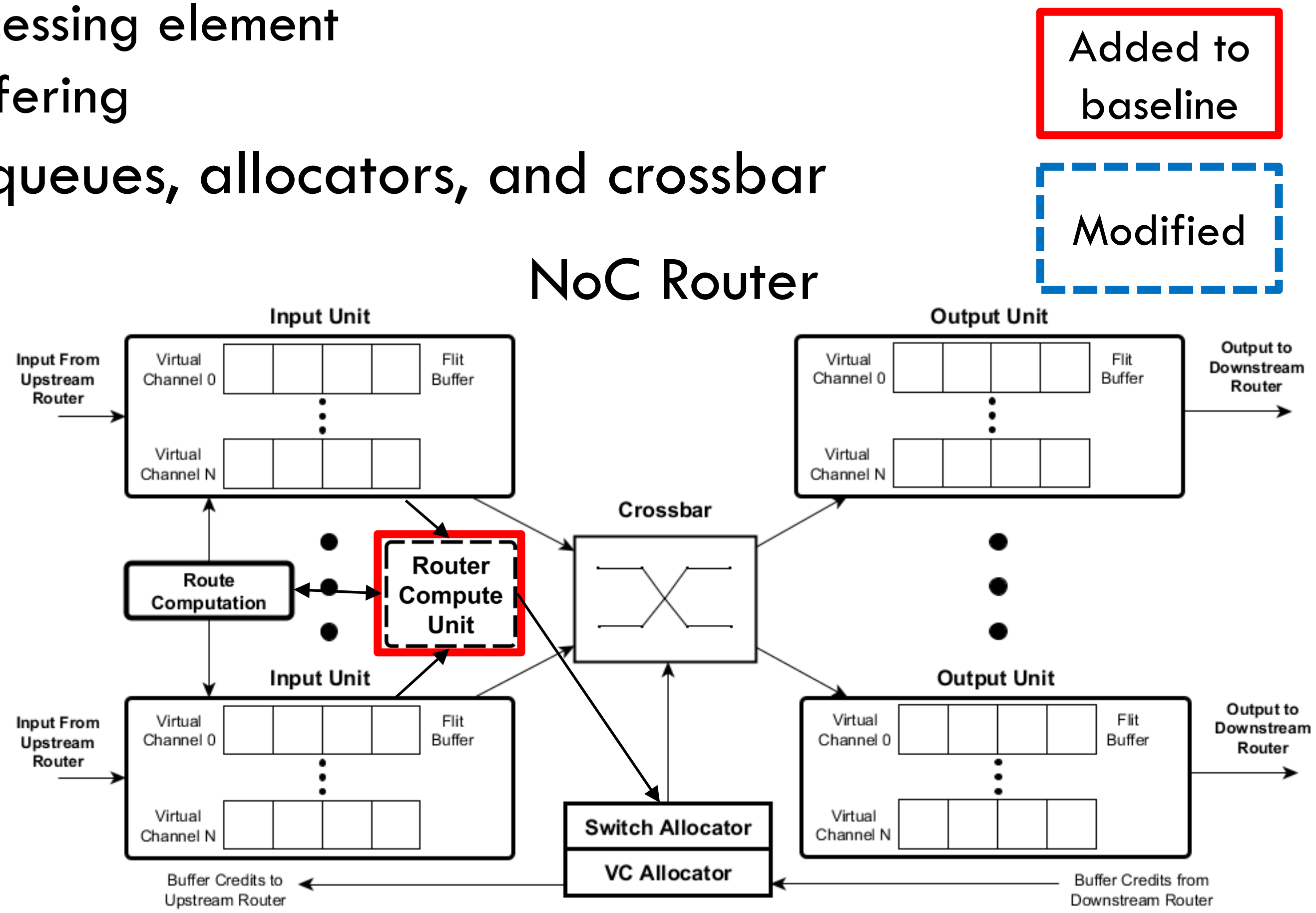

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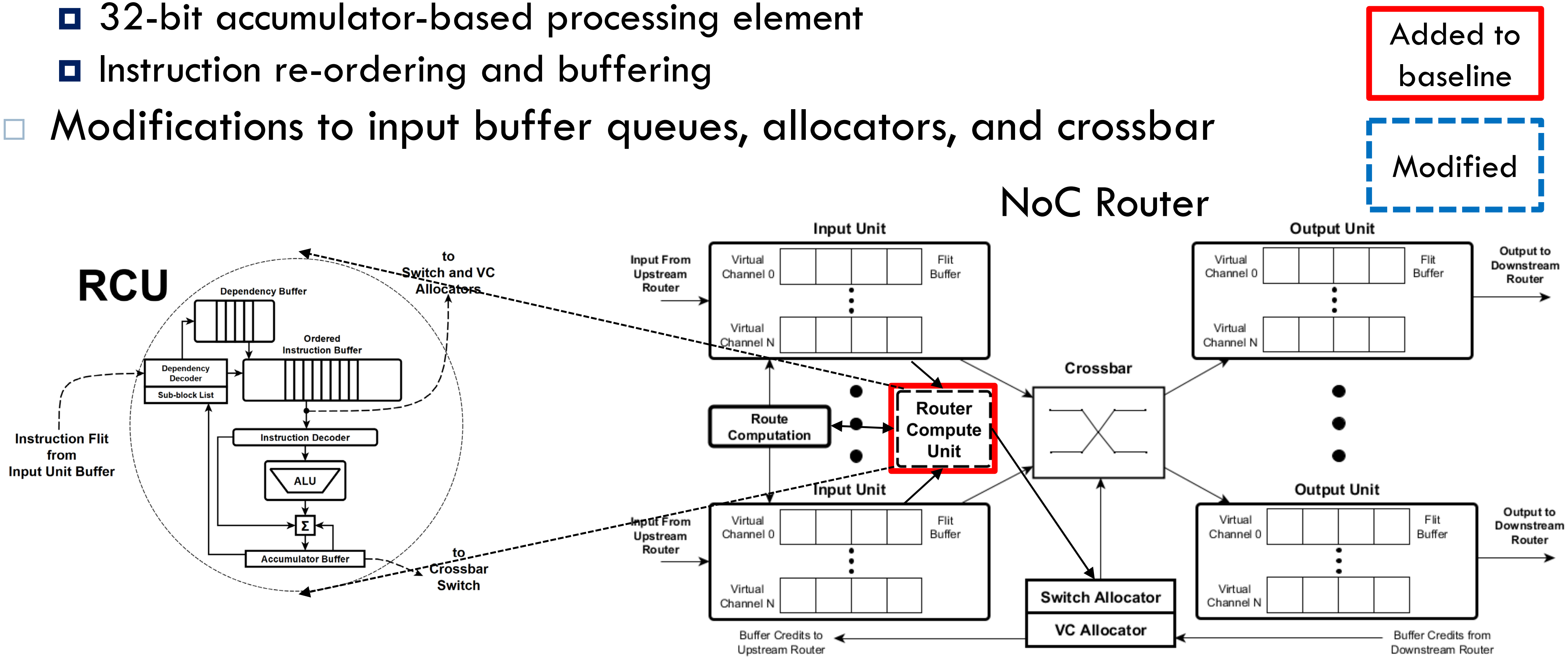

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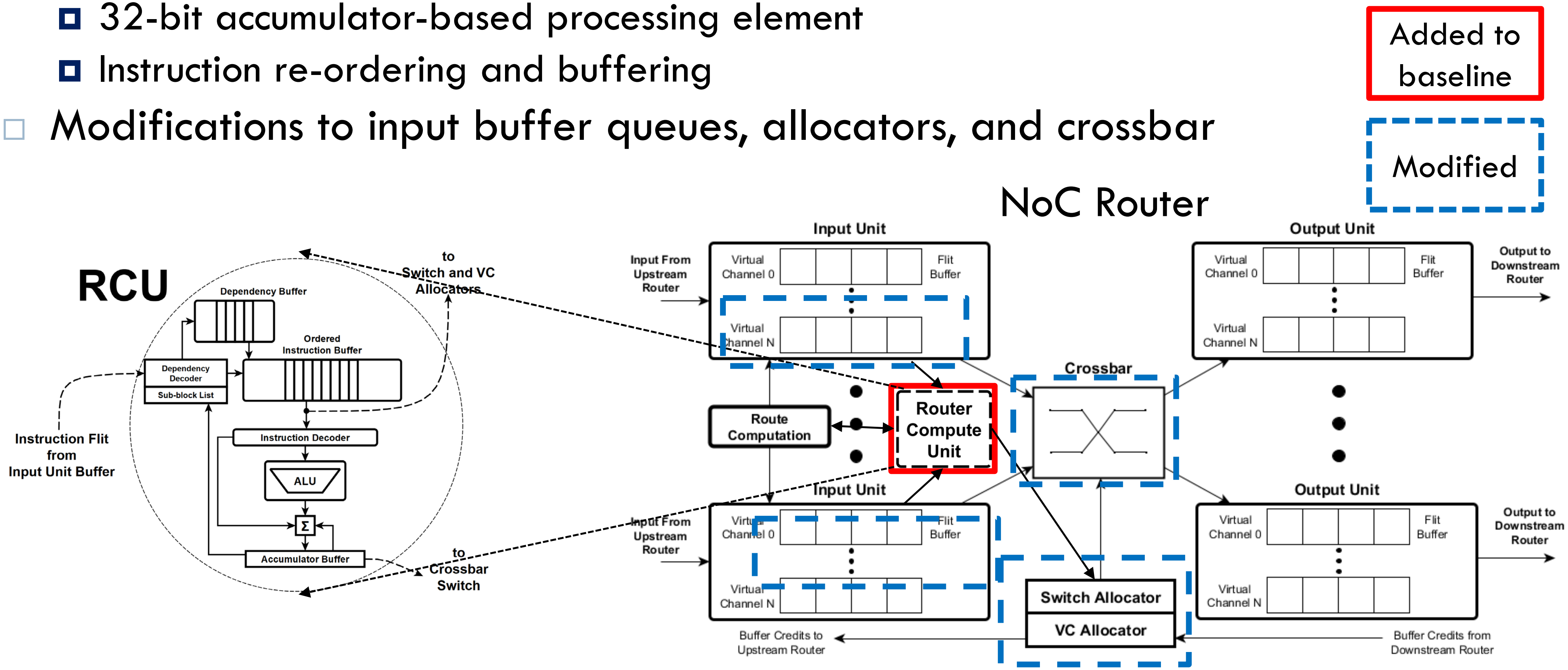
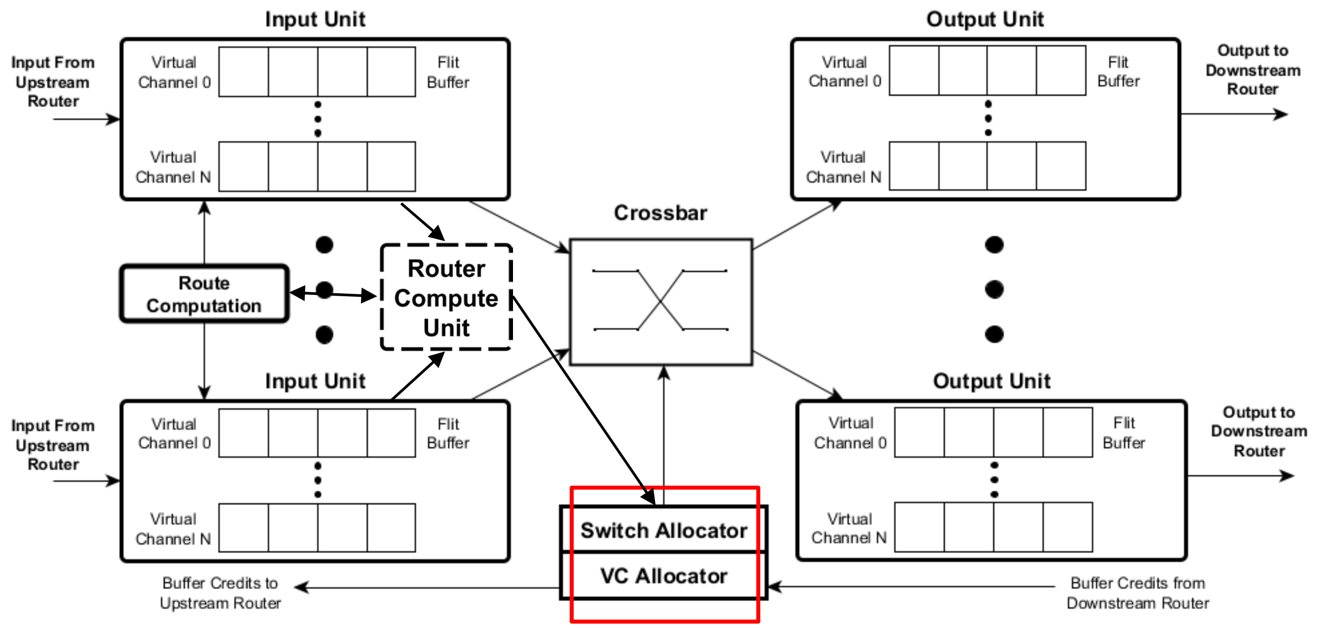


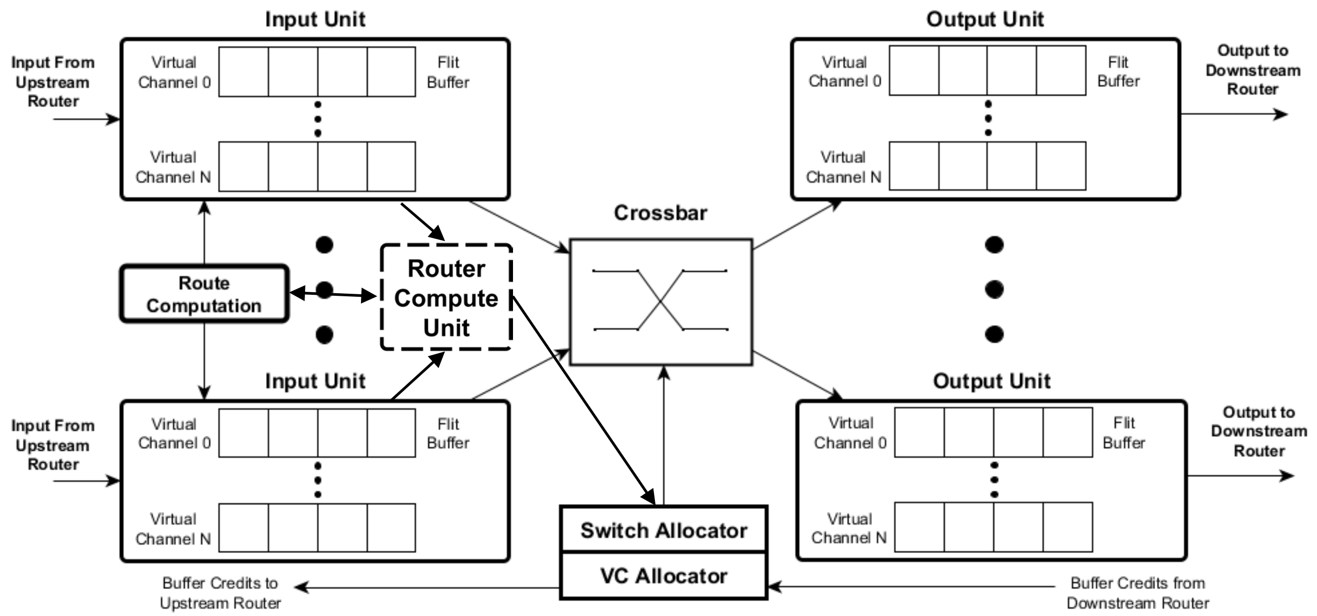
CPU Traffic Priority Arbitration

- Primary functionality of NoC is to transfer CPU core and memory traffic
  - “Fair” allocators are typically set to select traffic in round-robin
  - Allocators are modified to prioritize CPU traffic over SnackNoC instruction or data traffic



Transient Data Storage

- Input buffers typically have low contention
  - Available buffers and bandwidth can be used as transient storage
    - Useful to keep intermediate results and read-only values on chip



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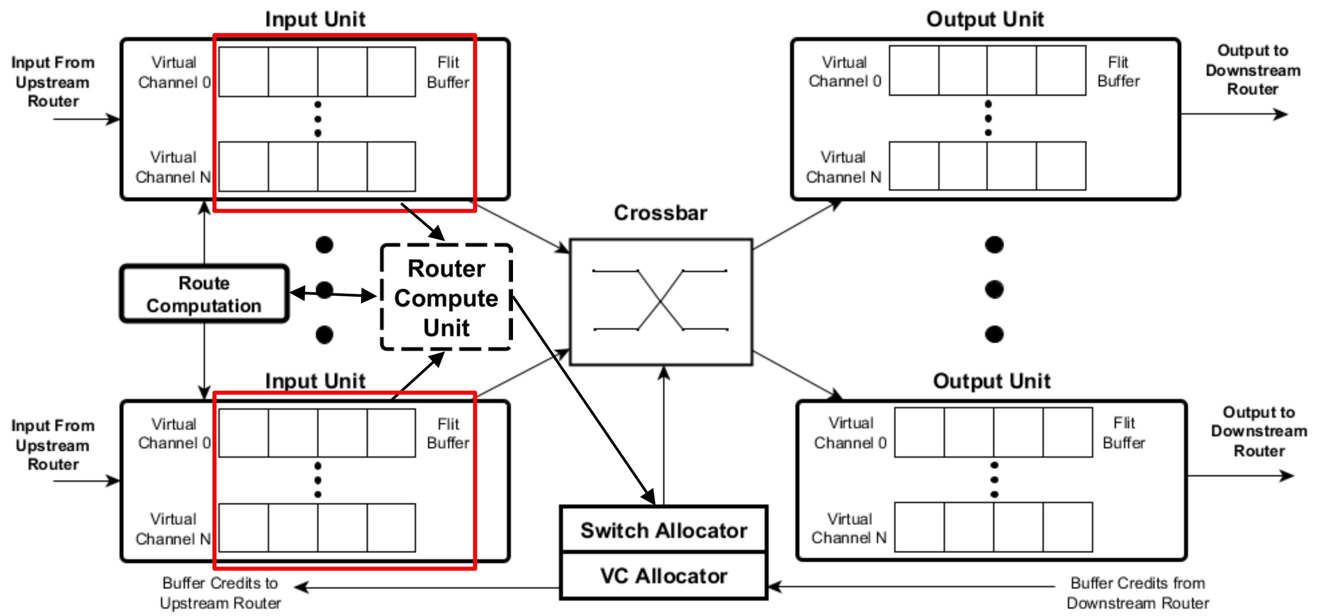

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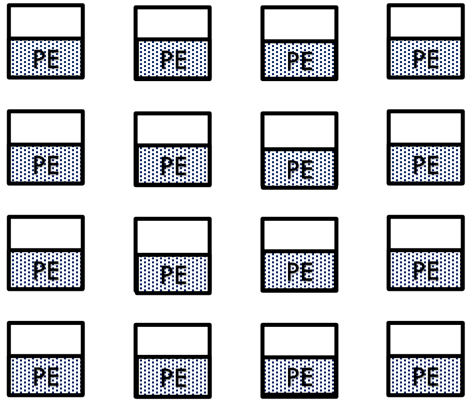
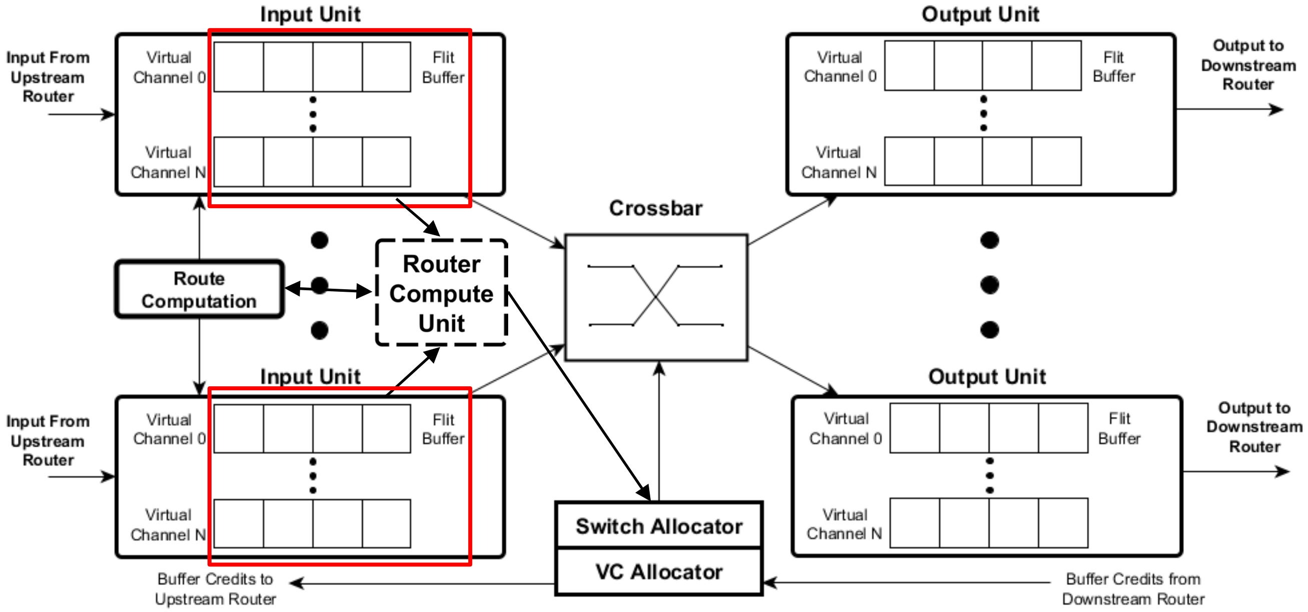
NoC Routers





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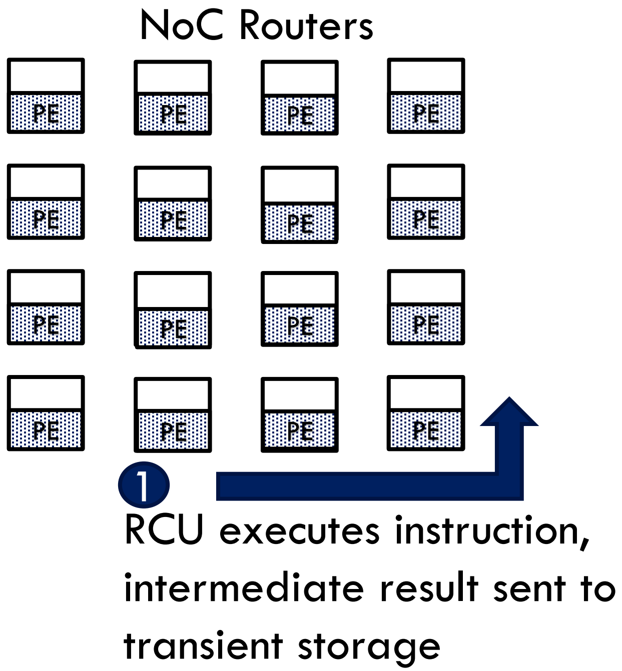

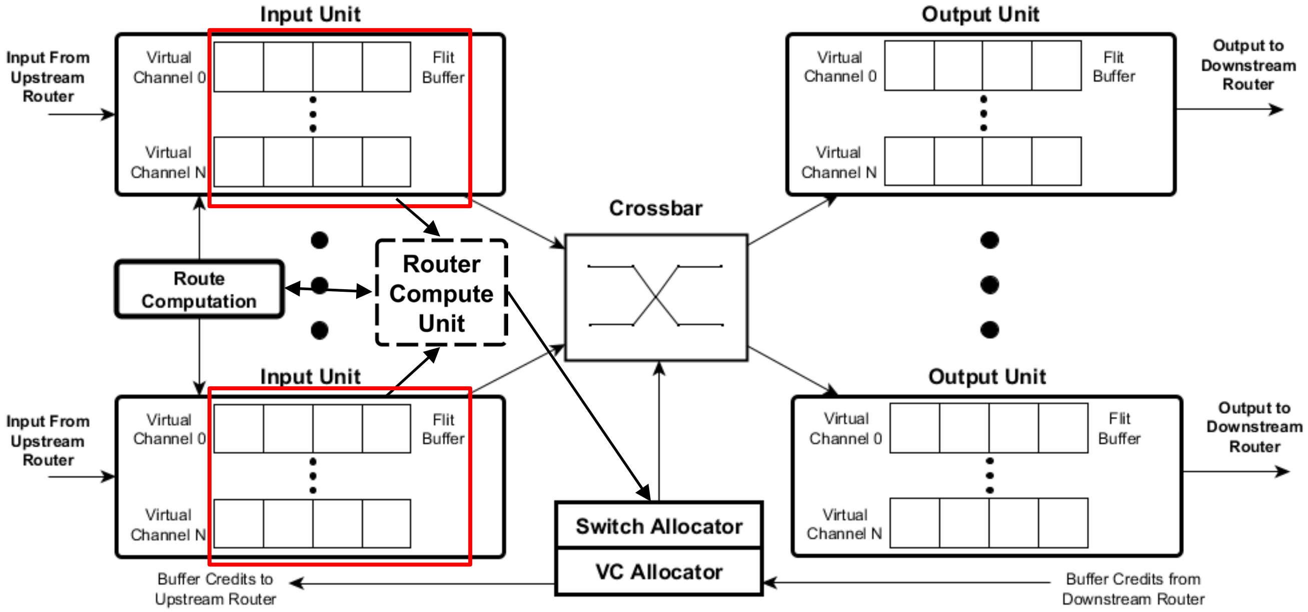

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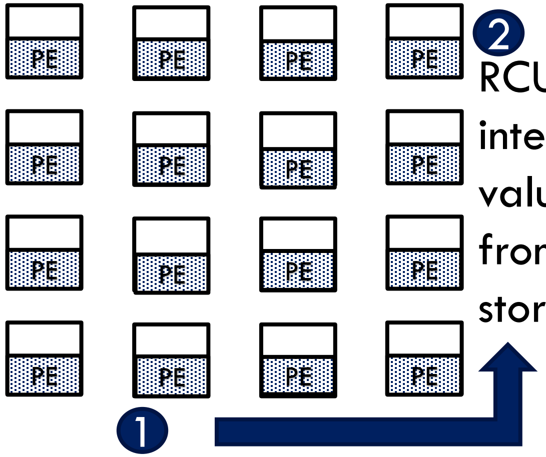
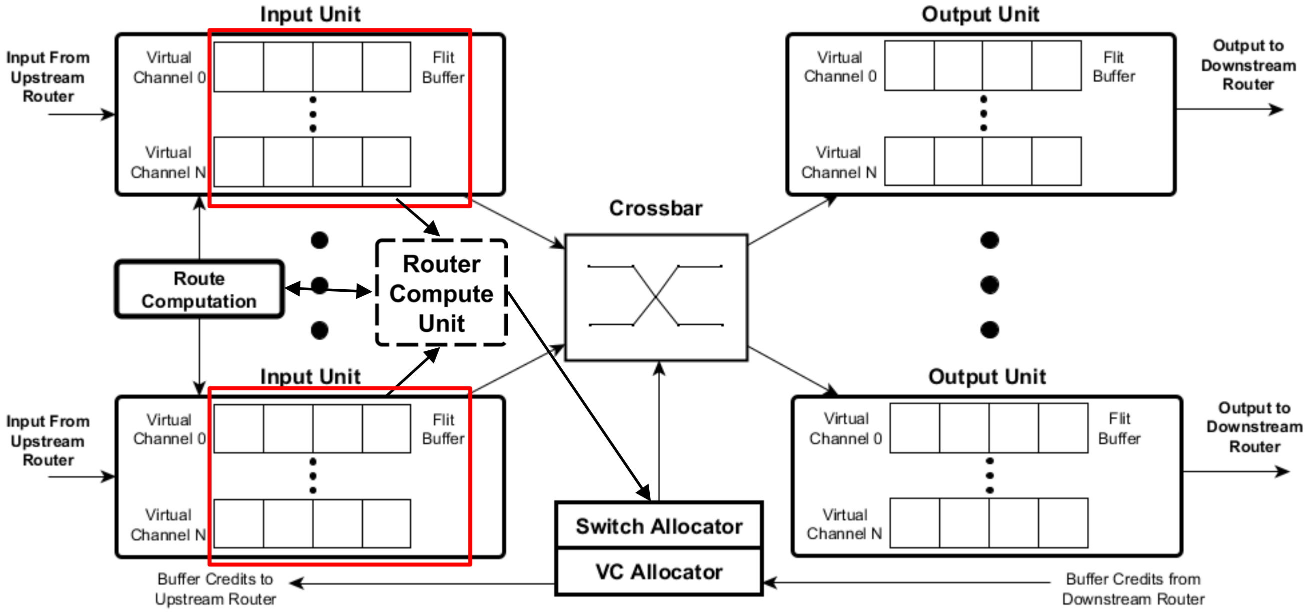


2 RCU waiting on intermediate value, received from transient storage

1 RCU executes instruction, intermediate result sent to transient storage



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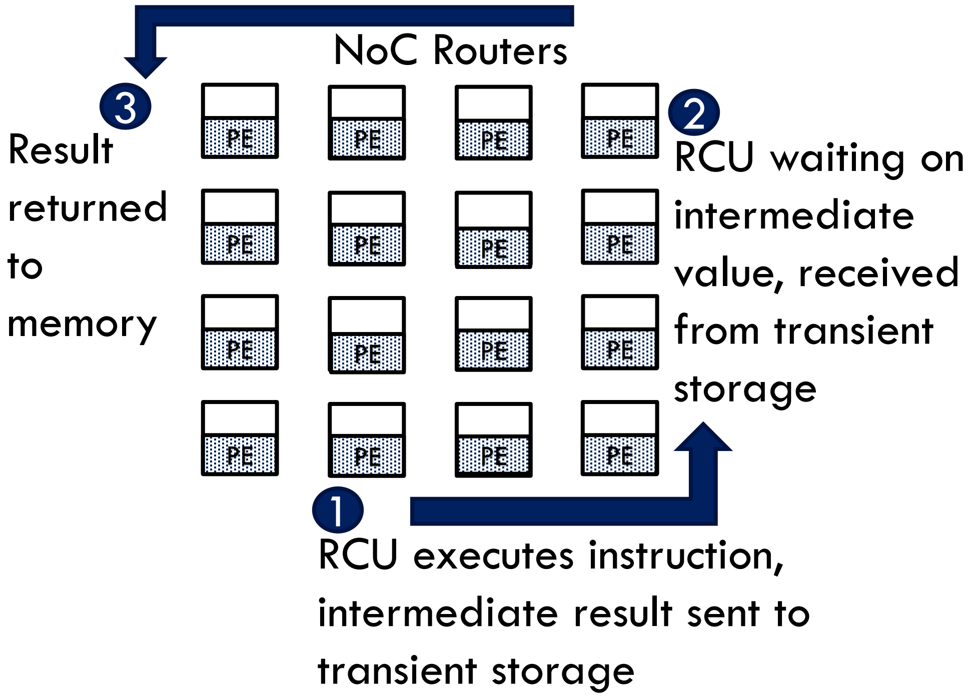

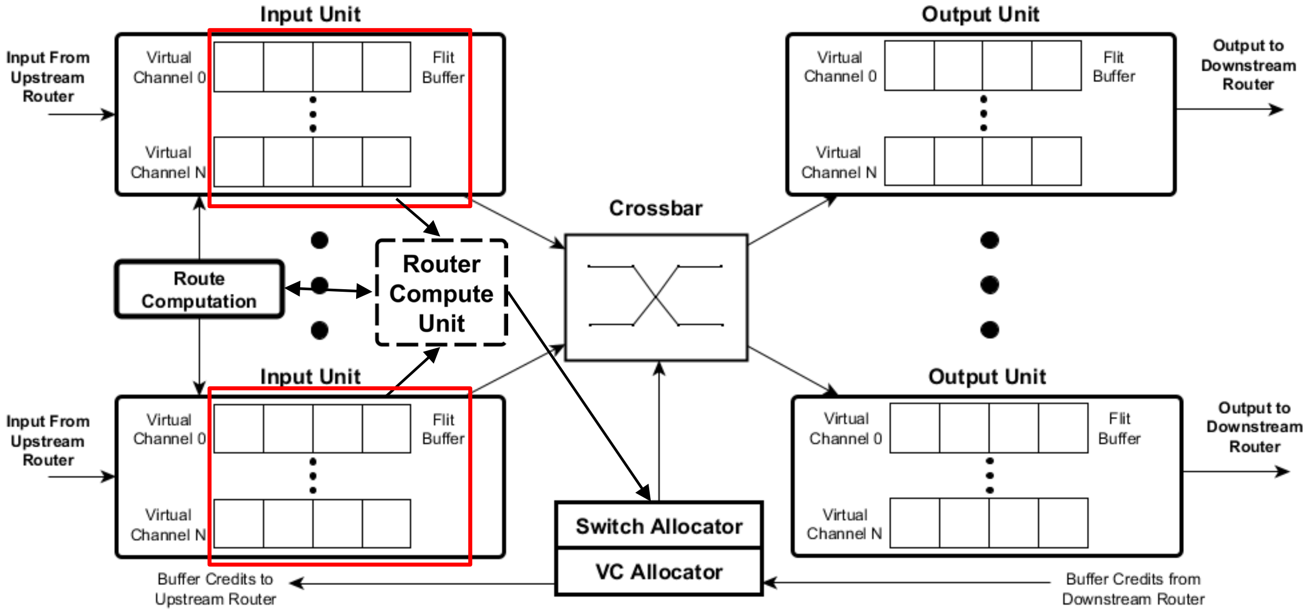

Running a SnackNoC Kernel

❶ C-code APIs for Matrix-multiply

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snA = sn_create_mat(cxt, "A", A, l, m);
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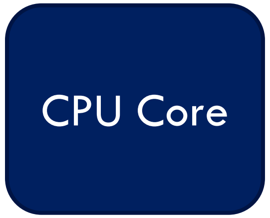

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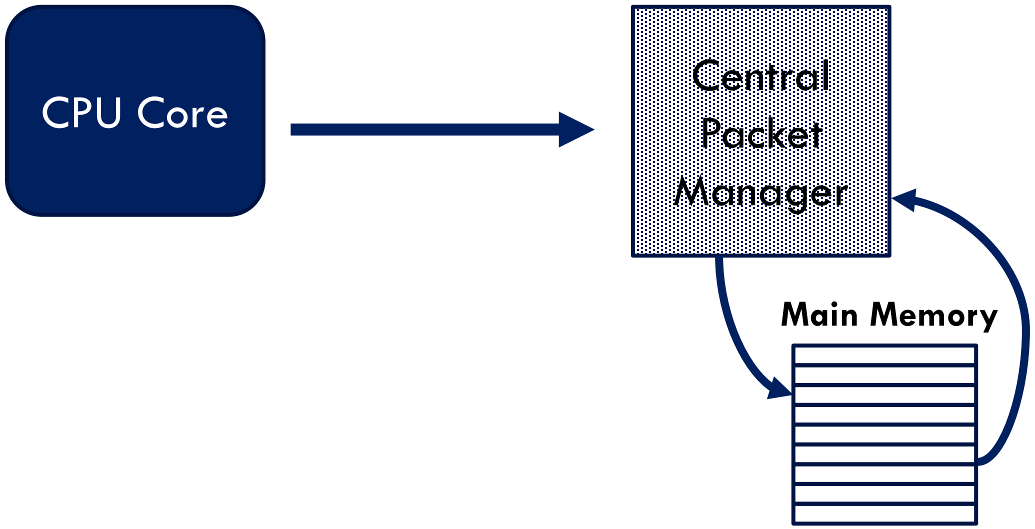
❷ CPM sets up kernel



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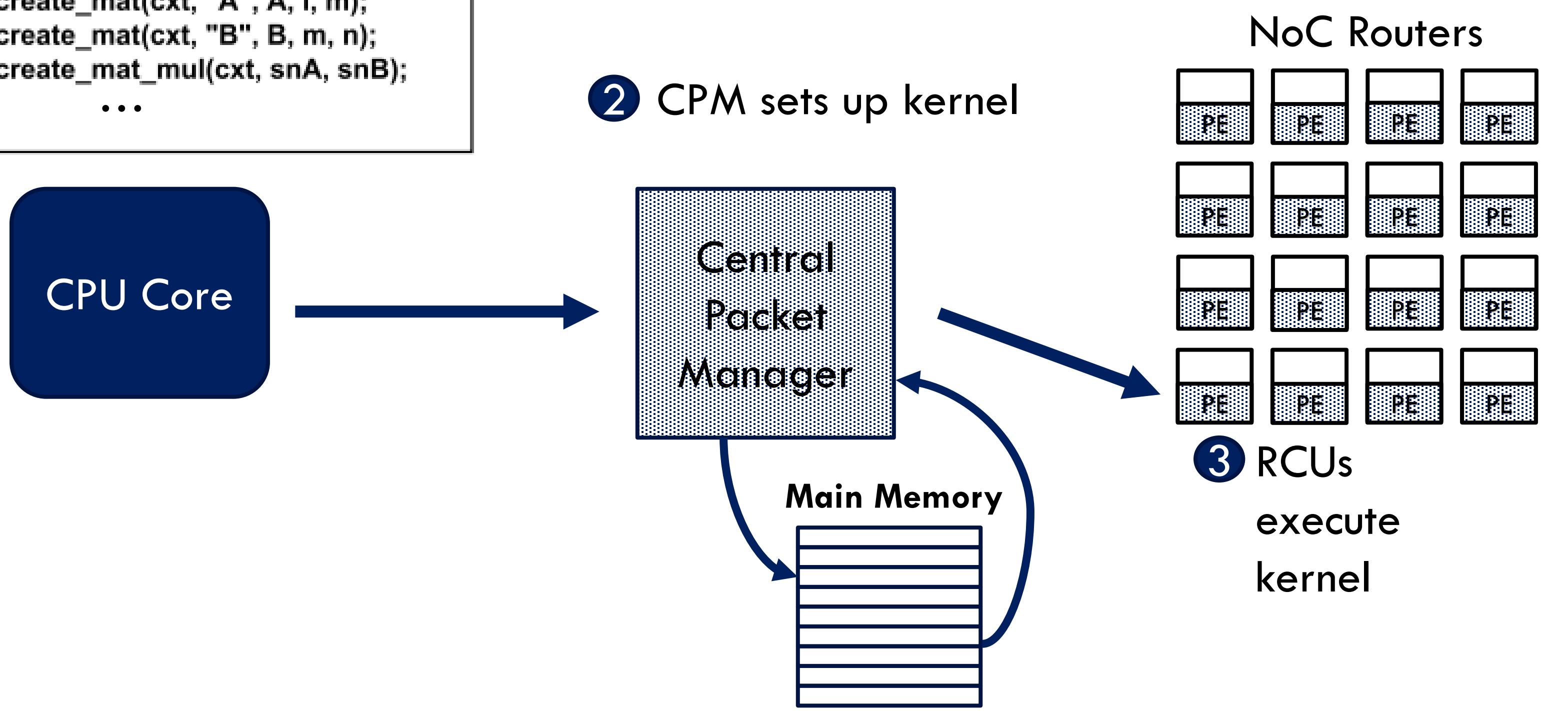

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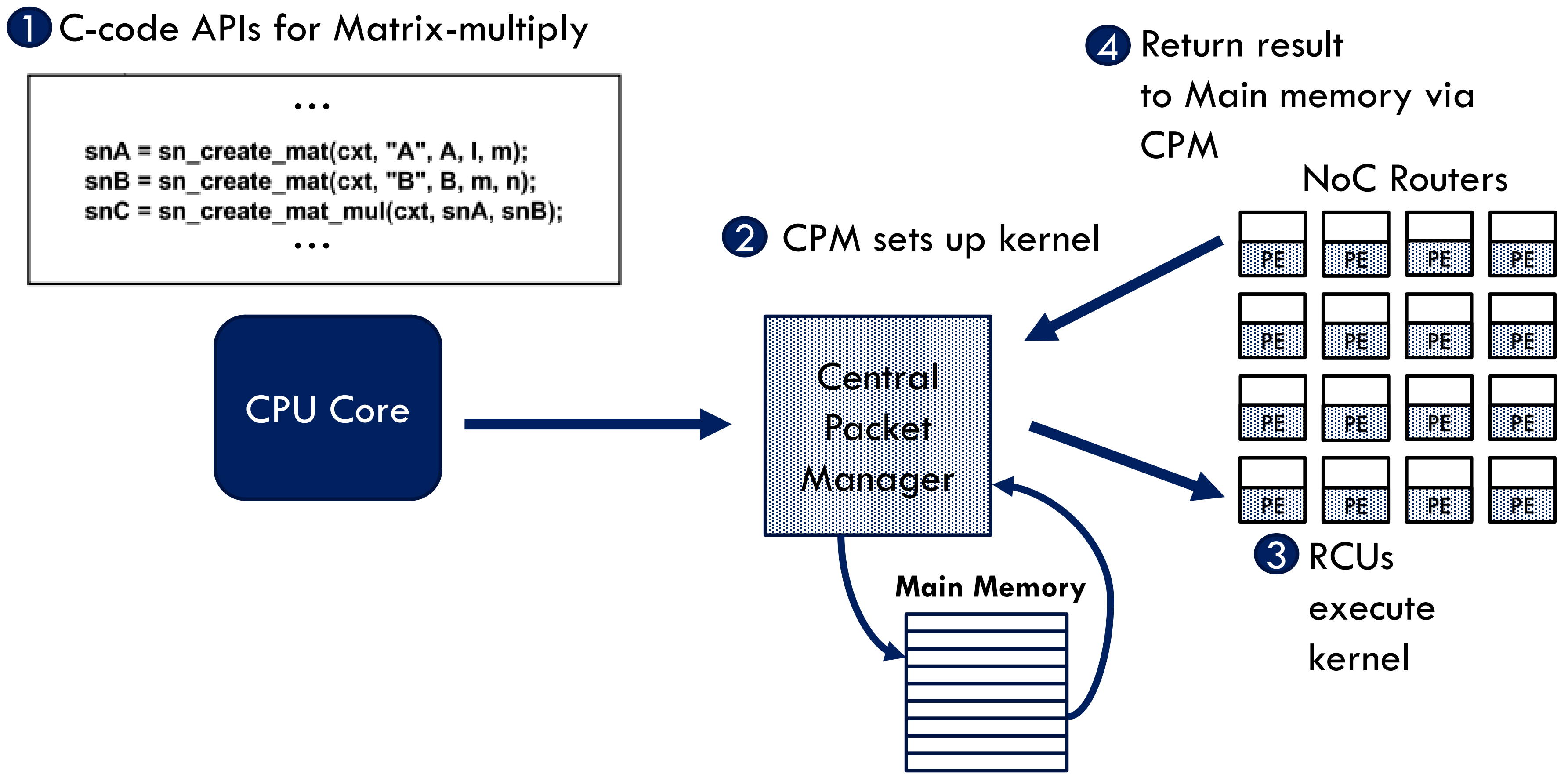
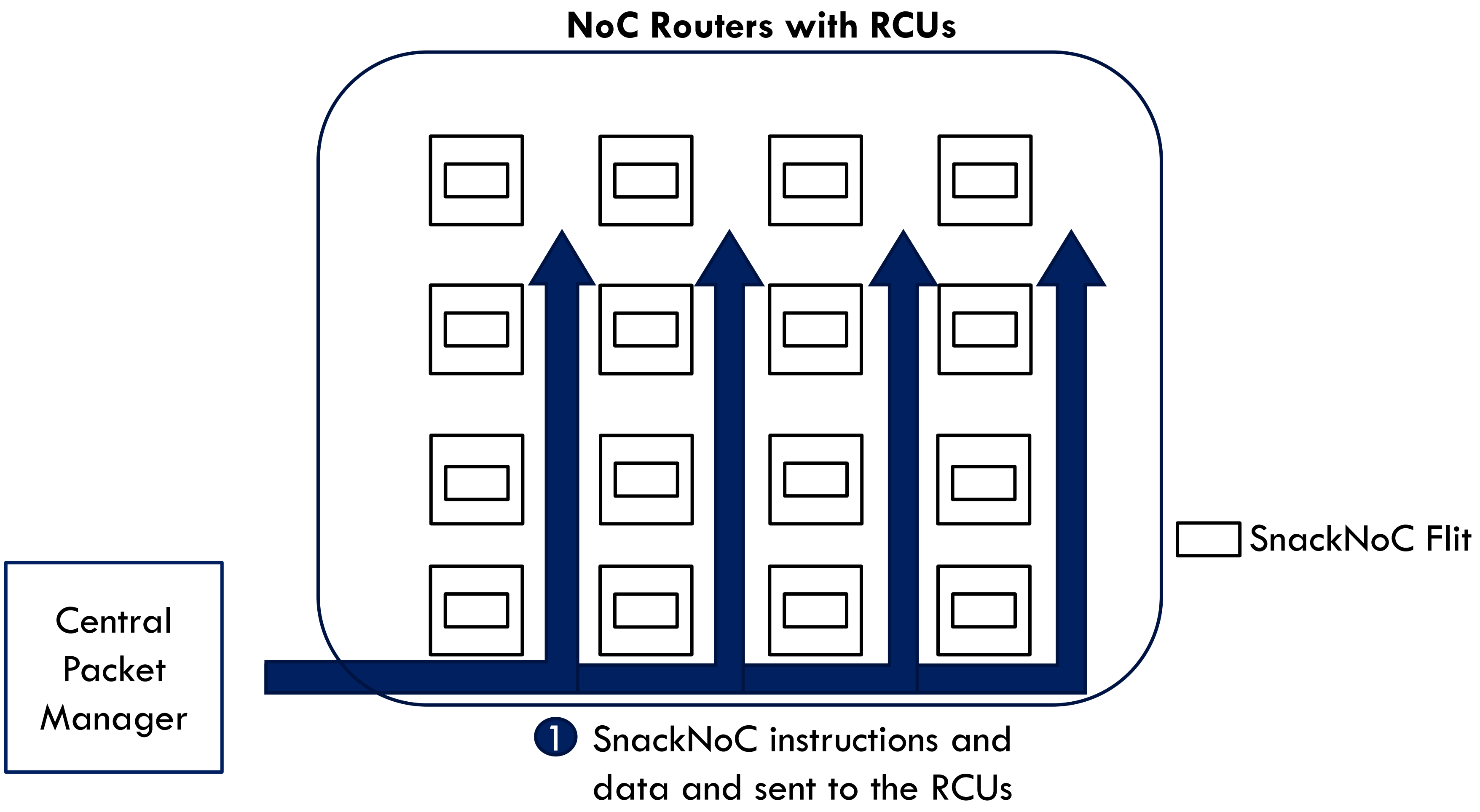


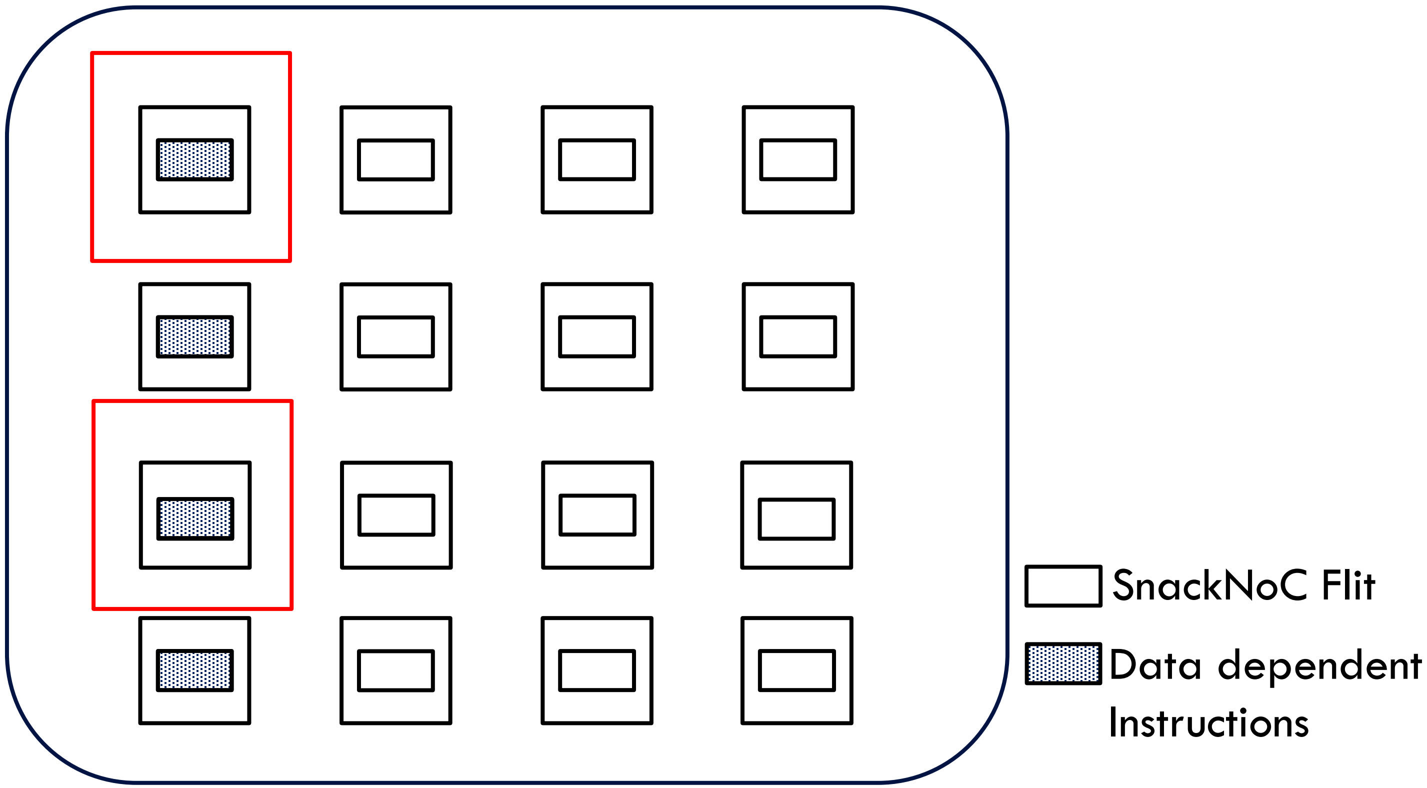
Example of a Reduction Kernel



Example of a Reduction Kernel

NoC Routers with RCUs

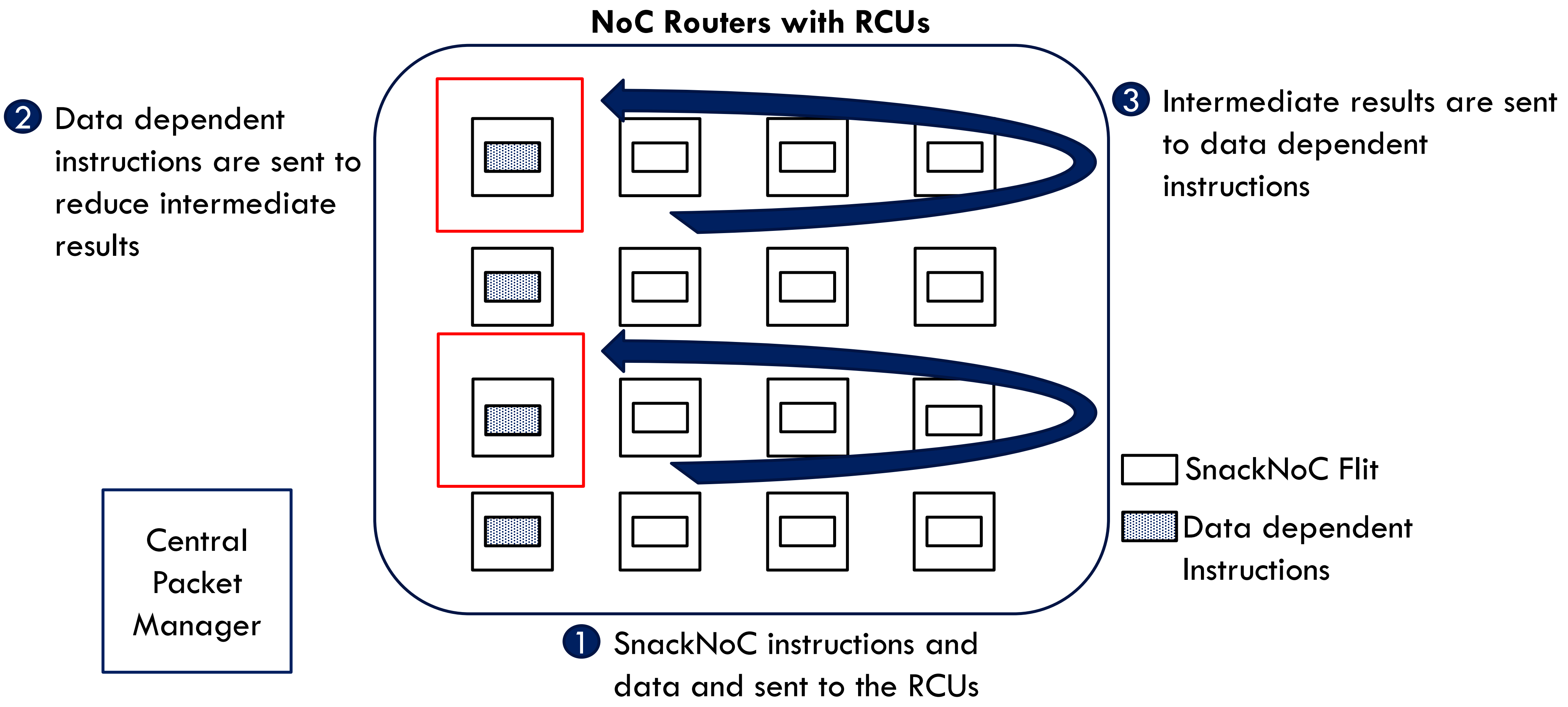
❷ Data dependent instructions are sent to reduce intermediate results



Central Packet Manager

❶ SnackNoC instructions and data and sent to the RCUs

Example of a Reduction Kernel



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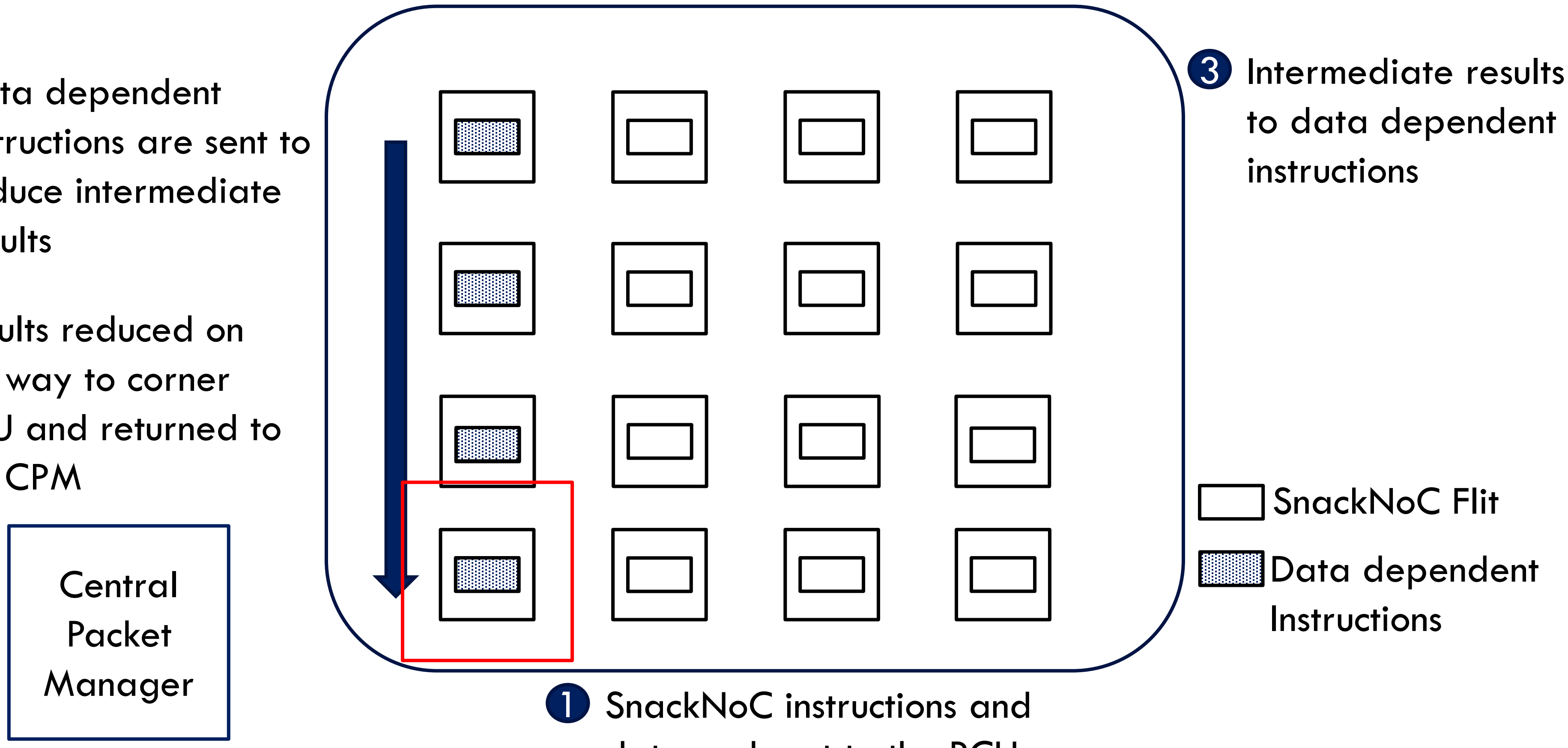
NoC Routers with RCUs

❷ Data dependent instructions are sent to reduce intermediate results

❹ Results reduced on the way to corner RCU and returned to the CPM



❸ Intermediate results are sent to data dependent instructions

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Central Packet Manager

❸ Intermediate results are sent to data dependent instructions

Repurposed our NoC router crossbar, network links, and internal buffers to compute this kernel.

SnackNoC Flit

Data dependent Instructions

❶ SnackNoC instructions and data and sent to the RCUs

Overview

- “Slack” of the Communication Fabric
- The SnackNoC Platform
- **Experimental Results**
- Conclusion and Future Considerations

Methodology

- Experiments:
  1. Assess the performance of SnackNoC
     - How many additional cores worth of performance can SnackNoC provide opportunistically?
  2. Quantify the performance interference of operating SnackNoC on the CPU cores

Implemented four SnackNoC kernels (SGEMM, Reduction, MAC, SPMV)

Executed 16 multi-threaded benchmarks from PARSEC3, Splash2X, FastForward2 to assess performance interference

Methodology – Quantifying SnackNoC Performance

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  2. Native Dell server with Intel Xeon E5-2660
     - C++ multi-threaded with OpenMP

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Native CPU Parameters	Configuration
Processor	Intel Xeon E5-2660 v3
Core Frequency	2.6GHz
L1 I&D Cache	32KB, 8-way
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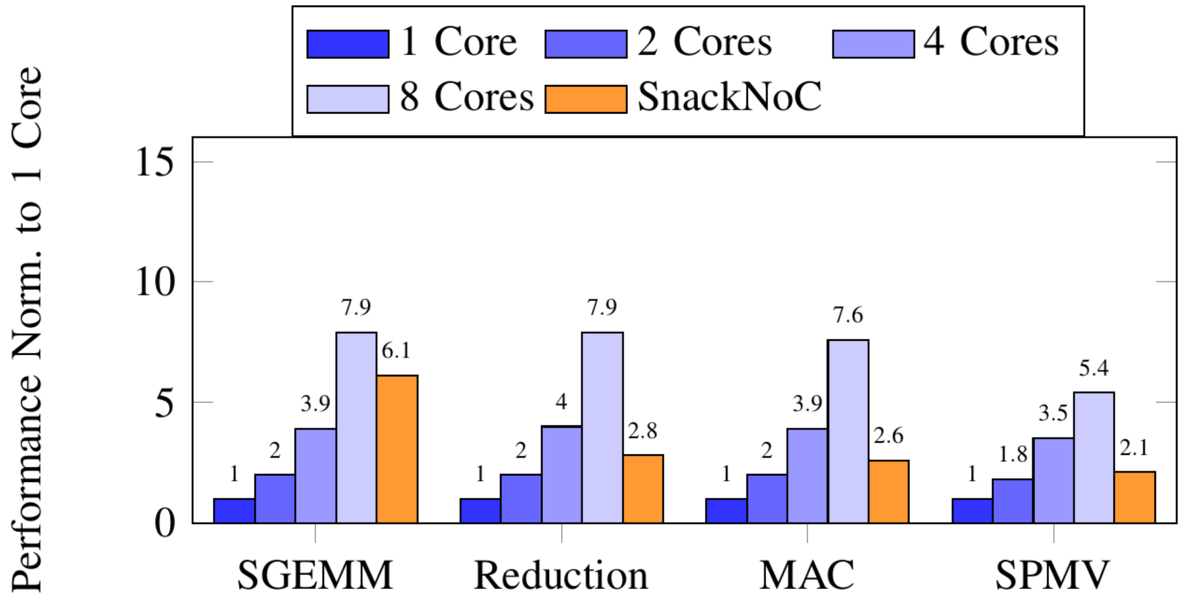
L3 Cache	20MB, 20-way

Quantifying SnackNoC Performance Gain

- SnackNoC kernels are executed on an increasing number of cores to determine comparable performance of SnackNoC



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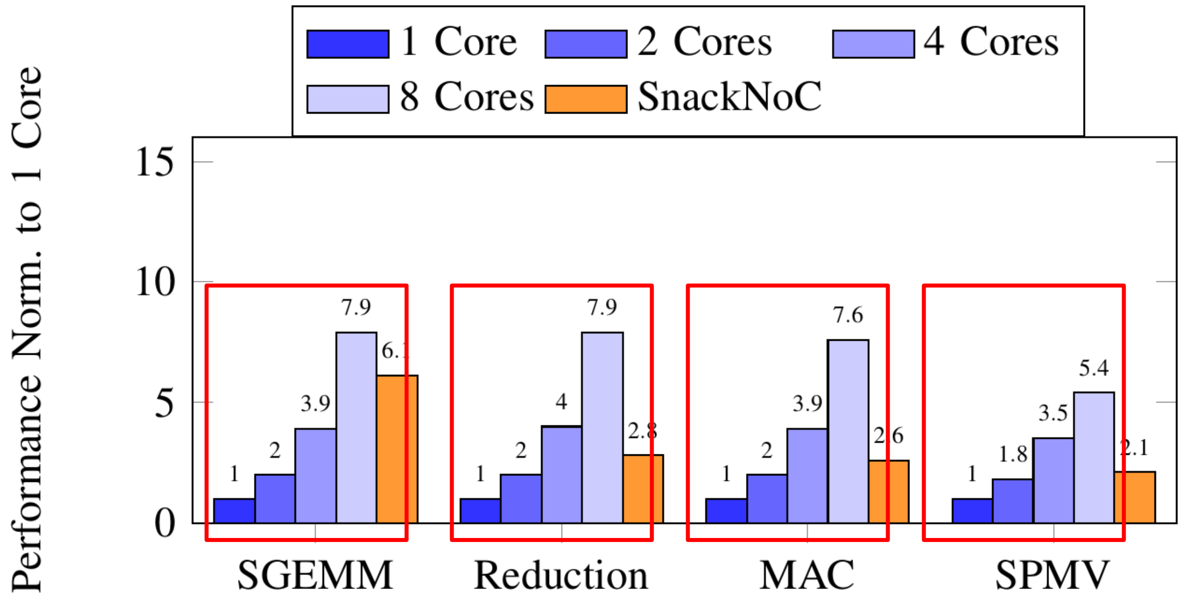

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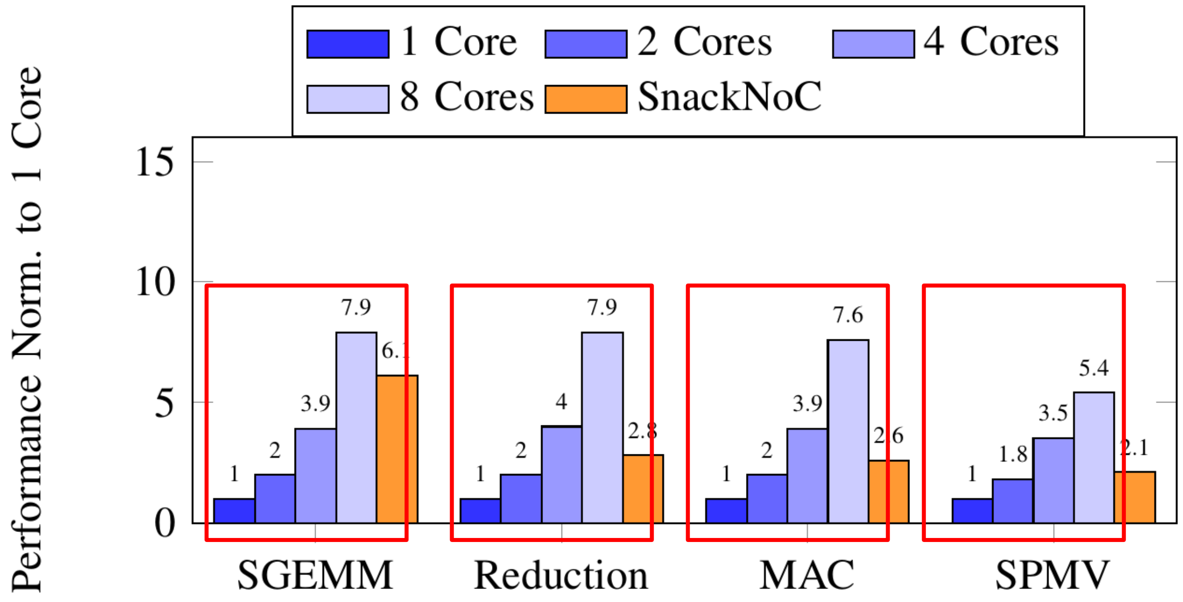

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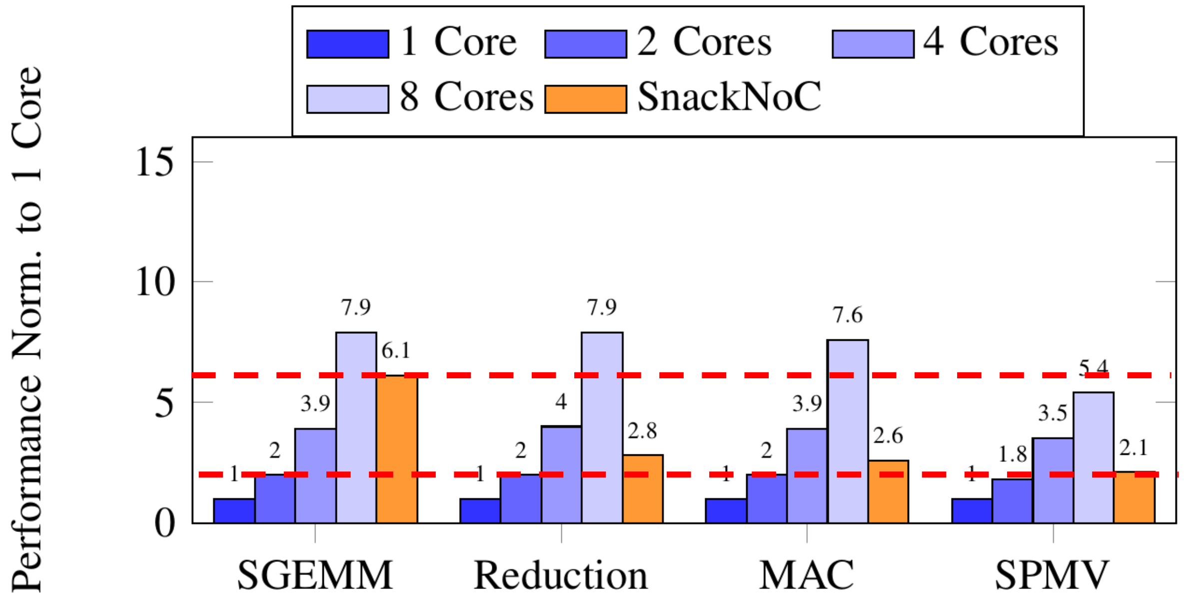
- Performance gain between 2 and 6 x86 OOO cores



SnackNoC Area and Power Overhead

- SnackNoC components' RTL implemented, synthesized with Synopsis Design Compiler:
  - 45nm NCSU technology node
  - Operating Freq. 1GHz

Router Control Unit (RCU)	Additional Power (%)	Additional Area (%)
32-bit Parallel Adder	1.14%	1.15%
32-bit Parallel Subtractor	1.14%	1.15%
32-bit Multiply and Accumulate (MAC)	2.05%	1.73%
Ordered Instruction Buffer	2.05%	2.30%
Dependency Buffer	2.51%	1.15%
Accumulator Buffer	0.68%	0.12%
Sub Block List	0.23%	1.73%
Total	**9.81%**	**9.33%**

Central Packet Manager	Additional Power (%)	Additional Area (%)
Assembly Logic and Buffers	0.08%	2.43%
Kernel State	0.16%	0.10%
Instruction Buffer	10.71%	25.75%
Offload Data Memory Buffer	0.95%	2.28%
Output Result FIFO	0.95%	2.28%
Total	**12.85%**	**33.04%**

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- Single CPM per NoC
  - 12.85% additional power per NoC
  - 33.04% additional area per NoC
    - Largest contributor is instruction buffer

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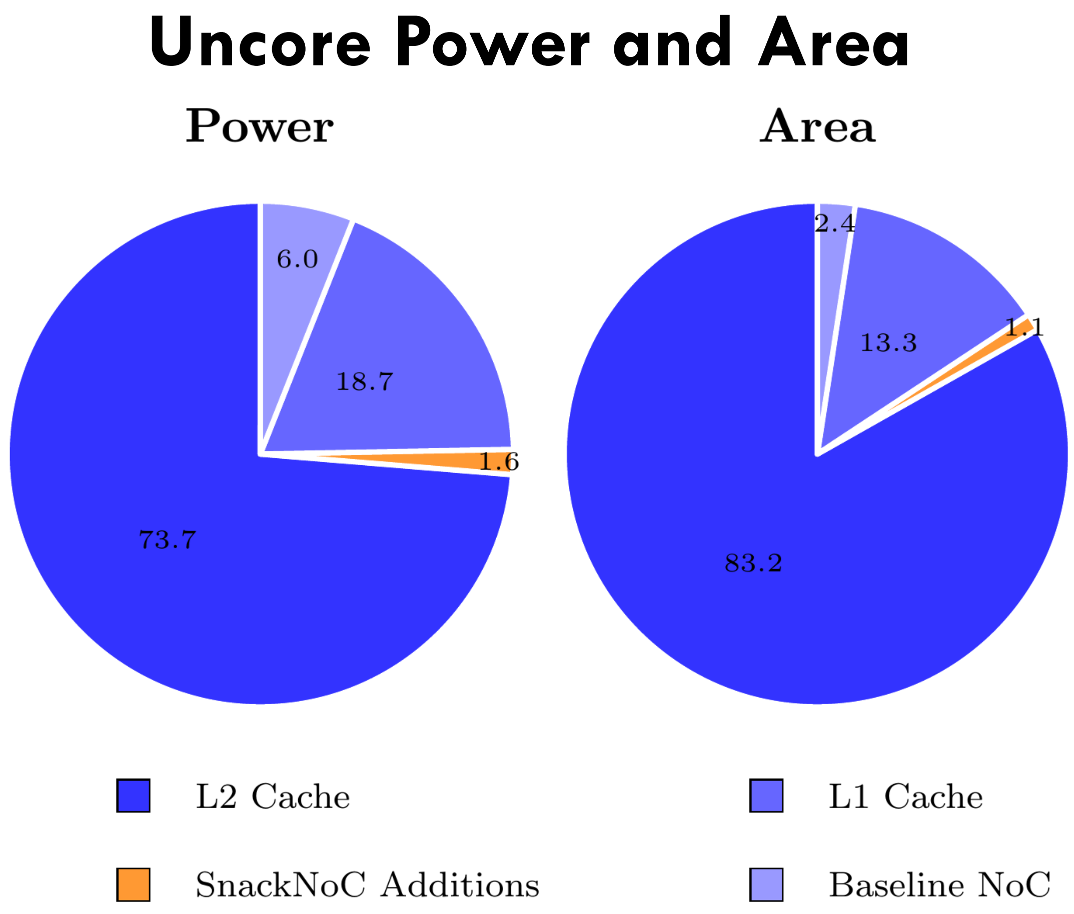

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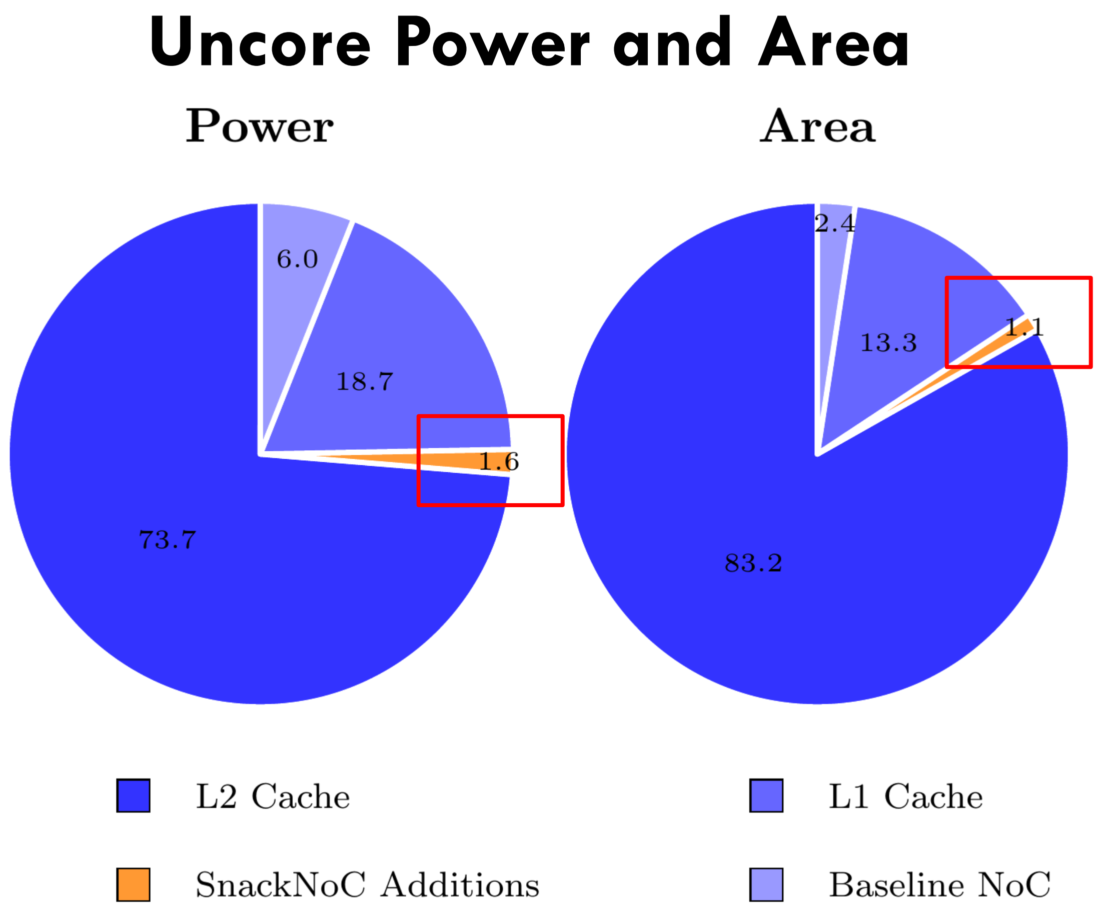

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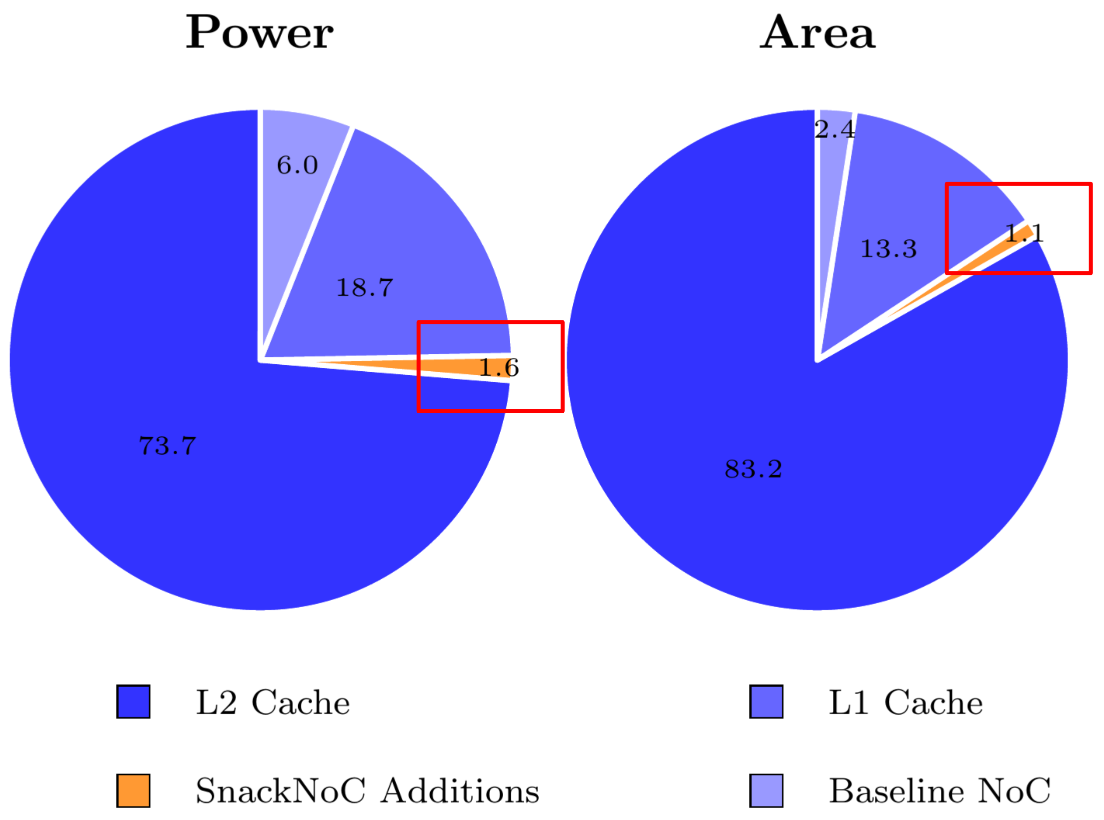
Uncore Power and Area



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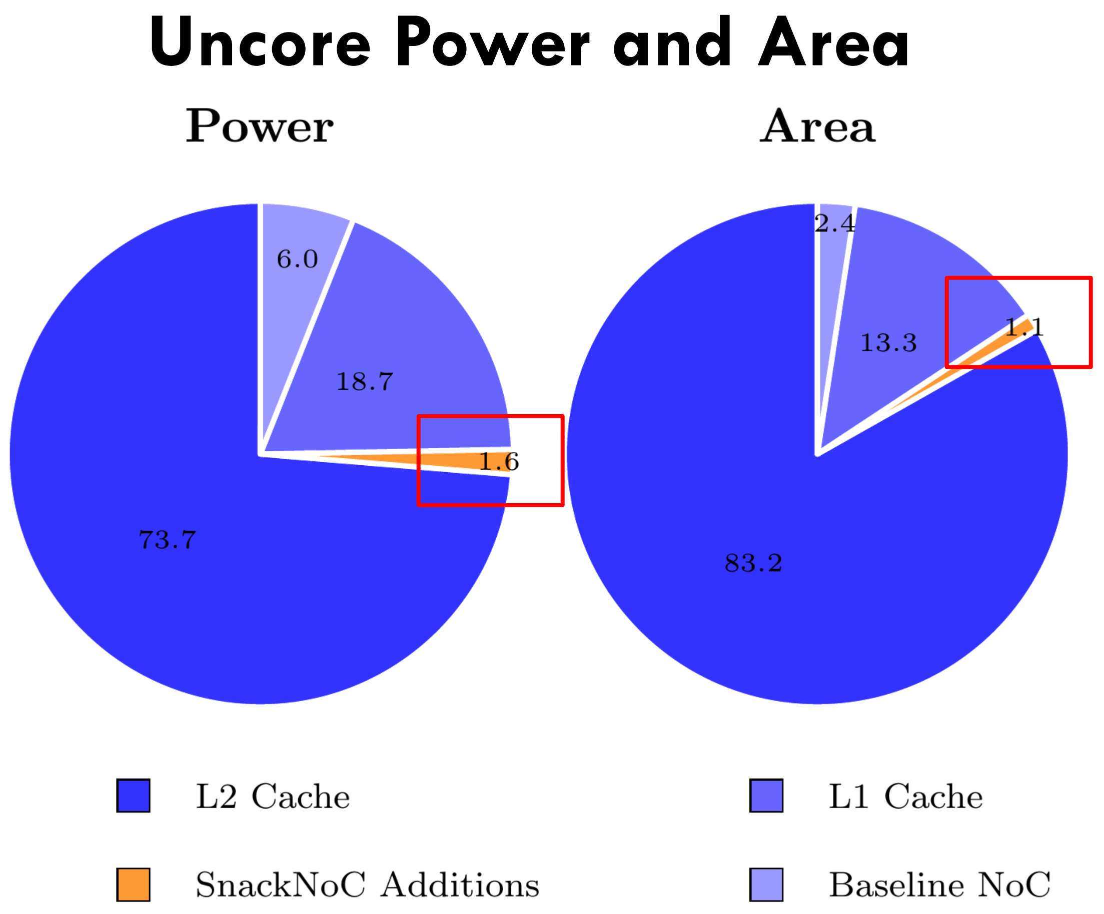
Satisfies goal of limited overhead



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- To quantify performance interference, the performance of the CMP is compared with and without SnackNoC Traffic

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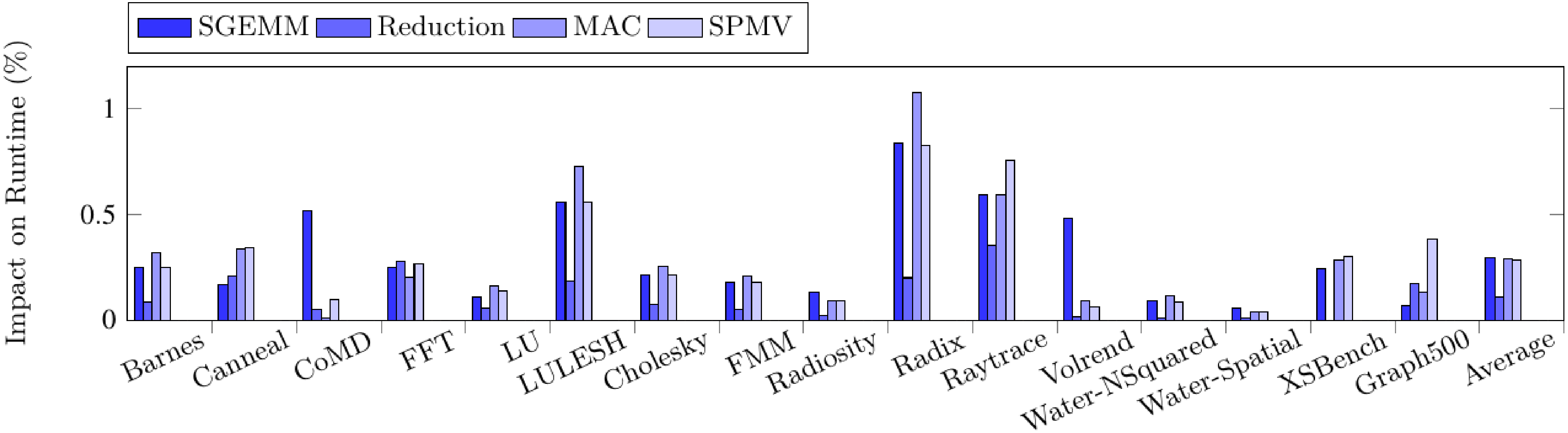
Minimal impact of “Snacking” on CMP performance



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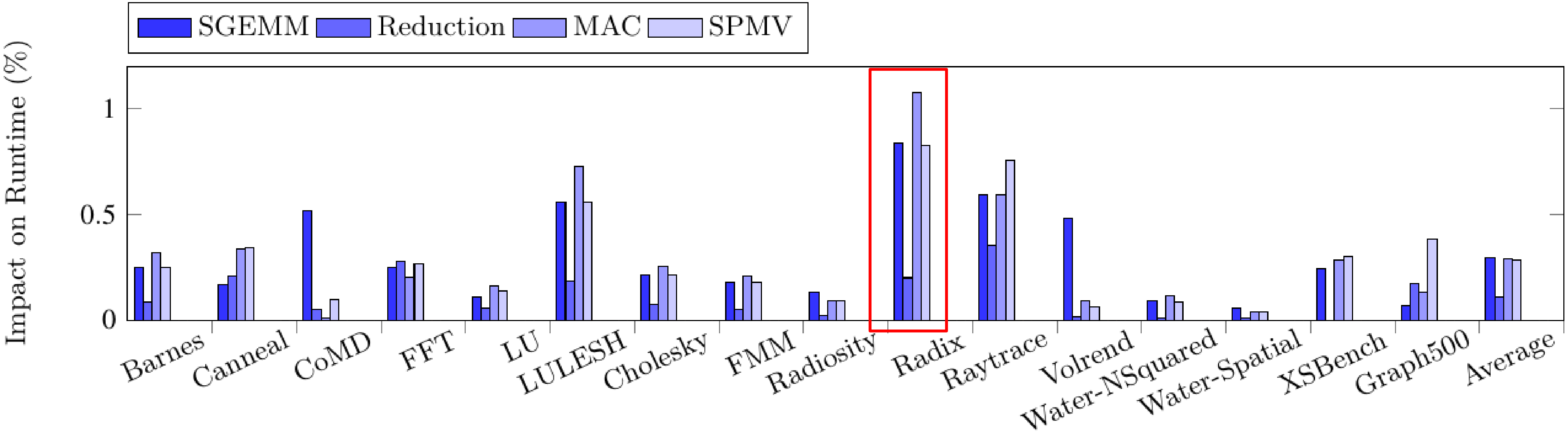

- Performance impact varies based on NoC utilization

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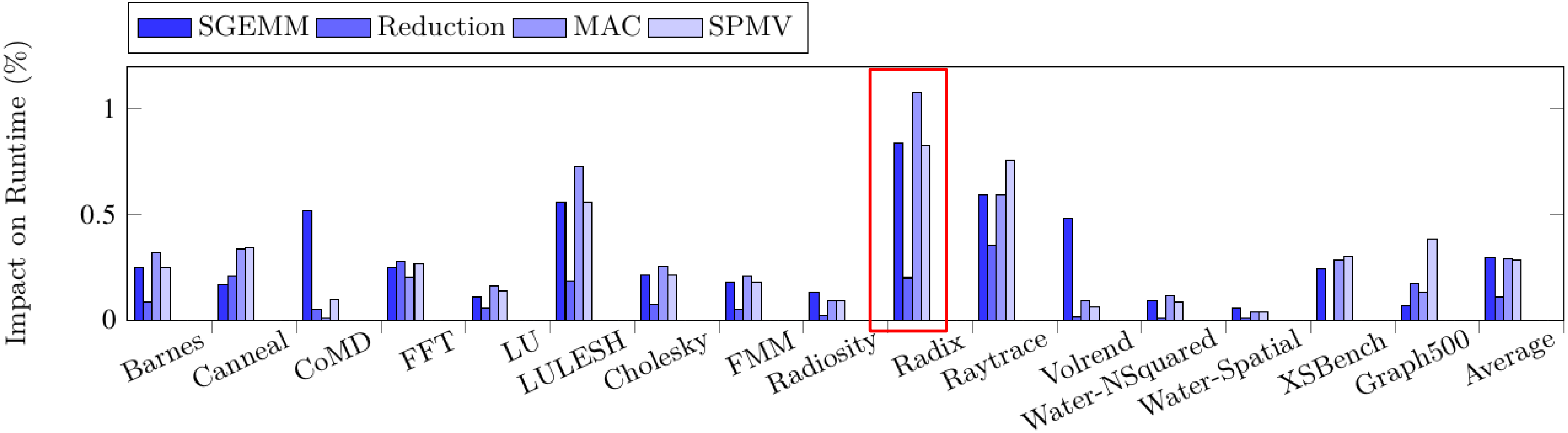

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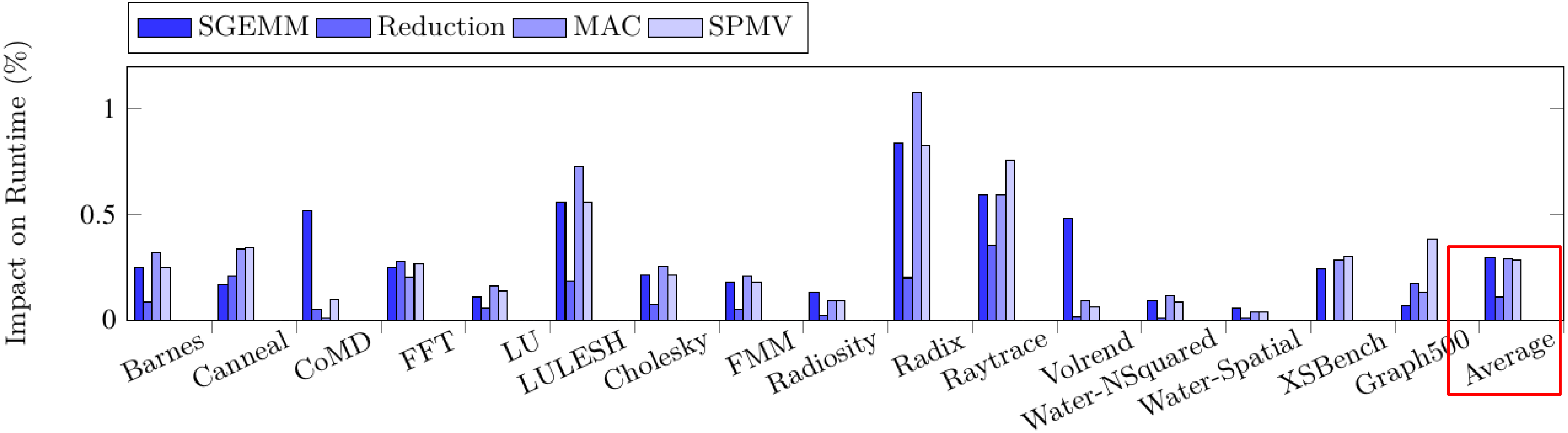

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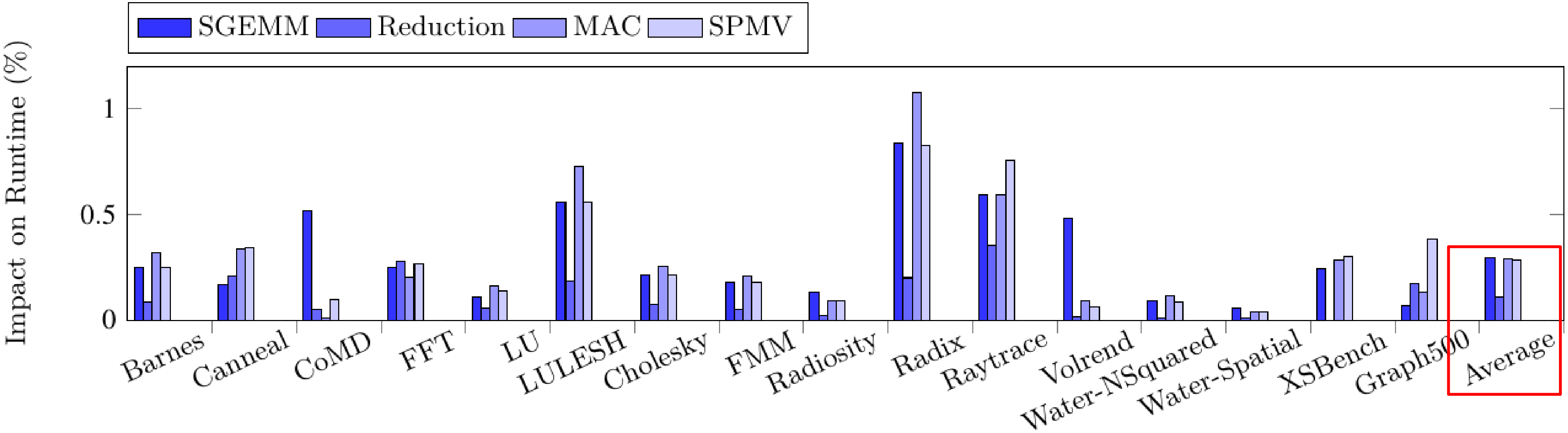

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- SnackNoC kernel completion time impacted at most 3.9% with fair arbitration

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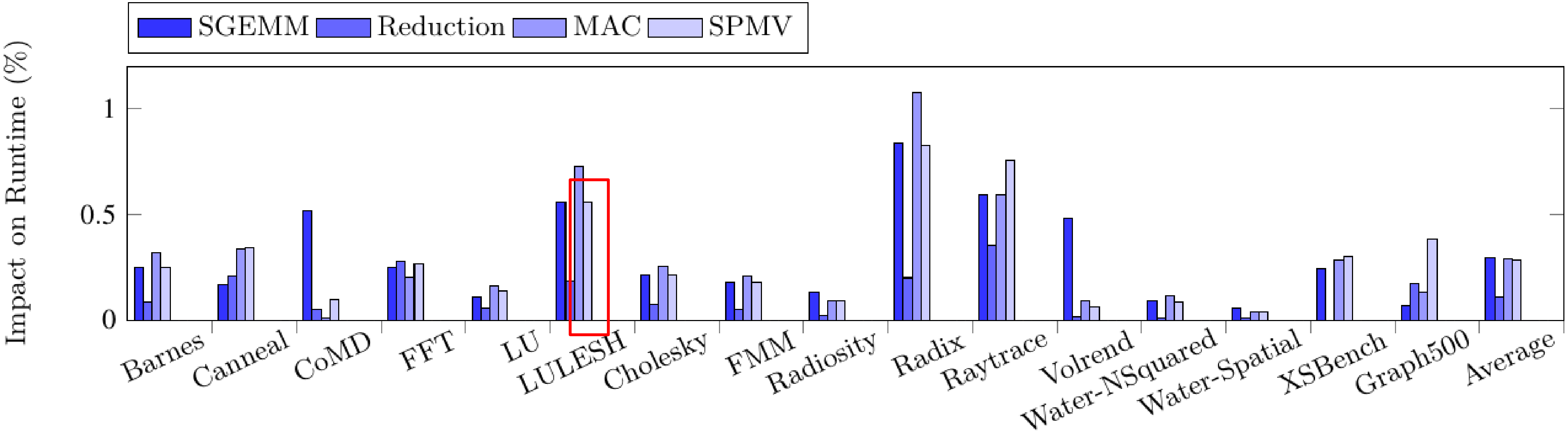

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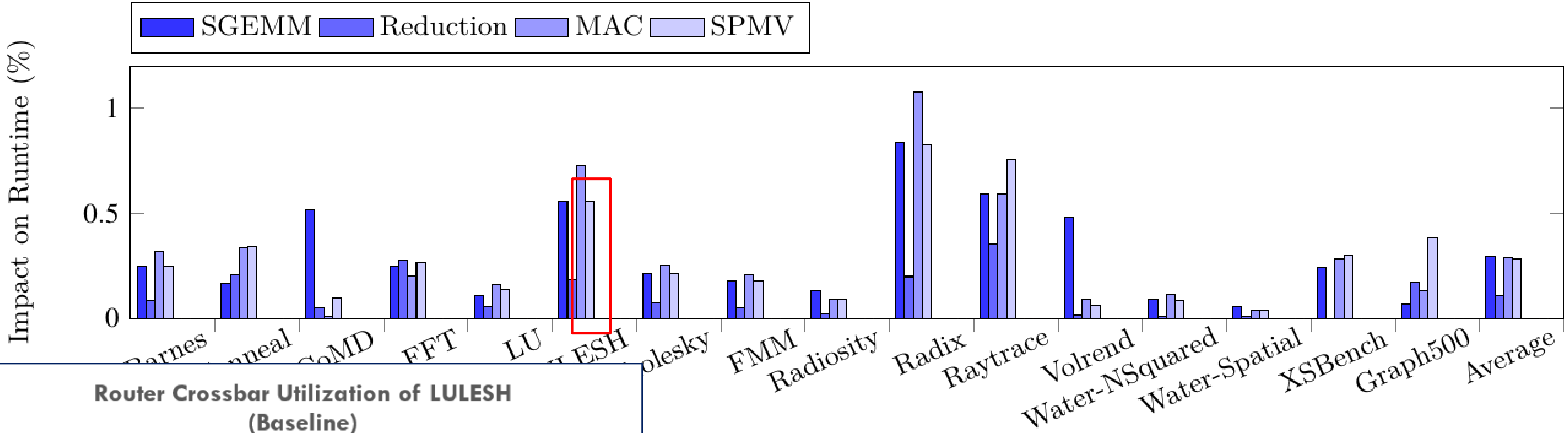

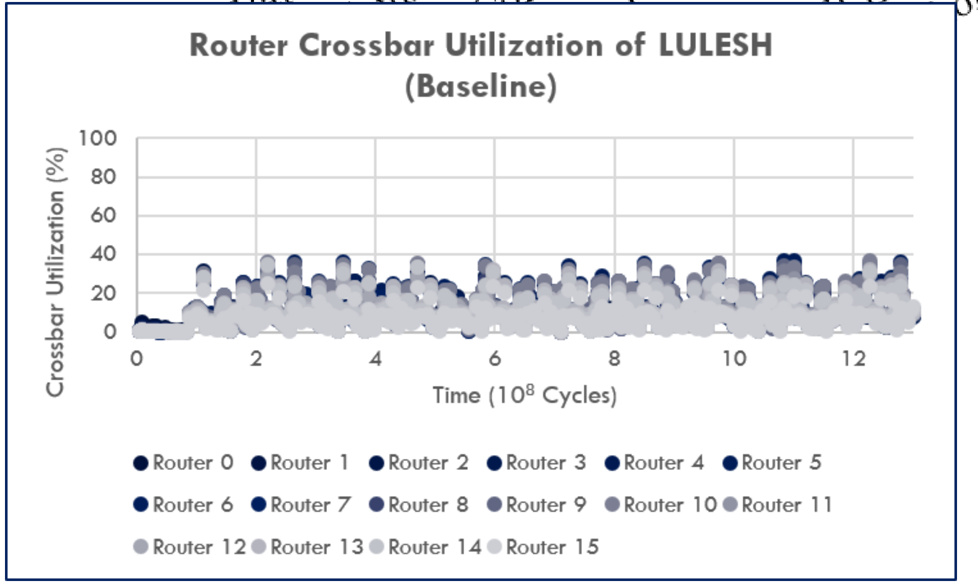

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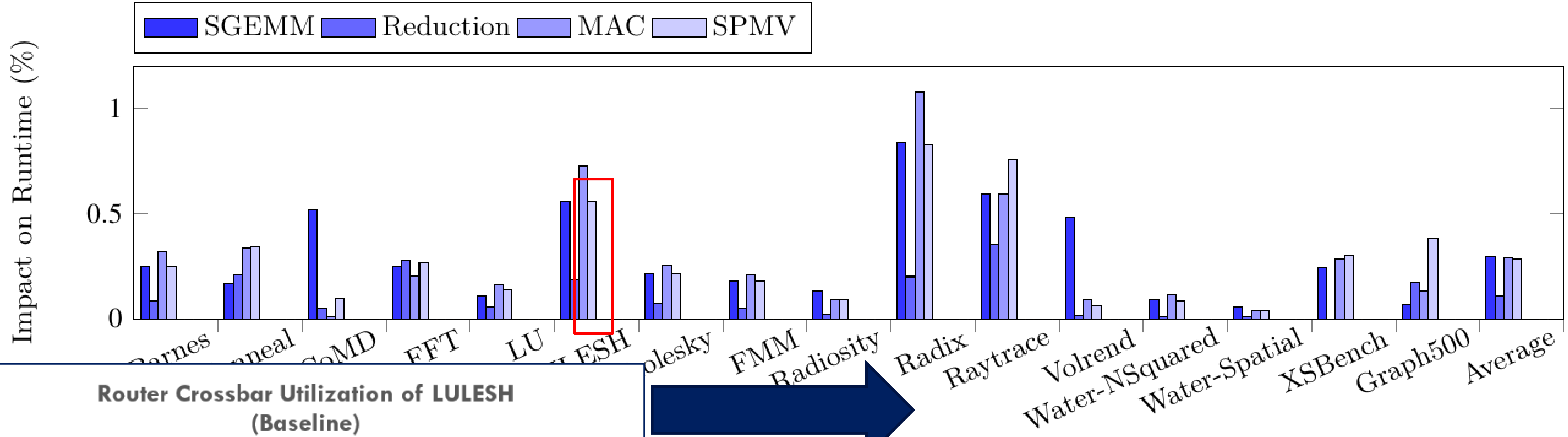

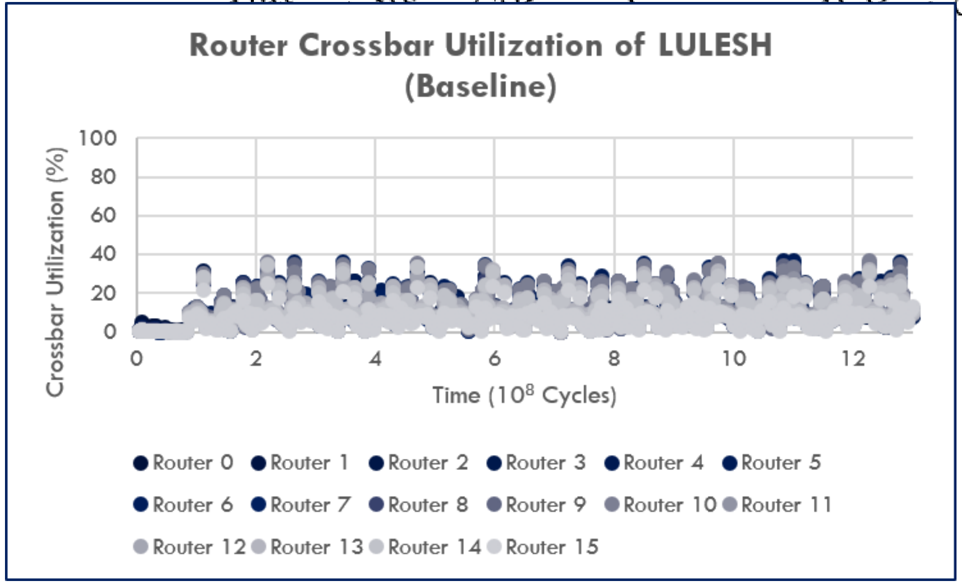

SnackNoC traffic added to LULESH

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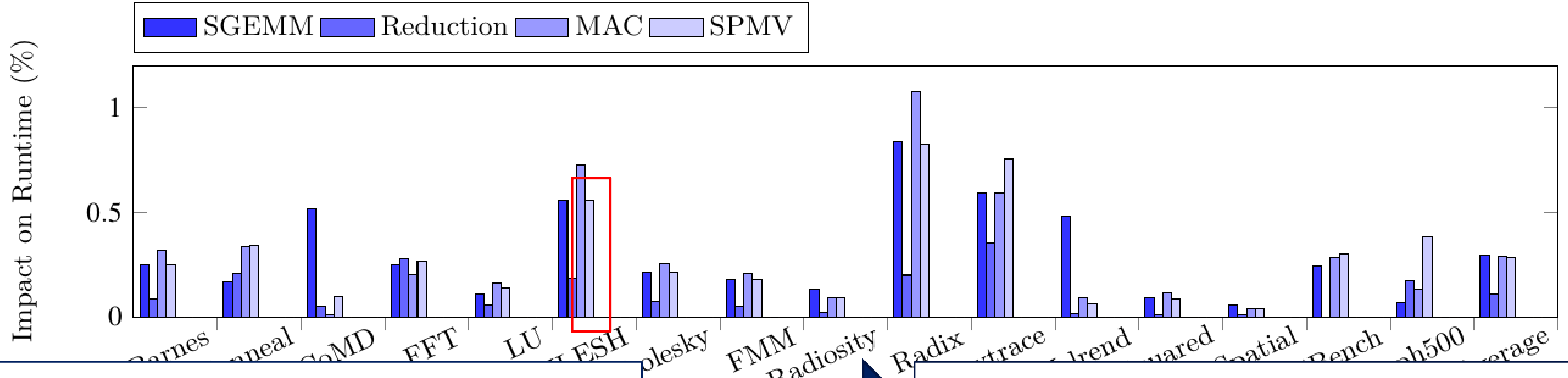

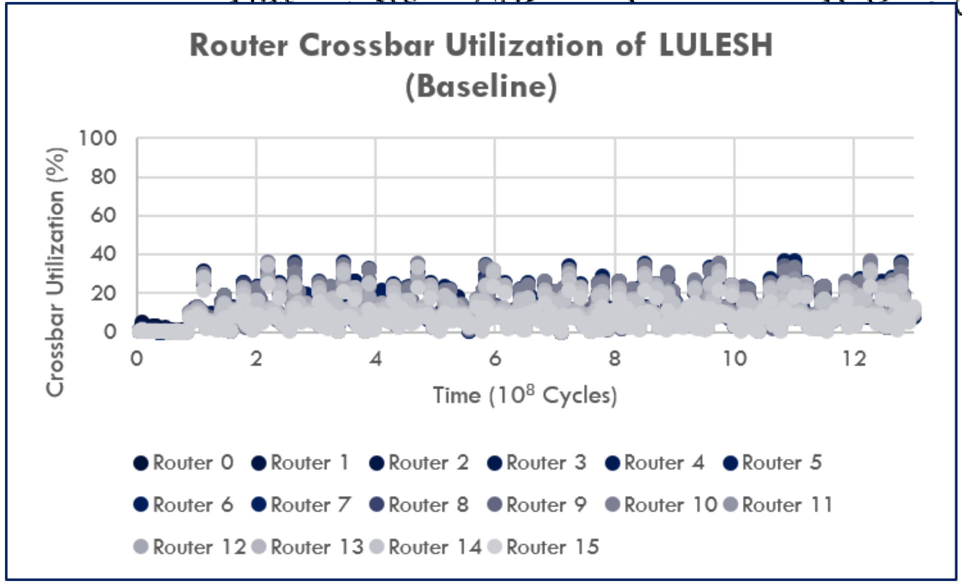

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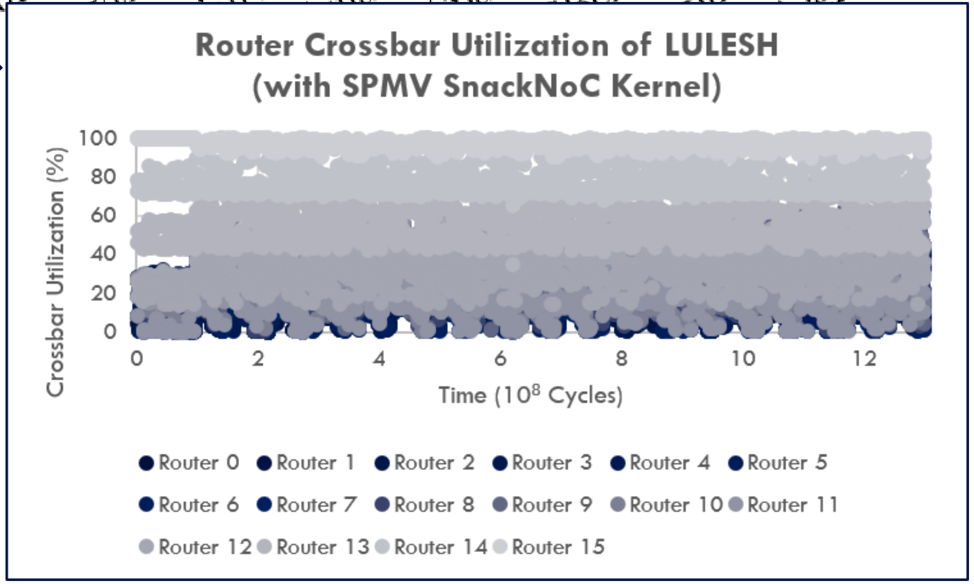
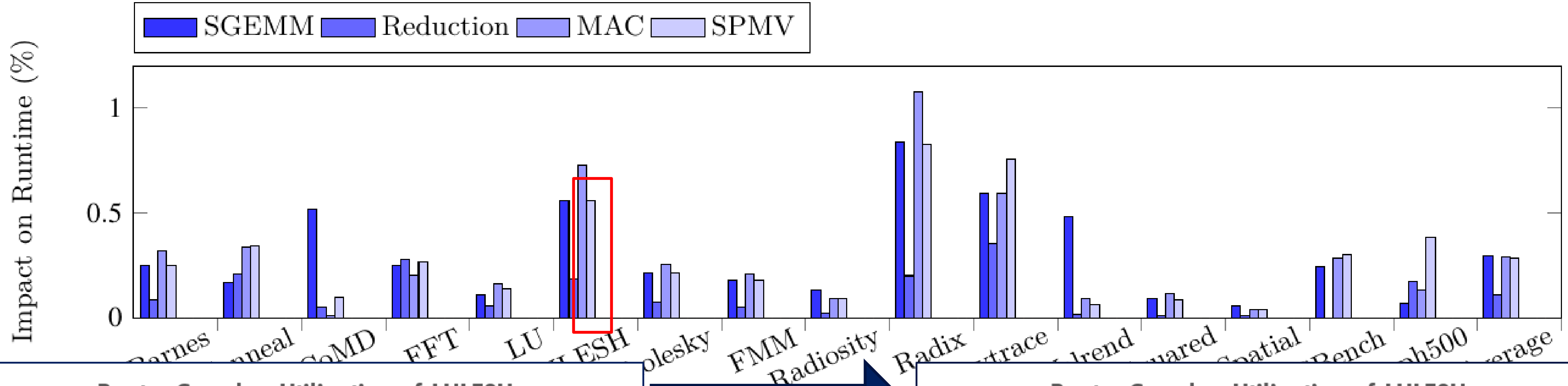
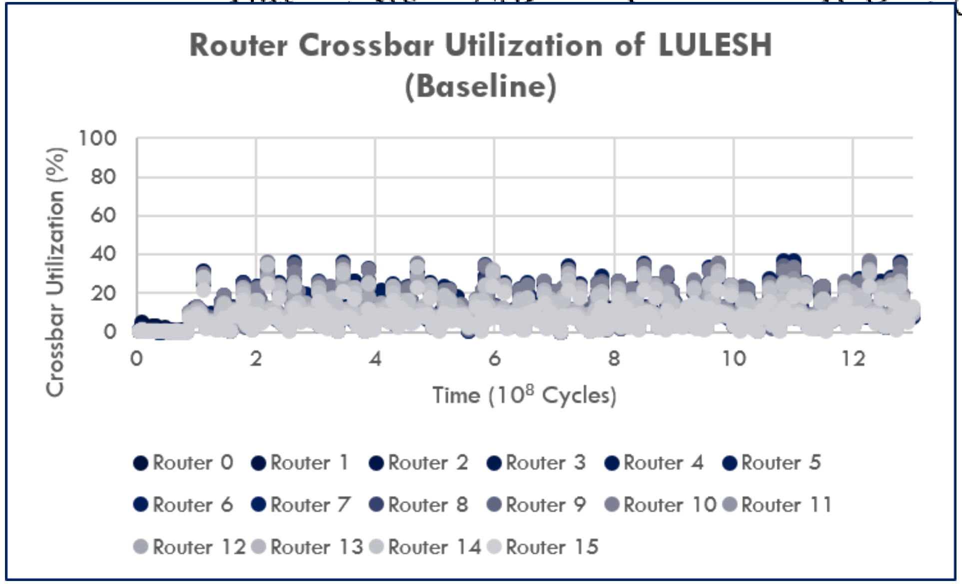


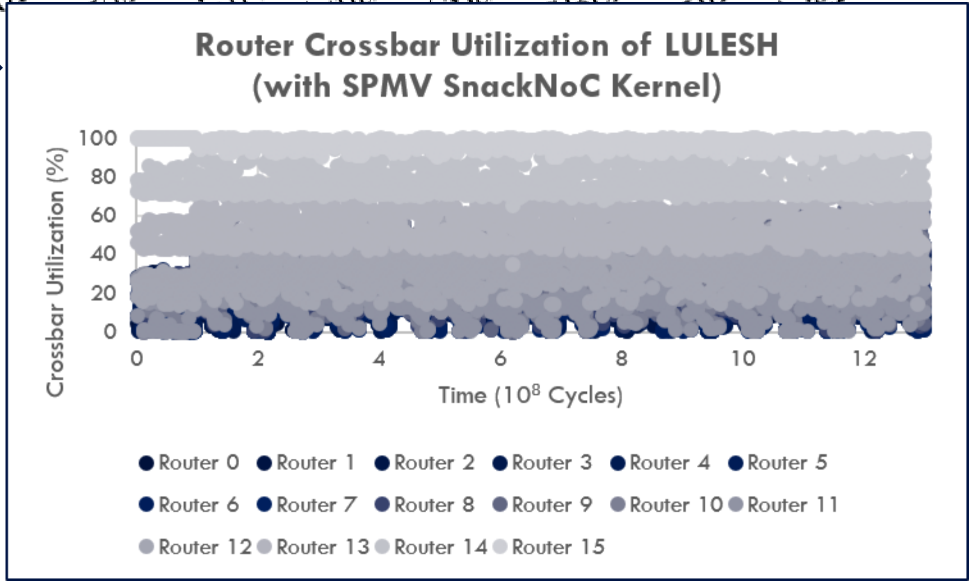
Minimal impact of "Snacking" on CMP performance



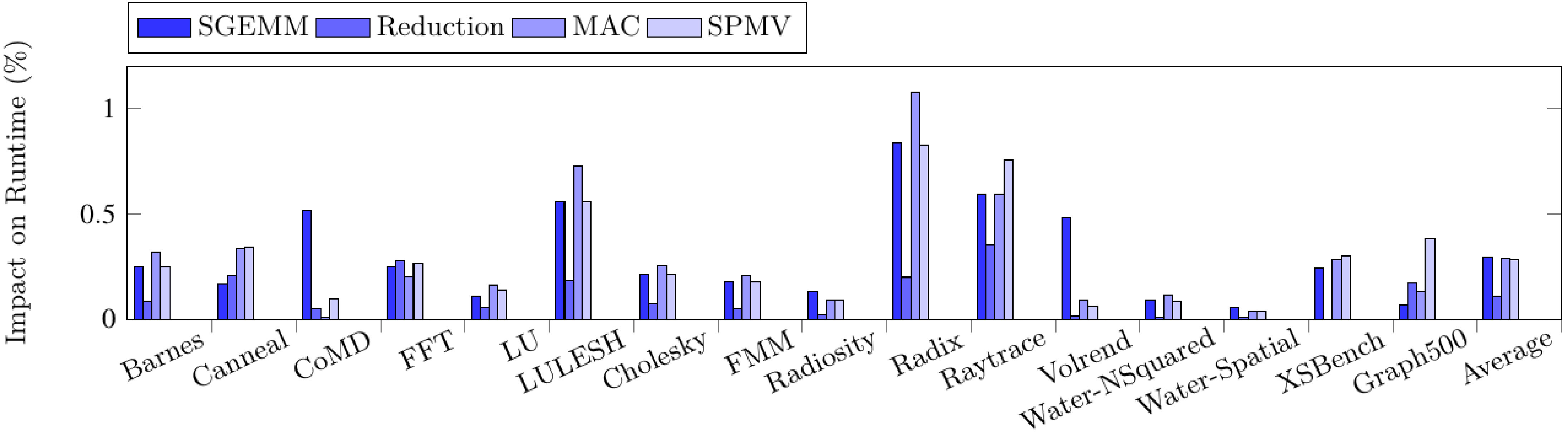


SnackNoC traffic added to LULESH

Minimal impact to CMP Performance



Further Reducing Impact with Priority Arbitration



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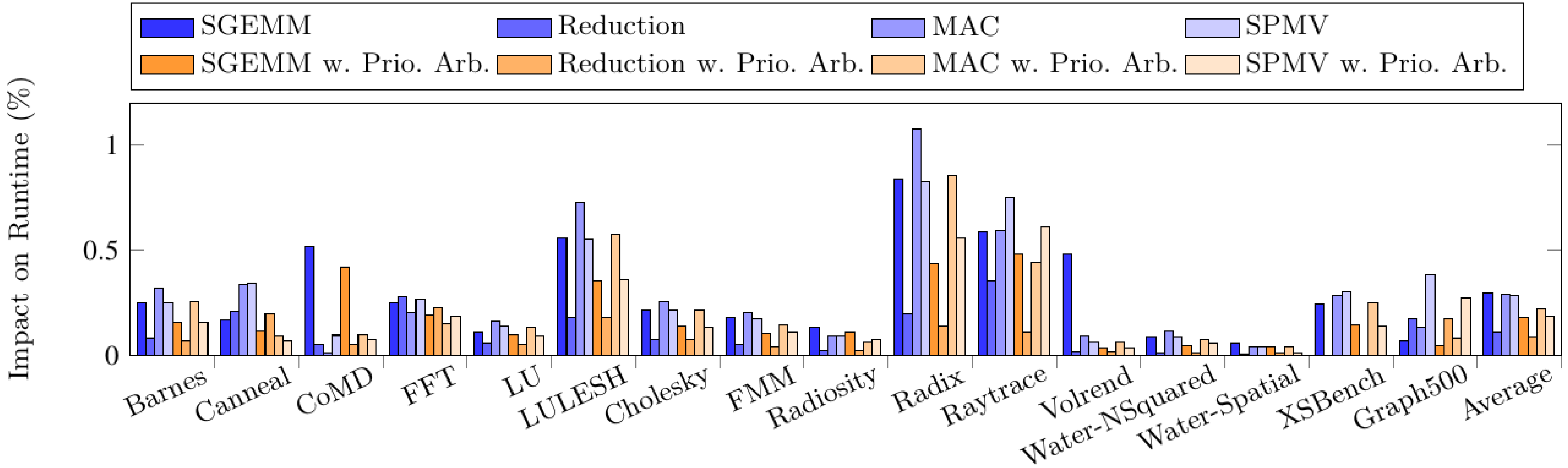

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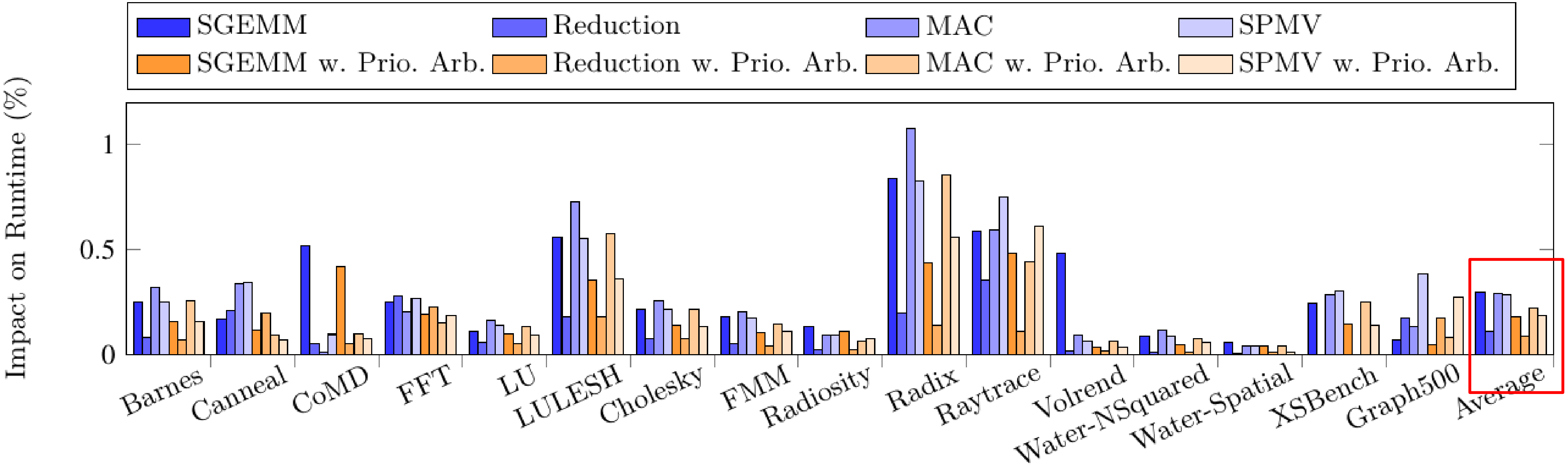

- Adding priority flit arbitration for CMP traffic:
  - Average performance impact drops from 0.25% to 0.17%

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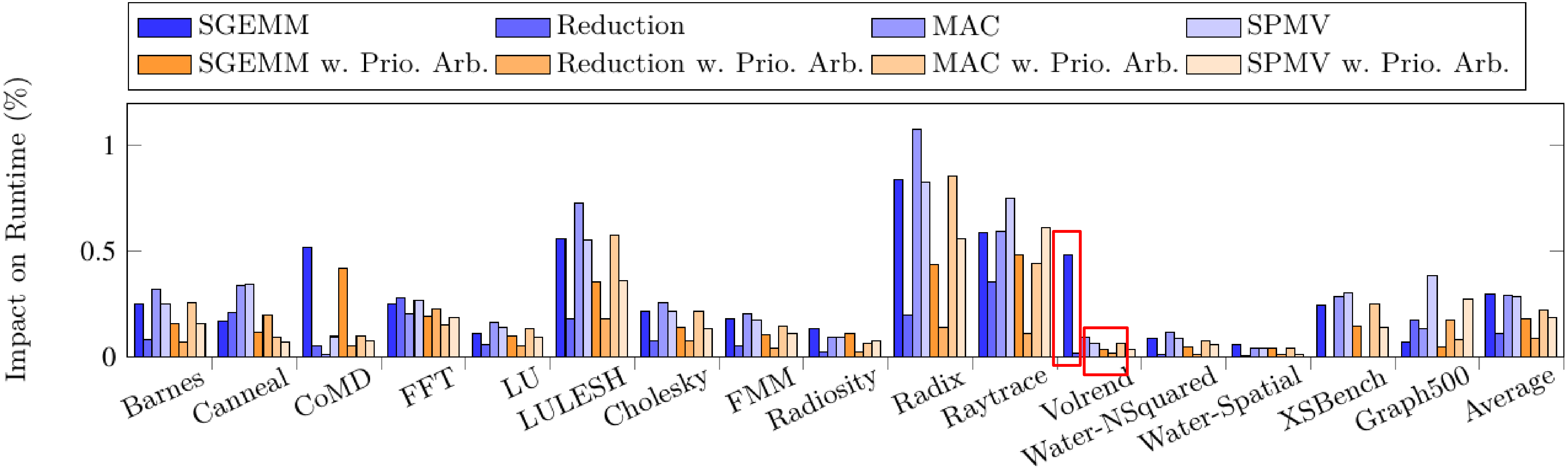

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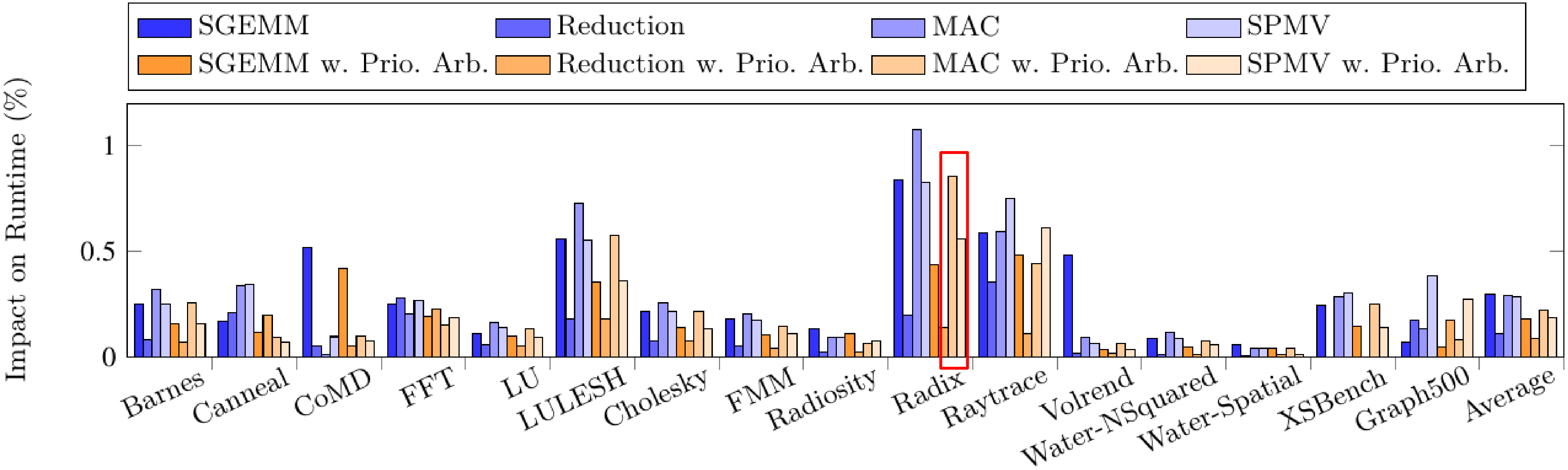
Further Reducing Impact with Priority Arbitration



- Adding priority flit arbitration for CMP traffic:
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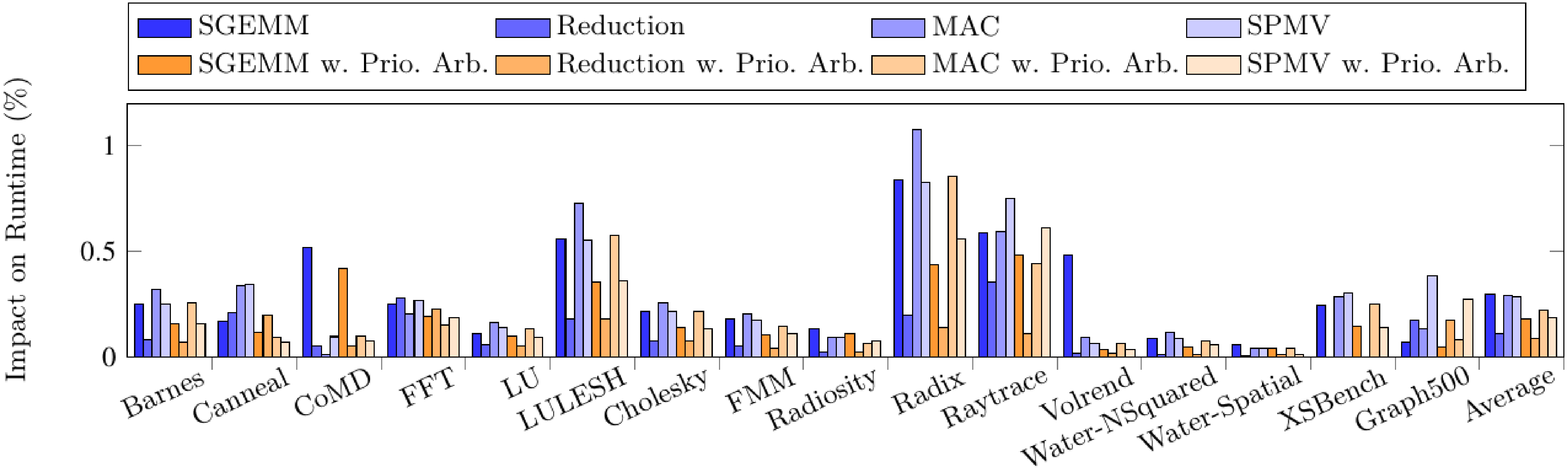
  - Peak performance impact with priority arbitration is 0.83%

Further Reducing Impact with Priority Arbitration



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Satisfies goal of limited performance impact

Overview

- “Slack” of the Communication Fabric
- The SnackNoC Platform
- Experimental Results
- **Conclusion and Future Considerations**

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- Further tradeoffs we're investigating:
  1. Growing application coverage
  2. Scaling compute density
  3. Supporting future topologies

Questions?

Main Contributions:

- Quantified design slack in the communication fabric
- Opportunistically adds 2 to 6 core performance to the CMP by repurposing NoC resources with low overhead

Karthik Sangaiah, Michael Lui, Ragh Kuttappa, Baris Taskin [Drexel University], and Mark Hempstead [Tufts University], "SnackNoC: Processing in the Communication Layer", Proceedings of the IEEE international Symposium on High Performance Computer Architecture (HPCA), February 2020.

http://vlsi.ece.drexel.edu/ & https://sites.tufts.edu/tcal/