Scott P. Lerner

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EDUCATION

- **Ph.D., Electrical Engineering**, GPA: 4.0, (expected graduation mid 2019).
  Drexel University, Philadelphia, PA.
- **B.S., Electrical Engineering**, GPA: 3.5, 2014.
  Drexel University, Philadelphia, PA.
- **B.S., Computer Engineering**, GPA: 3.5, 2014.
  Drexel University, Philadelphia, PA.

PROFESSIONAL EXPERIENCE

- **Researcher / Ph.D. Student**, (September 2014 – current)
  VLSI Laboratory, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA, USA

  – Ph.D. student and member of the VLSI lab
  – **NSF GRFP recipient** for research on Hardware resilience
  – Published on linear timing models for clock buffers
  – Studying Low-power circuits using the following techniques:
    – Clock Gating with delay estimates and optimal sizing
    – Low-power, high-performance enabled by low-swing circuits
  – Investigating Physical Design resilience by using Software workload-awareness

- **Low-Power Design Engineering Ph.D. Intern**, (June 2015 – September 2015)
  Advanced Micro Devices
  Austin, TX, USA

  – Responsible for designing Low-Power Clock Tree Synthesis trials for:
    – Clock Mesh Optimization
    – Clock Buffer Optimization
    – Clock Slew Optimization
  – Created Near-Threshold Variation Analysis guidelines for next-generation tapeouts
  – Characterization of novel low-power variation-tolerant flip flop for near-threshold operation

- **Undergraduate Research Assistant – VLSI Laboratory**, (January 2012 – August 2014)
  VLSI Laboratory, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA, USA

  – NSF Research Experience for Undergraduate (REU) grant
  – Clock tree mesh optimization algorithms (500 lines C++)
  – Implemented an advanced algorithm for clock buffer sizing (700 lines C++)
  – Custom VLSI Design, ASIC Design I/II, Network-on-Chip, Computer Architecture courses
    – Cadence: RTL Compiler, Encounter, Virtuoso, Spectre
    – Synopsys: 1) DC for synthesis, 2) ICC for physical design floorplanning, placement, routing, CTS,
    – 3) Primetime for Static Timing Analysis 4) HSPICE for simulation
    – BookSim, HNoC for Network-on-Chip simulation
  – Senior Design Project on Wireless Interconnect Design for 2D and 3D ICs
    – NoC simulation, HFSS modeling, RF and Antenna modeling

◇ **Undergraduate Research Assistant – DPAC Laboratory**, (January 2012 – August 2014)
DPAC Laboratory, Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA, USA
– Validated binary instrumentation error compared to full-system simulation
– Network-on-Chip design space exploration of resource optimization
– Automated verification testing for CPU event traces

◇ **DRAM Product Engineer**, (March 2011 – September 2011)
Micron Technologies Inc.
Boise, ID, USA
– Performed functional testing and verification on packaged and bare memory die
– Diagnosed part failures for physical design and signal integrity issues
– Worked with a team to brainstorm and apply innovative fixes to new products

CONFERENCES

◇ S. Lerner, B.Taskin, *Slew Merging Region Propagation for Bounded Clock Tree Synthesis*, in review for Transactions on Very Large Scale Integration Systems (TVLSI) 2018.

◇ S. Lerner, I. Yilmaz, B.Taskin, *Custard: ASIC Workload-Aware Reliable Design for Multi-core IoT Processors*, in review for Transactions on Very Large Scale Integration Systems (TVLSI) 2018.

◇ S. Lerner, V. Pano, B.Taskin, *NoC Router Lifetime Improvement using Per-Port Router Utilization*, Proceedings of the International Symposium on Circuit and Systems (ISCAS) 2018.

◇ V. Pano, S. Lerner, B.Taskin, *Workload-Aware Routing (WAR) for Network-on-Chip Lifetime Improvement*, Proceedings of the International Symposium on Circuit and Systems (ISCAS) 2018.

◇ R.Kuttappa, L. Fillipini, S. Lerner, and B.Taskin, *Stability of Rotary Traveling Wave Oscillators under Process Variations and NBTI*, Proceedings of the International Symposium on Circuits and Systems (ISCAS), May 2017.

◇ S. Lerner, B.Taskin, *WT-CTS: Incremental Delay Balancing Using Parallel Wiring Type for CTS*, Proceedings of the International Symposium on VLSI (ISVLSI), Jul. 2017.

◇ S. Lerner, E. Leggett, and B.Taskin, *Slew-Down: Analysis of Slew Relaxation for Low-Impact Clock Buffers*, Proceedings of the System Level Interconnect Prediction (SLIP) 2017.

◇ S. Lerner, B.Taskin, *Workload-Aware ASIC Flow for Lifetime Improvement of Multi-core IoT Processors*, Proceedings of the International Symposium on Quality Electronic Design, Mar. 2017.

◇ S. Nilakantan, S. Lerner, M. Hempstead and B. Taskin, *Can you trust your memory trace?: A comparison of memory traces from binary instrumentation and simulation*, Nominated for best paper at the IEEE International Conference VLSID, pp.135-140 Jan. 2015.

◇ C. Sitik, S. Lerner and B. Taskin, *Timing Characterization of Clock Buffers for Clock Tree Synthesis*, Proceedings of the IEEE International Conference on Computer Design (ICCD), pp.230-236 Oct. 2014.

SELECTED PRESENTATIONS

◇ S. Lerner, V. Pano, B.Taskin, *NoC Router Lifetime Improvement using Per-Port Router Utilization*, Awarded **1st Place** at the 10th Annual Drexel IEEE Research Symposium 2018.

◇ S. Lerner, B.Taskin, *WT-CTS: Incremental Delay Balancing Using Parallel Wiring Type for CTS*, Presented at the IEEE International Symposium on VLSI, Jul. 2017.

◇ S. Lerner, B.Taskin, *Workload-Aware ASIC Flow for Lifetime Improvement of Multi-core IoT Processors*, Presented at the IEEE International Symposium on Quality Electronic Design, Mar. 2017.

◇ S. Lerner, E. Leggett, and B.Taskin, *Slew-Down: Analysis of Slew Relaxation for Low-Impact Clock Buffers*, Presented at the IEEE System Level Interconnect Prediction 2017.

◇ S. Lerner, B. Taskin *Enhancements in Low Voltage and High Performance Clock Distribution Networks*, Poster presented at SRC Innovation and Intelligent Internet of Things, Nov. 2016.

◇ S. Lerner, B. Taskin *Workload-Aware EDA*, Presentation at IEEE CE Graduate Symposium, Feb. 2016.

PROFESSIONAL ACTIVITIES

- External Reviewer - Journal of Circuits, Systems, and Computers 2018
- External Reviewer - Design Automation Conference 2018
- Technical Chair - Drexel IEEE Graduate 2014-Current
- Member - Drexel IEEE Undergraduate 2013-2014
- Student Member - Institute of Electrical and Electronics Engineers 2010-Current

VOLUNTEER ACTIVITIES

- Fellowship Ambassador, Drexel University 2016-Current
- STAR Mentor - CTS Analysis GUI, Drexel University 2017
- STAR Mentor - High-Frequency CTS, Drexel University 2016
- STAR Mentor - Internal Node Relaxation for CTS, Drexel University 2016
- Lead Organizer - DragonHacks (500+ in attendance) 2015, 2016, 2017
- STAR Mentor - Low-power Circuit Design, Drexel University 2013-14
- Freshman Design Mentor - Wireless HDMI, Drexel University 2013-14
- TechGirlz Workshop held in Philadelphia, PA
- SeaPerch Underwater Robotics Challenge 2014 held in Philadelphia, PA
- Biomedical Sciences and Professional Studies Graduate Orientation 2014 held in Philadelphia, PA
- City Year Park Cleanup in Philadelphia, PA

SKILLS

- C, C++, Python, Perl, Matlab, Objective-C (10,000+ lines written)
- Pthread, OpenMP, Tcl, Assembly (MIPS), SystemC (1,000+ lines written)
- Verilog HDL, Arduino, LaTeX (1,000+ lines written)
- Synopsys – Design Compiler, IC Compiler, HSpice
  Cadence – RTL Compiler, Encounter, Virtuoso Suite, Spectre, PSpice
- vi, Office Suites
- Unix, Linux, Windows, DOS

ACADEMIC HONORS AND AWARDS

- Weggel Family Fellowship, 2018
- Frank and Agnes Seaman Endowed Fellowship, 2016
- **NSF Graduate Research Fellowship (GRFP) Program Recipient, 2015.**
- National Defense Science & Engineering Graduate (NDSEG) Recipient **(declined)**, 2015.
- Nihat Bilgutay Award, 2015
- TCVLSI Travel Award, 2015, 2016
- NSF Research Experience for Undergraduate (REU) Grant 2014
- A. Richard Newton Young Fellow Award 2014, 2015, 2016, 2017
- Dean's Choice Award at Philly Codefest for MotionExplorer 2014 held in Philadelphia, PA.
- NextFab Innovation Award at Philly Codefest for MotionExplorer 2014 held in Philadelphia, PA.
- Doctor Thomas Moore Endowed Grant 2014
- Dean's List, 2009, 2010, 2011, 2012, 2013, 2014.

REFERENCES

- **Dr. Baris Taskin**
  Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  E-mail: taskin@coe.drexel.edu
- **Dr. Mark Hempstead**
  Associate Professor, Department of Electrical and Computer Engineering
  Tufts University, Medford, MA
  E-mail: mark.hempstead@tufts.edu