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RESEARCH INTERESTS

My research interests span the areas of circuits and systems, computer architecture, cross-layer techniques, and emerging computing systems. I have specific interests in workload-awareness, machine learning, multi-core architectures, and internet-of-things.

EDUCATION

Drexel University — Philadelphia, PA
Ph. D. in Computer Engineering — *2014-, Expected mid-2019*
Dissertation Title: "Workload-Awareness for Multi-core Processors"
Advisor: Prof. Baris Taskin
National Science Foundation Graduate Research Fellowship Program (**GRFP**) 2015-2018
National Defense Science & Engineering Graduate (**NDSEG**) 2015
Advanced Micro Devices — Ph.D. Intern Low-Power Design Engineer

Drexel University — Philadelphia, PA
B. S. in Electrical Engineering — *June 2014*
B. S. in Computer Engineering — *June 2014*
National Science Foundation Research Experience for Undergraduate (**REU**) 2014
Two publications
Lockheed Martin — Spectrum Denial Engineer
Micron Technologies, Inc. — DRAM Product Engineer
Software Support-PMW — App Software Developer

PUBLICATIONS

JOURNALS

1. S. Lerner and B.Taskin, "Slew Merging Region Propagation for Bounded Slew and Skew Clock Tree Synthesis", in *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*, 2018.
doi: 10.1109/TVLSI.2018.2874572
2. S. Lerner, I. Yilmaz, and B.Taskin, "Custard: ASIC Workload-Aware Reliable Design for Multi-core IoT Processors", in *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*, 2018.
doi: 10.1109/TVLSI.2018.2878664
3. S. Lerner, and B.Taskin, "Workload-Aware ASIC Design Considering Lithography Information", in preparation for submission, 2019.

PAPERS

4. S. Lerner and B.Taskin, "Towards Design Decisions for Genetic Algorithms in Clock Tree Synthesis", Proceedings of the *IEEE International Green and Sustainable Computing (IGSC) Conference*, Oct. 2018.
5. S. Lerner, V. Pano, and B.Taskin, "NoC Router Lifetime Improvement using Per-Port Router Utilization", Proceedings of the *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018.
6. V. Pano, S. Lerner, and B.Taskin, "Workload-Aware Routing (WAR) for Network-on-Chip Lifetime Improvement", Proceedings of the *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018.
7. R.Kuttappa, L. Fillipini, S. Lerner, and B.Taskin, "Stability of Rotary Traveling Wave Oscillators under Process Variations and NBTI", Proceedings of the *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2017.

8. S. Lerner and B.Taskin, "WT-CTS: Incremental Delay Balancing Using Parallel Wiring Type for CTS", Proceedings of the *International Symposium on VLSI (ISVLSI)*, Jul. 2017.
9. S. Lerner, E. Leggett, and B.Taskin, "Slew-Down: Analysis of Slew Relaxation for Low-Impact Clock Buffers", Proceedings of the *System Level Interconnect Prediction (SLIP)*, Jun. 2017.
10. S. Lerner and B.Taskin, "Workload-Aware ASIC Flow for Lifetime Improvement of Multi-core IoT Processors", Proceedings of the *International Symposium on Quality Electronic Design (ISQED)*, Mar. 2017.
11. S. Nilakantan, S. Lerner, M. Hempstead, and B. Taskin, "Can you trust your memory trace?: A comparison of memory traces from binary instrumentation and simulation", **Nominated for best paper** at the *IEEE International Conference on VLSI Design (VLSID)*, Jan. 2015.
12. C. Sitik, S. Lerner, and B. Taskin, "Timing Characterization of Clock Buffers for Clock Tree Synthesis", Proceedings of the *IEEE International Conference on Computer Design (ICCD)*, Oct. 2014.

WORK EXPERIENCE

- **Ph.D. Intern Low-Power Design Engineer, Advanced Micro Devices,** Jun 2015 - Sep 2015. Part of a team of three that investigated the impacts of low-power techniques on the Zen microarchitecture. Designed and optimized strategies for pulsed latches, near-threshold logic, and clock network structure.
- **Spectrum Denial Engineer, Lockheed Martin**, Apr 2013 - Sep 2013. Optimized software defined radios for spectrum denial capabilities. Analyzed detection strategies and implemented counterattack measures.
- **App Software Developer, Software Support-PMW**, Jan 2012 - Sep 2012. Part of a team of four to design and update iOS and Android applications for point-of-sale businesses. Engaged in proactive design meetings with customers to further improve operation.
- **DRAM Product Engineer, Micron Technologies, Inc.**, Mar 2011 - Sep 2011. Responsible for the identification of hardware failures from physical design and signal integrity issues post-manufacturing. Worked with a team to brainstorm and apply innovative fixes to future products.

RESEARCH EXPERIENCE

- **Research Assistant, Drexel University**, Sep 2014 - Present.
  Workload-Aware Multicore Processors, (Dec 2016 - Present): We pose the question of whether multi-threaded applications use multi-core processor cores evenly, and show the issues associated with current state-of-the-art. I was the first to design a framework that can analyze large, multi-core designs quickly. The framework is then extended to include analysis of reliability, timing, and power. This research demonstrates that when future systems become heterogeneous, current analysis frameworks are inadequate.

  Machine Learning for Electronic Design Automation, (Jan 2017 - Present): Optimizing even one aspect of a design takes a long time due to scale and designer input. However, using straightforward heuristic-based analysis, machine learning models can be created to speed up design. This research is aligned with DARPA's I.D.E.A. program to perform design synthesis in 24-hours. I created two models for clock tree synthesis using convolutional neural networks and genetic algorithms. This research shows how effective current machine learning algorithms are and illustrates the need for improvement in future designs.

  Design Optimization for Clock Tree Synthesis, (Sep 2014 - Present): We propose that, due to technology scaling, next-generation designs will require a multi-optimization algorithm to satisfy the clock timing constraints of slew and skew. In the course of our work on clock tree synthesis, we described a new quality metric for balancing the multiple objectives. This was used to analyze a number of synthesis techniques, especially those for advanced technologies and reduced voltage.
- **Research Intern, Advanced Micro Devices, Austin, TX**, June - Sep. 2015.
  Low-Power Clock Tree Synthesis: Our work involved designing and analyzing practical solutions for reducing power on high-performance processors. Four techniques were investigated and proposed. Clock tree synthesis power optimization techniques like buffer sizing and placement were demonstrated. Pulsed latches were designed and implemented, but were not selected due to tapeout schedule. Near-threshold logic gates were created, but concerns over large variation restricted their use. Multi-Vt optimization showed great potential, but were not implemented due to manufacturing limitations.
- **VLSI Lab Undergraduate Research Intern, Drexel University**, Jan 2012 - Aug 2014.
  Clock Mesh Optimization, (Jan 2012 - Mar 2012): Developed an unsupervised learning algorithm to optimize clock mesh spine placement, under Prof. Baris Taskin.

Clock Buffer Optimization, (Mar 2012 - Sep 2012): Implemented a greedy optimization algorithm to mitigate timing violations post-CTS, under Prof. Baris Taskin.
Timing Characterization Buffer Models, (Sep 2012 - Aug 2013): Implemented a greedy optimization algorithm to mitigate timing violations post-CTS, under Prof. Baris Taskin.
Wireless Interconnect Design for 2D and 3D ICs, (Aug 2013 - Aug 2014): Our research on wireless interconnects was an extension of our senior design project, under Prof. Baris Taskin, to design a network-on-chip with antennas for communication.

- **DPAC Lab Undergraduate Research Intern, Drexel University**, Jan 2012 - Aug 2014.
  Binary Instrumentation Research: Validated binary instrumentation error compared to full-system simulation and performed resource optimization for network-on-chip design space exploration, under Prof. Mark Hempstead.

ACADEMIC HONORS

- IGSC Best Presentation Nominee, 2018
- IGSC Travel Award, 2018
- Weggel Family Fellowship, 2018
- Frank and Agnes Seaman Endowed Fellowship, 2016
- **NSF Graduate Research Fellowship (GRFP) Program Recipient, 2015-2018.**
- National Defense Science & Engineering Graduate (NDSEG) Recipient (declined), 2015.
- Nihat Bilgutay Award, 2015
- TCVLSI Travel Award, 2015, 2016
- NSF Research Experience for Undergraduate (REU) Grant, 2014
- A. Richard Newton Young Fellow Award, 2014, 2015, 2016, 2017, 2018
- Dean's Choice Award at Philly Codefest for MotionExplorer, held in Philadelphia, PA, 2014
- NextFab Innovation Award at Philly Codefest for MotionExplorer, held in Philadelphia, PA, 2014
- Doctor Thomas Moore Endowed Grant, 2014
- Dean's List, 2009-2014

TEACHING EXPERIENCE

- **Teaching Assistant (TA).** ECE Lab, Prof. Christopher Peters, Senior Level, Fall 2018, Drexel University.
  - Designed labs and objectives for a new ECE lab class.
- **TA.** Digital Systems Projects, Prof. Prawat Nagvajara, Junior Level, Fall 2018, Drexel University.
- **TA.** Advanced Programming, Prof. James Shackleford, Junior Level, Fall 2018, Drexel University.
- **TA.** Advanced Programming, Prof. Kurt Schmidt, Junior Level, Winter 2014, Drexel University.
- **TA.** Embedded Systems, Prof. Karkal Prabhu, Junior Level, Fall 2014, Drexel University.
- **TA.** Introduction to Computer Networks, Prof. Karkal Prabhu, Junior Level, Fall 2014, Drexel University.
- **TA.** Design with Microcontrollers, Prof. Prawat Nagvajara, Junior Level, Summer 2014, Drexel University.
- **TA.** ASIC Design II, Prof. Baris Taskin, Graduate Level, Spring 2013, Drexel University.

TALKS

CONFERENCE TALKS

1. "Towards Design Decisions for Genetic Algorithms in Clock Tree Synthesis", *International Green and Sustainable Computing Conference*, Pittsburgh, PA, October 2018.
2. "NoC Router Lifetime Improvement using Per-Port Router Utilization", *International Symposium on Circuit and Systems*, Florence, Italy, May 2018.
3. "Workload-Aware Routing (WAR) for Network-on-Chip Lifetime Improvement", *International Symposium on Circuit and Systems*, Florence, Italy, May 2018.
4. "WT-CTS: Incremental Delay Balancing Using Parallel Wiring Type for CTS", *International Symposium on VLSI*, Bochum, Germany, July 2017.

5. "Slew-Down: Analysis of Slew Relaxation for Low-Impact Clock Buffers", *System Level Interconnect Prediction*, Austin, Texas, June 2017.
6. "Workload-Aware ASIC Flow for Lifetime Improvement of Multi-core IoT Processors", *International Symposium on Quality Electronic Design*, Santa Clara, California, March 2017.
7. "Timing Characterization of Clock Buffers for Clock Tree Synthesis", *IEEE International Conference on Computer Design*, Seoul, South Korea, October 2014.

INDUSTRY/OTHER TALKS

8. "Enhancements in Low Voltage and High Performance Clock Distibution Networks", SRC Innovation and Intelligent Internet of Things, Dallas, Texas, Nov. 2016.

PROFESSIONAL ACTIVITIES

- Session Chair, International Green and Sustainable Computing Conference, Pittsburgh, PA, 2018
- Technical Chair, Drexel IEEE Graduate - 2014-Current
- Member, Drexel IEEE Undergraduate Chapter - 2013-2014
- Student Member, Institute of Electrical and Electronics Engineers - 2010-Current

SERVICE

- Reviewer (Journals) - *IEEE Transactions on Very Large Scale Integration, IEEE Transactions on Computer Aided Design, World Scientific Journal of Circuits, Systems, and Computers, Elsevier Journal on Integration, EAI Transactions on Industrial Networks and Intelligent Systems.*
- Reviewer (Conferences) - *IEEE/ACM Design Automation Conference 2017, 2018*

REFERENCES[1]

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[1]From Industry available upon request.