Effect of EMI between Wireless Interconnects and Metal Interconnects on CMOS Digital Circuits

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***Abstract*— Wireless interconnects are built with two or more antennas on a semiconductor integrated circuit (IC) communicating with each other to form an intra-chip communication network. The wireless interconnects are considered a viable solution to the global communications problems faced by ICs. In this work, the effects of the electromagnetic coupling between the on-chip antennas for wireless interconnects and the metal interconnects for local communication are considered. The effects of the electromagnetic coupling on the complimentary metal oxide semiconductor (CMOS) digital circuits are presented. The electromagnetic compatibility and electromagnetic interference analysis is performed using a co-simulation methodology. In particular, 3D finite element method (FEM) based full-wave electromagnetic simulations are co-simulated with the radio frequency (RF) models of the devices on a circuit simulator. The presented simulation models are based on a contemporary 9-metal layer 90 nm process technology.**

I. Introduction

The increasing demand for high speed and high performance integrated circuit (IC) systems has been a driving force for increasing the speed and performance of metal oxide semiconductor field effect transistors (MOSFET) devices which constitute the IC. The increase in the speed of the MOSFET devices has primarily been enabled due to reduction in their sizes. However, this reduction in the MOSFET device sizes has been accompanied by a proportional reduction in the cross-sectional area of the metal interconnects used for communication on an IC die as depicted in Figure 1. The increased system complexity, density and die size of a typical planar IC, coupled with the reduction in the cross-sectional area of metal interconnects, have increased the parasitic effects associated with the interconnects. The global metal interconnect lines are now considered as a bottleneck to the increase in IC speed as the delay due to the interconnects is higher than the delay due to the MOSFETs [1].

Certain conventional design approaches used by the semiconductor industry to mitigate this problem include increasing the interconnect width (i.e. reverse scaling of the interconnects) and changing the inter layer dielectrics (ILD) on the die to low κ dielectric materials [1]. However, these design approaches only increase the life time of the global interconnect system by a few technology generations [2]. In contemporary design approaches, 3D integrated circuits (3D ICs) are considered as a viable solution to alleviate the problems posed by the scaling of metal interconnects in planar integrated circuits (ICs). IC die stacking in 3D ICs reduces the length of the interconnects between two communication end-points thereby reducing the interconnect delay [3].

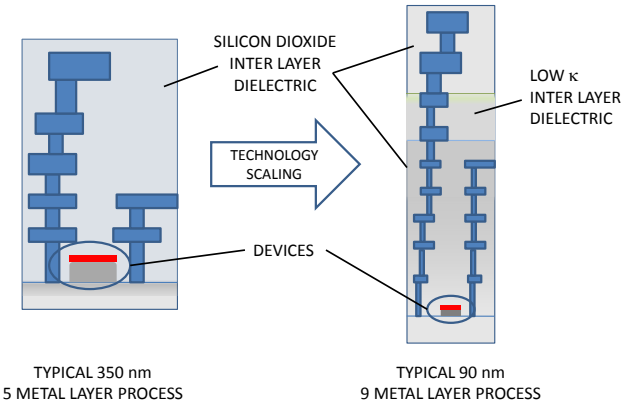


Fig. 1. Depiction of semiconductor technology scaling.

Another possible alternative for a global communication network on a chip is to use radio frequency (RF) interconnects. There are two (2) types of RF IC interconnects of note: The micro-strip transmission line based interconnects operating in the RF range [4] and the wireless communication based intra-chip interconnects operating in the RF range [5]. This paper focuses on the second type, that is, the use of on-chip antennas for the wireless interconnects. The feasibility of establishing an intra-chip wireless communication channel using on-chip antennas for the global delivery of the clock signal has been shown in [5]. In particular, this paper focuses on the electromagnetic compatibility (EMC) of the on-chip antennas with the complimentary metal oxide semiconductor (CMOS) digital circuits for a typical 9-metal layer 90 nm CMOS technology. The electromagnetic compatibility is studied through a co-simulation of full-wave 3D finite element method (FEM) based electromagnetic simulations and circuit simulations. The methodology presented in this work can also be used to investigate the electromagnetic compatibility of the on-chip antennas optimized for RF communication functionalities on radio frequency integrated circuits (RFICs) or system-on-chips (SoCs).

The previous work on the electromagnetic interaction between the on-chip antennas and the CMOS circuit components is outlined in Section II. The methodology and the simulation setup is discussed in Section III and the results of the co-simulations are presented in Section IV.

II. Literature Review

The previous body of work on the electromagnetic interaction (EMI) between the on-chip antennas and the CMOS circuit components can be categorized into three categories in relevance to the work presented in this paper:

1) The effect of the metal interconnects on the antenna characteristics [6, 7],
2) The effect of the electromagnetic radiation from the on-chip antennas on the MOSFET devices [8],
3) The effect of the electromagnetic radiation from the on-chip antennas on the metal interconnects [7, 9, 10].

In [6], it is shown that the presence of metal interconnects placed on the same metal layer as that of the antenna in parallel orientation to the antenna decreases the antenna gain in the lower frequency range and increases it in the mid-band and high frequency ranges. However, the change in the gain is not very large and does not have a major influence on the transmission gain. In other words, the presence of the metal interconnects shifts the response to a higher frequency range. However, the percentage metal utilization of the metal layers considered in [6] is very low and untypical of ICs (the CMOS manufactory processes require a percent metal utilization between 20% and 80%). In [7], it is shown that the transmission gain reduces substantially for higher percentage utilization.

In [8], the effect of the radiation from the antennas of the wireless interconnect system on the MOSFET devices is studied. It is shown in [8] that the effect of the radiation on the leakage current of the MOSFET devices is very low and can be neglected. However, the study in [8] only considers the effect of the EM radiations on the MOSFET device alone and neglects the effects of the electromagnetic interaction with the metal interconnects. The functionality of the CMOS digital circuits can also be effected due to the signal coupling with the metal interconnects.

In [9] and [10], it is shown that the majority of the wave propagation happens in the substrate and through surface waves. Since there are local metal interconnects present in the same metal layer as that of the antenna, substantial amount of power can be transmitted to these interconnects from the radiations. Hence, it is critical to analyze the signal coupling between the antenna and the metal interconnects. Since the metal interconnects are essentially micro-strip elements, the signal coupling depends on the dimensions of the interconnect. In [7], the signal coupling between the on-chip antennas and the metal interconnects is characterized for varying width, length and placement of the metal interconnect. It is shown in [7] that it is possible to have a good electromagnetic compatibility for the on-chip antennas. In [7] guidelines are provided for the dimensions and placement of the metal interconnects in presence of on-chip antennas.

Though [7] investigates the signal coupling between the on-chip antennas and the metal interconnects, it does not consider the effect of this signal coupling on the CMOS digital circuits. The criticality of the analysis of the antenna electromagnetic radiation effects on the CMOS digital circuits significantly increases for deep sub-micron technologies as V_{DD} and noise margins for these technologies are scaled down significantly.

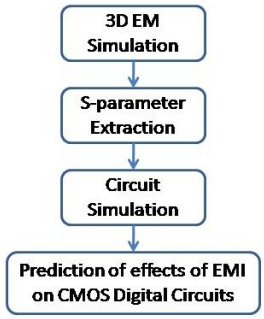


Fig. 2. Block diagram of the co-simulation methodology.

III. Co-simulation Methodology

The block diagram of the co-simulation methodology is shown in Figure 2. The 3D model of the die with the meander antennas and the interconnect is first simulated in a 3D FEM based full wave electromagnetic simulator. This simulation provides the scattering parameters (s-parameters) for the network (Tx and Rx antennas and metal interconnect ports). The four port s-parameter data describes both the desired signal coupling between the transmitting and receiving antennas and the undesired signal coupling between the transmitting antenna and the metal interconnect. The model incorporates the typical environment of operation of the on-chip antennas. The resulting s-parameters from the 3D EM simulation is then co-simulated with the RF models of the devices with a circuit simulator. This co-simulation methodology has also been used in [11].

A. Electromagnetic Simulation

The study in [7] concludes the following trends for the signal coupling between the on-chip antennas and the metal interconnects. The coupling:

1) Decreases with placement in different metal layers. Lower coupling for higher separation of metal layers,
2) Remains approximately constant with varying width of the interconnect,
3) Is low at small interconnect lengths. Peaks at interconnect length of approximately quarter of the wavelength of the EM waves,
4) Monotonously decreases with increasing distance from the transmitting antenna.

Based on these results, only the worst case simulations are repeated in this work for the 9-metal 90 nm process. In particular, the EM simulations are performed for interconnects on the same metal layer as that of the transmitting antenna. Also, since the signal coupling remains approximately constant with varying widths, the minimum width ($= 3\ \mu m$) of the interconnect for the ninth metal layer is considered. Since the signal coupling varies substantially with length, the length of the interconnect is varied from $100\ \mu m$ to $1500\ \mu m$.

The electromagnetic radiation effects of the wireless interconnect system on a die are obtained using Ansoft HFSS (High

TABLE I

MATERIAL CHARACTERISTICS OF DIFFERENT SILICON REGIONS ON A DIE.

Material	Conductivity (S/m)	Relative Permittivity
Silicon Dioxide	0	3.7
20 Ω-cm Substrate (lightly doped)	5	11.9
P-type Silicon	800	11.9
N-type Silicon	2300	11.9

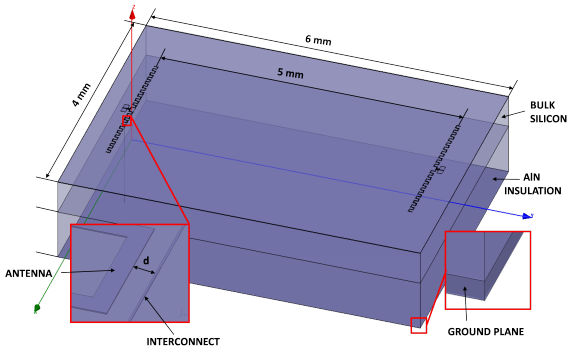


Fig. 3. Simulated structure for the wireless interconnect system.

Frequency Structure Simulator) [12], a 3-D FEM based full-wave electromagnetic simulator. In particular, the wireless interconnect system is analyzed for the coupling of the transmitting and receiving antennas as well as the (undesirable) coupling between the transmitting antenna and the metal interconnects. The design parameters for the die are selected according to a typical 9-metal layer 90 nm CMOS technology manufactory data. Conductivity parameters of this 90 nm CMOS technology are presented in Table I [11]. In the 9-metal layer 90 nm process, the antennas are placed on the 9^{th} metal layer, and are operating at a frequency of 15 GHz. The simulation structure is shown in Figure 3.

B. Circuit Simulation

The s-parameter data obtained from the 3D EM simulation for different interconnect lengths l and separation d from the transmitting antenna is incorporated into Agilent ADS (Advanced Design System) [13] for simulation with the RF models of the devices. This simulation setup is shown in Figure 4. Typical ICs have three types of interconnects, *a)* V_{DD}, *b)* GND and *c)* signal or data interconnects. The electromagnetic interference effect on the output of an inverter is investigated for all three interconnect types.

The electromagnetic interference effect on the output of the "driven buffer" is investigated by simultaneously providing an input at the "INT-1" port and at the "Tx port". The "Tx port" is excited with a 1 V, 15 GHz (the operating frequency of the antennas) sinusoidal signal. First, the electromagnetic interference effect is studied by assuming the metal interconnect to be a V_{DD} interconnect. The "INT-1" port is connected to a power supply and the "INT-2" port to the V_{DD} supply of the "driven buffer". A similar analysis is performed for the GND interconnect by connecting the "INT-1" port to ground and the

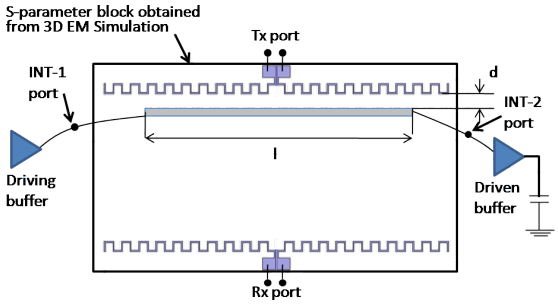


Fig. 4. Circuit simulation setup.

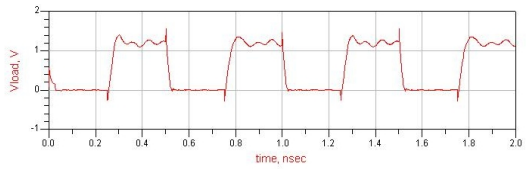
"INT-2" port to the ground connection of the "driven buffer". The electromagnetic interference effect on the output of the "driven buffer" assuming the metal interconnect is a signal or data interconnect is performed by exciting the "INT-1" port with the "Driving buffer" provided with a 2 GHz square wave input. The load capacitor is set at 40 fF, which is the input capacitance seen while driving an inverter with a PMOS of width 20 μm and a NMOS of width 8 μm for the selected 90 nm process technology. The MOSFET devices are modeled according to the BSIMv4 parameters, which are optimized for and incorporate the high frequency effects of a MOSFET device [14].

IV. RESULTS AND DISCUSSIONS

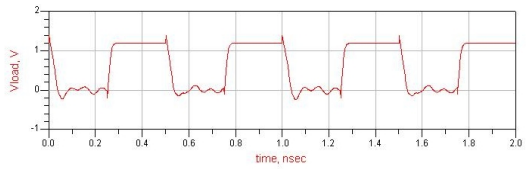
The s-parameter data for the four port network (Tx and Rx antennas and metal interconnect ports) is obtained from the EM simulations. The EM simulations are performed for varying lengths of a 3 μm wide interconnect placed at a distance of 1 μm from the transmitting antenna on the same metal layer as the transmitting antenna. Since the signal coupling between the transmitting antenna and the metal interconnect decreases with increasing distance between the two [7], a separation of 1 μm between the transmitting antenna and the metal interconnect provides the worst case scenario. The length of the interconnect is varied from 100 μm to 1500 μm, and the distance between the transmitting and receiving antennas is kept fixed at 5 mm.

The results of the EM simulation for the signal coupling between the transmitting antenna and varying lengths of the metal interconnect follow a similar trend to the results reported in [7]—the signal coupling increases with increasing length of the metal interconnects. The signal coupling is characterized by the s-parameters between the interconnect ports and the transmitting antenna.

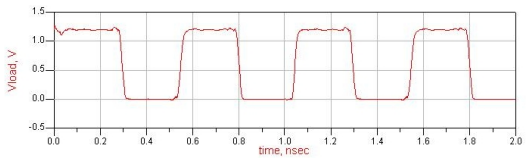
In order to characterize the level at which the output of the "driven buffer" is not acceptable the noise margin for a symmetric inverter is considered. For a symmetric inverter designed using the regular threshold voltage in the chosen 90 nm process technology the noise margin high and noise margin low are 0.48 V. Hence, if the output "high" or "low" of the "driven buffer" which represents bit 1 and 0, respectively, is 0.48 V below V_{DD} or 0.48 V above GND then the output signal is considered unacceptable. Such an unacceptable signal can cause malfunctioning of the digital circuit by causing the



(a) V_{DD} interconnect.

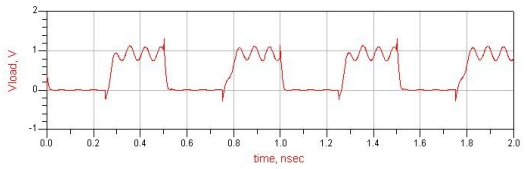


(b) GND interconnect.

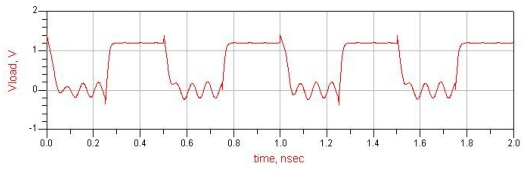


(c) Signal and data interconnect.

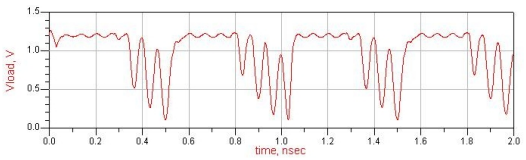
Fig. 5. Effects of electromagnetic interaction between the transmitting antenna and a 100 μm long metal interconnect on the CMOS digital circuit.



(a) V_{DD} interconnect.



(b) GND interconnect.



(c) Signal and data interconnect.

Fig. 6. Effects of electromagnetic interaction between the transmitting antenna and a 1000 μm long metal interconnect on the CMOS digital circuit.

subsequent circuits to switch states due to the interference from the wireless interconnects.

The co-simulation results for a 100 μm and a 1000 μm long interconnect are shown in Figure 5 and Figure 6, respectively. These two solution sets provide for a nominal case and a case for failure of the CMOS digital circuits due to the electromagnetic interference, the results for all the other metal interconnect lengths in this range lie between these two cases. It is observed that for shorter lengths (lower signal coupling) of the interconnects the effects of the electromagnetic interference is minimal. It is also possible for the interference to disrupt the logical functionality of the digital circuits for a longer length of the metal interconnects. However, such continuous long lengths of the interconnects are not typical of ICs. They are typically broken down to smaller sections with buffers to replenish the signal. If a scenario exists wherein such continuous long lengths need to be implemented, then the interconnect should be placed at a larger distance from the transmitting antenna to reduce the signal coupling as discussed in [7].

V. Conclusion

The electromagnetic compatibility of wireless interconnects using on-chip antennas is studied using a 3D FEM based full-wave and circuit analysis co-simulation methodology for a 9-metal layer 90 nm CMOS process technology. It is shown that it is possible to have a good electromagnetic compatibility between wireless interconnects using on-chip antennas and the IC elements. It is shown that for most typical interconnect geometry and placement the effects of the electromagnetic interference on the circuit elements is minimal. The design considerations for the interconnect geometry and placement with respect to the antenna specifications must be integrated into the physical design automation processes for a system utilizing wireless interconnects.

References

[1] *ITRS International Technology Roadmap for Semiconductors*, 2006.

[2] D. Sylvester and K. Keutzer, "A global wiring paradigm for deep submicron design," *IEEE Transactions on Computer-Aided Design of Integrated Circuit and Systems*, vol. 19, pp. 242–252, February 2000.

[3] P. Garrou, C. Bower, and P. Ramm, *Handbook of 3D Integration: Technology and Applications of 3D Integrated Circuits*. Wiley, 2008.

[4] M. F. Chang, V. P. Roychowdhury, L. Zhang, H. Shin, and Y. Qian, "RF/wireless interconnect for inter- and intra-chip communications," *Proceedings of the IEEE*, vol. 89, pp. 456–466, April 2001.

[5] B. A. Floyd, C. M. Hung, and K. K. O, "Intra-chip wireless interconnect for clock distribution implemented with integrated antennas, receivers and transmitters," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 543–551, May 2002.

[6] M. Bialkowski and A. Abbosh, "Investigations into intra chip wireless interconnection for ultra large scale integration technology," in *Proceedings of the IEEE Antennas and Propagation Society International Symposium (APSURSI)*, June 2009, pp. 1–4.

[7] A. More and B. Taskin, "Simulation based study of wireless RF interconnects for practical cmos implementation," in *Proceedings of the System Level Interconnect Prediction (SLIP)*, June 2010, (in press).

[8] ——, "Leakage current analysis for intra-chip wireless interconnects," in *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 49–53.

[9] K. Kim, "Design and characterization of RF components for inter- and intra- chip wireless communication," Ph.D. dissertation, University of Florida, 2000.

[10] M. Sun, Y. P. Zhang, G. X. Zheng, and W. Y. Yin, "Performance of intra-chip wireless interconnect using on-chip antennas and UWB radios," *IEEE Transactions on Antennas and Propagation*, vol. 57, pp. 2756–2762, September 2009.

[11] S. Bronckers, K. Scheir, G. V. Plas, G. Vandersteen, and Y. Rolain, "A methodology to predict the impact of substrate noise in analog/RF systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuit and Systems*, vol. 28, pp. 1613–1626, November 2009.

[12] *High Frequency Structure Simulator: User's Guide*, 10th ed., Ansoft Corporation, June 2005.

[13] *Advanced Design System: User's Guide*, Agilent Corporation.

[14] *BSIM4.6.4 MOSFET Model: User's Manual*, University of California, Berkley.