FOPAC: Flexible On-chip Power and Clock

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***Abstract*—A novel flexible on-chip power and clock (FOPAC) generation and distribution circuit is proposed to enable fast dynamic voltage and frequency scaling (DVFS). FOPAC utilizes resonant rotary clocks (ReRoCs) along with multi-phase voltage regulators (MPVR) for the clock and power generation and distribution. The locally distributed ReRoCs provide the required clock phases to the MPVR, and the MPVR provides the required voltage levels to the ReRoC, providing spatial and temporal flexibility for fast DVFS. The ReRoC and MPVR share the on-chip fly capacitor of the switched capacitor voltage regulators to achieve greater frequency scaling at run-time while reducing the overhead. The FOPAC architecture is evaluated on industrial designs demonstrating a <2 ns DVFS switching time.**

***Index Terms*—Resonant rotary clock, voltage regulators, low power, VLSI.**

I. Introduction

MODERN integrated circuits have an increasing need for various levels of both supply voltage (V) and operating frequency (f) available at fine spatial and temporal granularity. This work introduces a unique solution that provides a high number and quality of locally distributed V/f domains through FOPAC, as shown in Figure 1. Opportunistically sharing design resources and features between multi-phase voltage regulators (MPVRs) and resonant rotary clocks (ReRoCs) enabling i) the scalability to hundreds of domains, ii) fast switching times for both voltage and frequency, leading to temporal flexibility, and iii) locally distributed designs, leading to spatial flexibility.

The performance improvements and power savings enabled by flexible on-chip power and clocks (FOPAC) are motivated in Figure 2 with shaded regions. When a higher performance is needed, the voltage is scaled up (V_0 to V_1) followed by frequency up-scaling (f_0 to f_1). The speed of V/f up-scaling enables high performance node starting at time t_2 as opposed to t_4 in Figure 2. Alternatively, when a lower performance is sufficient (i.e. for better energy-efficiency), the frequency is decreased followed by voltage down-scaling. Here, the speed of down-scaling enables higher amount of time to be spent in the lower performance node, initiated at time t_8 as opposed to t_9 in Figure 2. The granularities of the voltage V and frequency f values achievable with specific hardware implementations also impact the energy-efficiency. Costly implementations of fractional PLLs are used to provide frequency granularity (such as in [1]), whereas a multitude of voltage regulators and power grids are common to provide voltage granularity.

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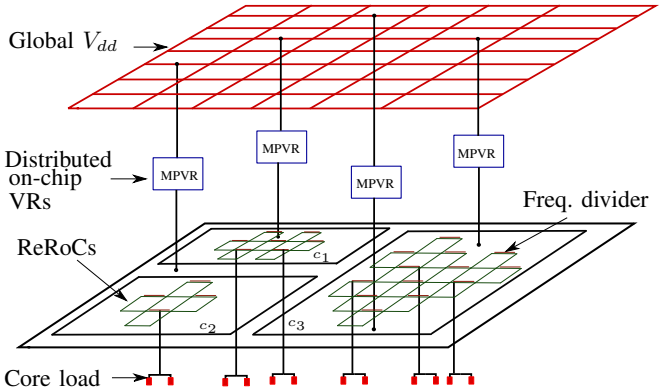


Fig. 1. FOPAC topology with resonant rotary clocks (ReRoC) and multiphase voltage regulators (MPVR).

FOPAC provides spatially and temporally flexible power/clock domains that are fine-tuned for each individual unit and collectively designed with shared overhead with superior performance. This flexibility comes with significant savings in power, performance, area, and accuracy, thanks to the opportunistic design of the MPVR and the ReRoC, leading to the following novelties:

1) fast switching between different V/f pairs,
2) symmetric switching between V/f pairs to improve power savings and performance, as illustrated in Figure 2,
3) improved granularity of frequency values, without the overhead of multiple fractional PLLs distributed locally,
4) opportunistic sharing of the fly capacitor as illustrated in Figure 3, to reduce design overhead and to help scale

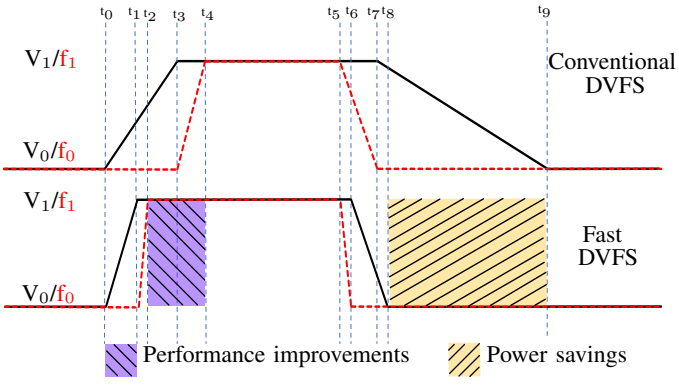


Fig. 2. Fast and symmetric DVFS with FOPAC.

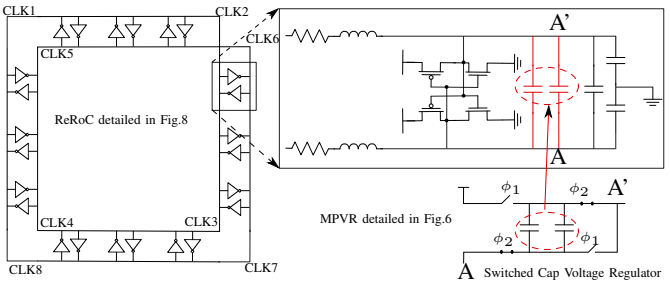


Fig. 3. FOPAC circuit with the multiphase voltage regulator sharing the fly capacitor with the resonant rotary clock.

the ReRoC frequency,

5) power savings of ≈35% as compared to PLL based designs.

The preliminaries encapsulating the circuit level aspects necessary for the proposed DVFS approach with ReRoCs and MPVRs are presented in Section II. The proposed architecture is presented in Section III. The simulation setup and results are discussed in Section IV. Conclusions are provided in Section V.

II. Preliminaries

The following sections discuss the on-chip voltage regulator and resonant rotary clock background, and prior works.

A. Switched Capacitor Voltage Regulator

On-chip voltage regulators (OCVRs) have been widely studied in prior works making the implementation feasible in traditional CMOS processes [2–5]. OCVRs can provide faster voltage scaling, reduce the number of dedicated I/O pins to the power, and facilitate fine granularity power management techniques [2, 4, 6]. Switched capacitor voltage regulators (SCVR) utilize fly capacitors to generate a DC output voltage [2]. A schematic of a 2:1 SCVR is illustrated in Figure 4. SCVRs are designed with non-overlapping signals ϕ_1 and ϕ_2 that operate at the MHz frequency range [7]. The intrinsic, switching, and conduction loses related to the fly capacitors result in lower conversion efficiency. To overcome the ripple at the output, multi-stage interleaving is proposed [3, 8]. Interleaving necessitates the need for multiple phases of the clock [3, 8]. To generate multiple clock phases, dedicated and robust clock sources are required.

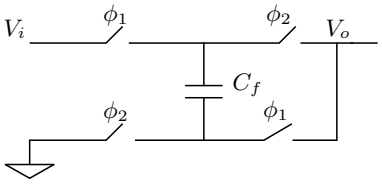


Fig. 4. 2:1 Switched capacitor voltage regulator (SCVR).

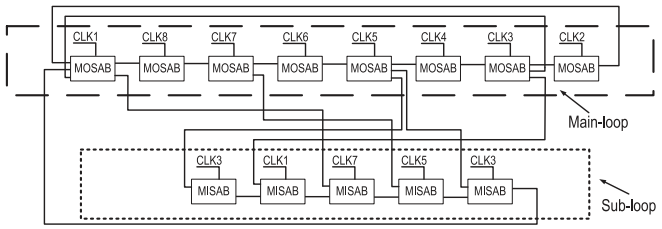


Fig. 5. Dynamic resonant rotary frequency divider [9].

B. Resonant Rotary Clock Design

Resonant rotary clocks (ReRoCs) is a type of resonant clocking with constant magnitude, low power, low jitter, and multiple phases [10]. ReRoCs are designed using IC interconnects for the transmission lines and inverter pairs that are uniformly distributed along the transmission lines in anti-parallel fashion, as illustrated in Figure 3. The ReRoC is modeled as an LC oscillator, where the frequency is estimated by,

$$f_{osc} = \frac{1}{2\sqrt{L_T C_T}}. \quad (1)$$

In Eq. (1), f_{osc} is the operating frequency of the ReRoC. The total inductance and total capacitance is given by L_T and C_T, respectively [10]. Most efficient design of ReRoCs are sparse rotary oscillator arrays (SROA) [11], similar to a non-uniform clock mesh topology. The capacitive load and inductance affect the frequency of oscillations. SROA is correct by design through algorithmic novelties proposed in the local distribution for use in the proposed FOPAC methodology.

The improved granularity of frequency values, without the overhead of multiple local fractional PLLs, is achieved via the use of the resonant frequency dividers [9]. The frequency dividers, as illustrated in Figure 5, are designed with spot advancing blocks (SAB) and transmission gates for the multiplexers to maintain the adiabatic property of the ReRoCs. The building blocks are the multi-input SABs (MISAB) and multi-output SABs (MOSAB), as illustrated in Figure 5. CLK1 through CLK8 inputs of the SABs are the multiple phases readily available on each local ReRoC building block of the SROA. In particular, CLK1 is shifted by 0° from a reference, whereas CLKN is shifted by (N-1)*360/N degrees. The dynamic frequency division, with improved granularity proposed in this work is accomplished by topologically changing the connections CLK1 through CLK8 shown in Figure 5.

C. Prior Work

The existing resonant DVFS approaches have relatively low frequency scalability and require bulky inductors and capacitors [5, 12–14] making it challenging to achieve high energy efficiency. On-chip SCVRs have been prototyped targeting high conversion efficiency [2, 3]. These prior works achieve good conversion efficiencies but require robust multi-phase non-overlapping clock signals. The generation and synchronization of the input clock signal to each multi-phase voltage regulator (MPVR) stage becomes quite costly and even

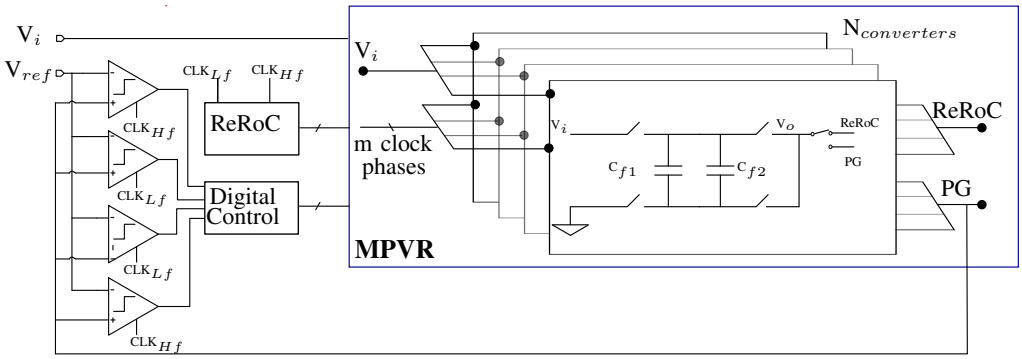


Fig. 6. FOPAC device: MPVR architecture with ReRoCs.

unfeasible when the number of phases is very high [15, 16]. A prototype implementation for the MPVRs utilized ring oscillators to generate the multi-phase clock signals [15]. Prototype implementations of ReRoCs on silicon have been presented to explore the energy efficiency and the multiple phases [10, 17]. Rotary clock based distribution networks have been well studied in recent years focusing on optimization of the local and global clock networks [11, 18–22]. Additionally, there has been some work on the co-design of power and clock distribution network [23] which focuses on the global interconnect, rather than the fusion of power and clock generation circuitry. In Table I, the silicon measured results for DVFS and DVS implementations for resonant clocking and multiphase SCVRs are presented, respectively.

III. Proposed FOPAC Architecture

Flexible on-chip power and clock (FOPAC) architecture encompasses the FOPAC circuit building blocks, as illustrated in Figure 3, distributed through a circuit, as illustrated in Figure 1, using an ASIC-flow-compliant methodology. The on-chip voltage regulators are distributed throughout the power grid and the ReRoCs are distributed locally. The FOPAC methodology is detailed in the following sections, first focusing on DVFS operation (Section III-A and Section III-B) and next on describing the integration with standard ASIC flow (Section III-C).

TABLE I
Prior works with silicon prototypes.

Design	Restle [5] ISSCC 2014	Rahman [12] JSSC 2018	Lu [15] ISSCC 2015
Technology	22 nm SOI	65 nm bulk	65 nm bulk
Results	Experimental	Experimental	Experimental
Clock source	PLL+resonant grid	PLL+resonant grid	VCO
System resonant	Always	Always	No
Resonant DVFS	No	Yes	No, DVS only
Voltage range	0.75-1.05 V	0.7-1.2 V	0.6-1.2 V
Frequency range	2.5-5 GHz	DC-132 MHz	-
Inductor	On chip (0.3-2.5 nH each)	Off chip (7 nH)	-
Voltage regulator (VR)	Yes	No	Yes
DVS speed	DNR	-	2.5 V/μs
η_{max} of VR	DNR	-	78.3%
ρ (W/mm^2) @η_{max}	DNR	-	0.18
Power reduction	36%	34%-38%	-
Clock power reduction	-	-	-

DNR - Did not report

A. Dynamic Voltage Scaling with MPVR

The circuit topology for the proposed MPVR, which is an integrated SCVR with ReRoC for FOPAC, is illustrated in Figure 6. MPVRs are designed with ReRoCs that provide the multiple clock phases for the interleaved operation. The voltage ripple across the capacitor is reduced with multi-phase interleaving [3, 8], and the ReRoCs provide higher granularity of phases. The adaptive gain comparators and the integrator logic in the feedback loop are illustrated in Figure 6 and 7, respectively [24]. The comparators that provide high gain in the design are driven by a higher frequency clock signal (CLK$_{Hf}$) whereas the comparators that provide nominal gain by a lower frequency clock signal (CLK$_{Lf}$) [24]. This significantly improves the speed of the regulation at the output of the MPVR while also maintaining the stability of the control loop. The two different frequencies of the clock signal are provided from the same ReRoC, with the minimal overhead of an additional frequency divider. The comparator architecture is chosen as double-tail latch-type for speed and low kickback noise. To increase the settling speed of the integrator, several integrator regions that have different step sizes based on the difference in between the output and reference voltages are designed. This technique helps the integrator to keep up with the actual current requirement at the output rather than setting it to the maximum value for fast recovery [8].

Overall, one ReRoC structure with k dividers can provide the k distinct clock frequencies for comparator operation, and the m multi-phase signals, shown in Figure 6 for k=2 (i.e. for CLK$_{Hf}$ and CLK$_{Lf}$). ReRoCs are designed in the GHz frequency range and the clock for the SCVR is generated after frequency division and duty cycle conversion. The placement of the frequency dividers with respect to the ReRoC rings is illustrated in Figure 8. It is straight forward to tap the m multi-phase clock sources for the SCVRs since the tapping locations are accurately known and the routing not as complex as clock distribution networks accomplished in [21]. Consider the tapping point for a particular phase Θ_{P_i} to be located at (x,y). The SCVR clock source taps onto Θ_{P_i} that satisfies the phase requirement. The placement of the SCVR depends on: i) Θ_{SCVR_p} - the phase required for the SCVR and ii) Θ_{l_i} the phase attributed to the tapping wire l_i. The SCVR is placed such that $\Theta_{SCVR_p} = \Theta_{l_i} + \Theta_{P_i}$.

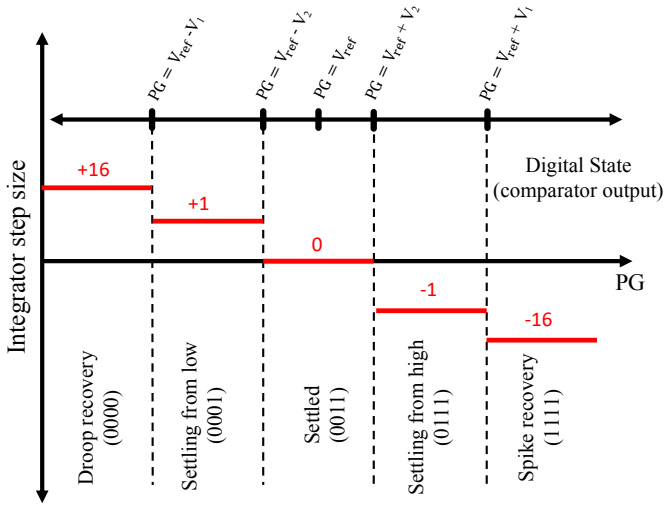


Fig. 7. Integrator logic [24].

Two sets of results are presented to validate and measure the effectiveness of the DVS operation with MPVR. The first set of results is the symmetric and fast response to both step-up and step-down changes in the reference voltage of the MPVR with a maximum output current of 50 mA shown in Figure 9. The high gain comparators are clocked at an arbitrarily selected ReRoC frequency of 3.3 GHz (CLK$_{Hf}$ in Figure 6). The nominal gain comparators (CLK$_{Lf}$ in Figure 6) and MPVRs are clocked at 360 MHz after performing frequency division by 9. Step-up and step-down scaling with MPVRs takes 89 ps and 87 ps, respectively. The robust ReRoC signals with accurate phase matching between the SCVRs and ReRoCs along with the digital control helps in achieving the symmetric step-up and step-down scaling of the MPVRs. A maximum voltage ripple of 20 mV is achieved with 18 interleaved stages of the MPVR.

The second set of results for DVS scaling with MPVR are based on the fly capacitor selection on i) SCVR conversion efficiency and ii) the opportunistic design assisting DFS. In Figure 10(a), the voltage conversion efficiency η_{SCVR} for different fly capacitor values is shown. The overall power

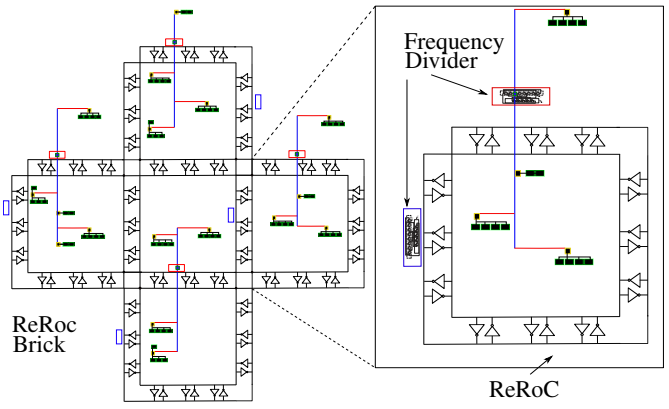


Fig. 8. ReRoC with divider placement.

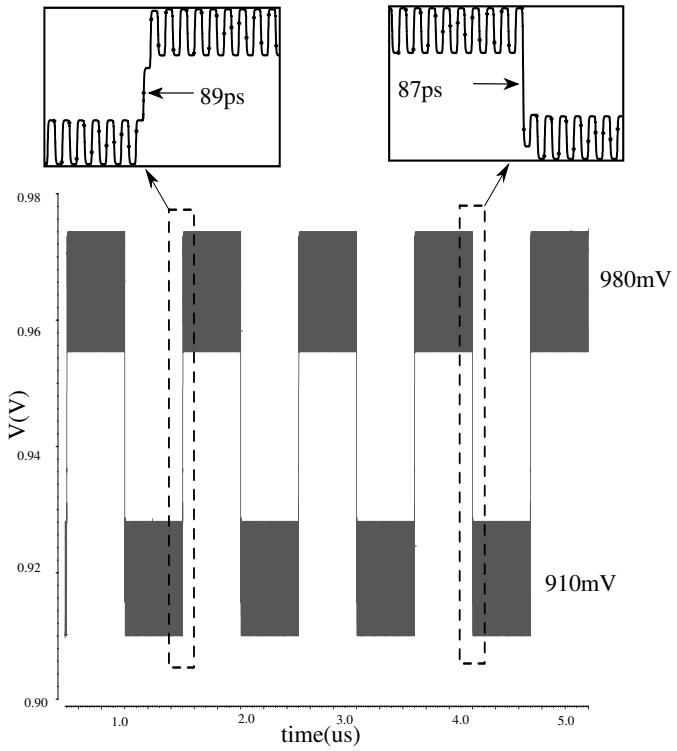


Fig. 9. MPVR symmetric step up and step down scaling, with reference voltages of 980 mV and 910 mV.

efficiency of the SCVR is computed as,

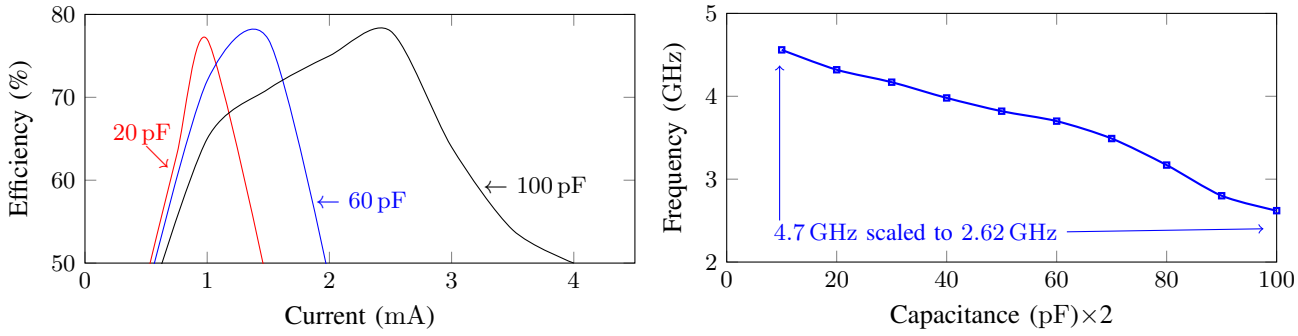
$$\eta_{SCVR} = \frac{P_{out}}{P_{out} + P_{sw} + P_{buff} + P_{control} + P_{par}}. \quad (2)$$

In Eq. (2), $P_{out}, P_{sw}, P_{buff}, P_{par}$, and $P_{control}$ are the output power, switching power, buffer power, parasitic power, and control and reference circuit related power, respectively. These values are obtained from SPICE simulations of extracted layouts of a FOPAC designed in a 65 nm technology. The (known) impact of the fly capacitor size on the maximum power efficiency is for varying load current is shown in Figure 10(a). The fly capacitors can be split to achieve maximum power efficiency for varying load currents.

In the FOPAC architecture, fly capacitors connected to the ReRoCs can optionally be used to lower the frequency. Frequency scaling with different fly capacitor values on an arbitrarily selected ReRoC frequency of 4.7 GHz is shown in Figure 10(b). The fly capacitors are split to achieve finer granularity of frequency scaling. This design parameter of fly capacitors supplements the DFS operation provided by the resonant rotary divider (Section III-B), enabling even finer control of the DFS operation in FOPAC.

B. Dynamic Frequency Scaling of ReRoC

In the dynamic ReRoC frequency divider, illustrated in Figure 5, the phase delay between the adjacent MOSABs in the main-loop is expressed as $((m-1)/m)\cdot 2\pi$ and the phase delay between the MISABs in the sub-loop is expressed as $((m-2)/m)\cdot 2\pi$ [9]. When n_1 is the number of connections



(a) SCVR conversion efficiency

(b) Freq. scaling with fly cap

Fig. 10. Power conversion efficiency of SCVRs and frequency scaling of ReRoC with fly caps.

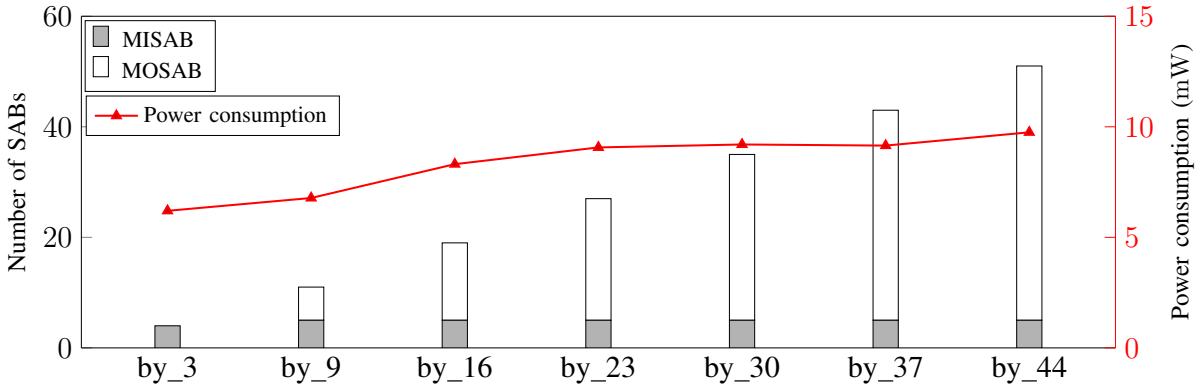


Fig. 11. Power consumption of the dynamic frequency divider, 6 main-loops and 1 sub-loop.

between the MOSABs in the main-loop, and n_2 is the number of connections between the MISABs and MOSABs in the main-loop and sub-loop, then the number of connections required to perform a division of ratio r is,

$$\left(n_1 \cdot \frac{m-1}{m}\right) \cdot 2\pi + \left(n_2 \cdot \frac{m-2}{m}\right) \cdot 2\pi = r \cdot 2\pi. \quad (3)$$

The m phases of the ReRoCs are used to produce the frequency divider output. When $m = 8$, the phase delays between the adjacent SABs in the main-loop is $7/8 \cdot 2\pi$ and the sub-loop is $6/8 \cdot 2\pi$, as illustrated in Figure 5. From Eq (3), to perform a frequency division of $r = 9$, $n_1 = 6$ and $n_2 = 5$ connections are required. This can be achieved with a circuit topology similar but not identical to that in Figure 5. The proposed topology is not identical because for $r = 10$, $n_1 = 8$ and $n_2 = 4$, connections would be required, which are higher than the available SABs in Figure 5 [9]. A modified topology is proposed in this paper in order to perform frequency division greater than 9. The main-loop in Figure 5 is stacked with an additional main-loop. An increase in the number of the main-loops requires larger multiplexers to enable the selection between the main-loops and the sub-loop. In [9], it is shown that restricting the number of MISABs in the sub-loop is desirable for power savings and lower area. Stacking additional main-loops, any integer division ratio from 3 to n can be achieved, at limited power and area cost. This is achieved by implementing the smallest number of n_1 and n_2 desirable for power savings and area reduction from Eq. (3).

The power consumption of the frequency dividers for division ratios 3 to 44 with a master clock of 3.3 GHz is shown in Figure 11. The total number of MISABs and MOSABs increases monotonically along with the division ratio. The power consumption however does not increase monotonically due to the adiabatic nature of the resonant frequency dividers and

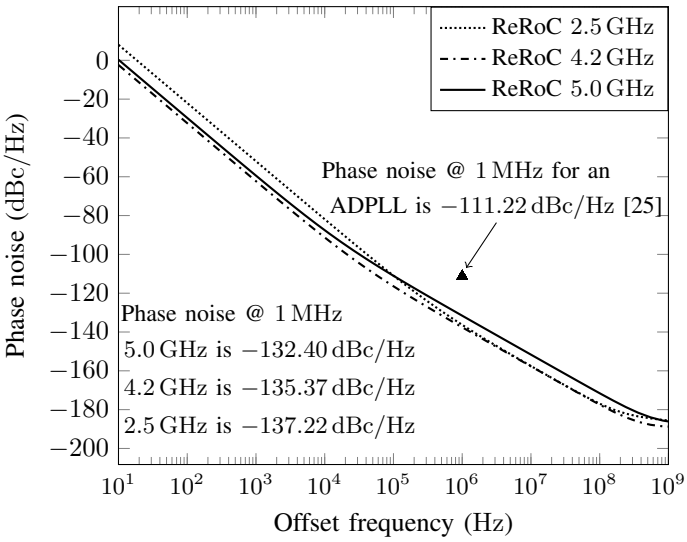


Fig. 12. Phase noise versus offset frequency of the ReRoCs.

TABLE II
DYNAMIC FREQUENCY SCALING WITH DIVIDER.

Div ratio	ReRoC master clock 2.5 GHz			ReRoC master clock 4.2 GHz			ReRoC master clock 5 GHz		
	Power (mW)	Power normalized to div ratio 44	DFS time (ns)	Power (mW)	Power normalized to div ratio 44	DFS time (ns)	Power (mW)	Power normalized to div ratio 44	DFS time (ns)
3	7.32	0.67×	1.18	5.20	0.59×	0.72	4.31	0.55×	0.59
9	7.90	0.73×	1.19	5.78	0.66×	0.69	4.89	0.62×	0.60
16	9.43	0.87×	1.19	7.31	0.84×	0.71	6.42	0.82×	0.61
23	10.18	0.94×	1.21	8.07	0.92×	0.70	7.18	0.91×	0.60
30	10.32	0.95×	1.20	8.20	0.94×	0.71	7.31	0.93×	0.60
37	10.27	0.94×	1.19	8.15	0.93×	0.72	7.26	0.92×	0.60
44	10.87	1×	1.19	8.74	1×	0.68	7.86	1×	0.59
Avg.	9.47	0.85×	1.19	7.35	0.81×	0.70	6.46	0.79×	0.60

the selection lines for the DFS. The switching time between frequency domains is approximately 3 clock cycles (≈0.60 ns for a 5 GHz clock). Experiments are repeated for arbitrarily selected master clock frequencies of 2.5 GHz, 4.2 GHz, and 5 GHz, demonstrating similar trends of sub-linearly increasing power dissipation with increasing divider value and under 3 clock cycles of switching time for DFS as shown in Table II.

In Figure 12, the phase noise of the ReRoCs designed for Table II is plotted. The phase noise of the 2.5 GHz ReRoC at an offset frequency of 1 MHz is −137.22 dBc/Hz. The phase noise for the 4.2 GHz and 5 GHz master clock frequencies are −135.37 dBc/Hz and −132.40 dBc/Hz, respectively. An all digital phase locked loop (ADPLL) manufactured in the 65 nm SOI technology node with an output frequency of 4 GHz has a phase noise of −111.22 dBc/Hz at an offset frequency of 1 MHz [25].

C. FOPAC Methodology

The novelties of this work are embedded into the FOPAC methodology, compliant with the traditional ASIC flow, as illustrated in Figure 13. First, the design is synthesized with an industrial tool and undergoes initial placement, power planning, and placement blockages for the ReRoCs. Then, the designs undergo ReRoC design and power generation. The custom flows enabling FOPAC are as follows:

1) ReRoC design: The custom ReRoC clock distribution network synthesis has five steps, illustrated in Figure 13.

1) Register clustering to generate balanced capacitance load clusters.
2) BST/DME to generate an unbuffered steiner tree for each cluster [26].
3) ReRoC topology generation with the dynamic frequency dividers.
4) Generation of synchronous distribution aware sparse ReRoCs (SReRoC) [11].
5) Physical connections translation to a netlist and PVT analysis of the clock distribution network.

Step 1 and step 2 constitute the subnetwork tree generation process for a bottom-up clock tree synthesis (CTS) process. The clock network and distribution are designed to be correct by design, thanks to steps 1 through 4, concluding with the PVT analysis with SPICE-accurate verification in step 5. The proposed steps for ReRoC are similar to [27], where [27] details the automation of resonant rotary clock design for any ASIC design. ReRoC is differentiated from [27] in co-designing clock and power, i.e. the power planning input to the ReRoC Stage has pervasive impact on the ReRoC design, as the fly capacitors are opportunistically shared.

2) Power generation: The power generation (and distribution) has five steps, illustrated in Figure 13.

1) Power budget estimation for the design.
2) Determination of the number of SCVRs and topology.
3) Placement of the MPVR.
4) Power grid extraction along with the ReRoCs and core load.
5) Worst case static IR and Ldi/dt analysis.

The input to Step 1 is the topology of the ReRoC rings including the number of ReRoC rings and tapping points for the multiple phases required for the MPVRs from the

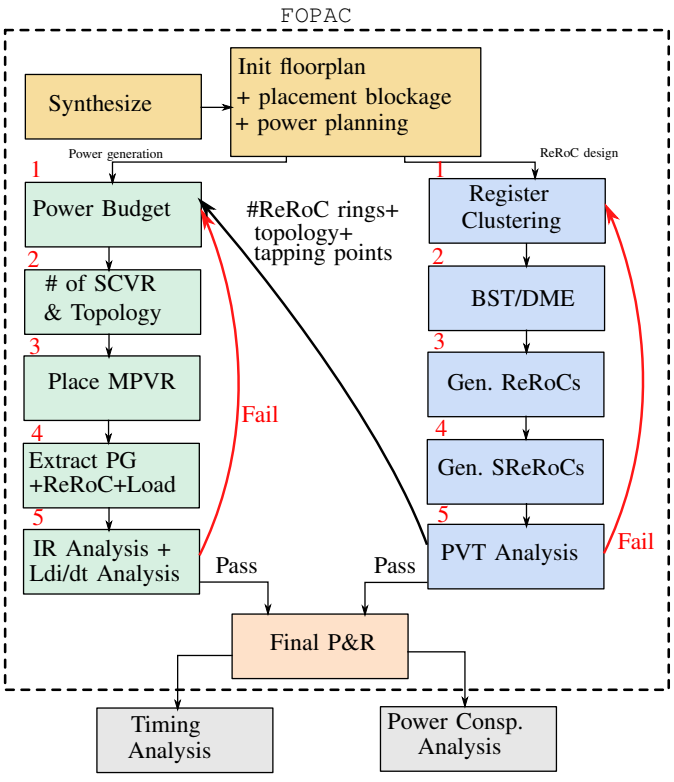


Fig. 13. FOPAC Methodology.

ReRoC design flow. For a given power budget, an SCVR topology is designed with the goal of achieving the desired target efficiency by distributing the power budget over multiple SCVRs. The number of SCVRs required is divided such that each ReRoC ring has a voltage regulator (with load balancing) and the rest of the design has the appropriate number of voltage regulators necessary to operate during the low performance mode. Similar to use of PVT analysis in ReRoC design for DFS, the power generation stage utilizes SPICE simulations in step 5 for signal integrity analysis of DVS operation.

IV. FOPAC Evaluation

FOPAC is demonstrated on three different industrial designs that are publicly available: 1) *AES* encryption core, 2) *Arm core* - CORTEX M0, and 3) *VSCALE* RISC-V. The designs are placed and routed (P&R) and subjected to STA in order to verify the timing of the ASIC flow at the system level. The timing and power characteristics of the FOPAC components (ReRoC and MPVR) are analyzed in deeper detail through SPICE simulations of layout-extracted models that include parasitics. In particular, the transmission line interconnect parasitics are extracted using the high frequency structural simulator (HFSS) [28]. The algorithms are implemented in C++ and Matlab. An industrial 65 nm technology library is used for the evaluation.

The simulations results and conclusions are presented within three major categories:

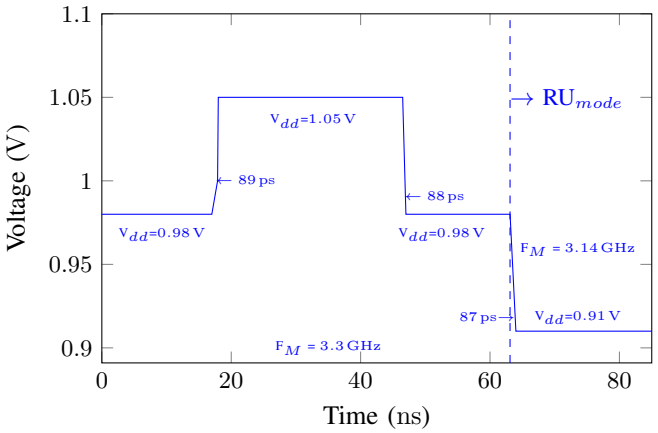
1) FOPAC DVFS operation,
2) FOPAC power consumption with respect to traditional systems, and
3) FOPACs power consumption with respect to previous literature on resonant systems.

A. FOPAC DVFS Operation

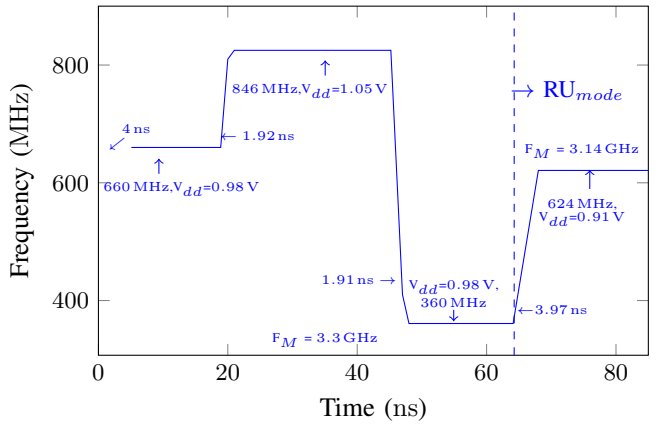
An arbitrary ReRoC frequency of 3.3 GHz (F_M) is chosen to evaluate the FOPAC methodology. Two sets of dynamic resonant frequency dividers to perform frequency division in integer ratios 3 to 9 are designed for the core clock source (F_{core}) and the MPVR clock source (F_{mpvr}). In the PVT stage, the geometries of the ReRoC rings along with the frequency dividers are varied ±10% to represent the worst case scenarios. The deviation from the target frequency of 3.3 GHz with PVT variations for 500 Monte-Carlo runs are presented in Table III. The variation analysis is performed across the three designs. Average frequency variations of <1% and <0.6% are observed under intra- and inter-die variations, respectively.

TABLE III
PVT, IR and Ldi/dt Analysis Results.

Design	PVT (500 Monte-Carlo Runs)		Static IR & Ldi/dt
	Max. intra-die	Max. inter-die	
AES cipher	31 MHz	15 MHz	2.1%
CORTEX M0	35 MHz	17 MHz	1.9%
VSCALE RISC-V	28 MHz	24 MHz	2.4%
Average	30 MHz	19 MHz	2.1%



(a) Dynamic voltage scaling speed



(b) Dynamic voltage and frequency scaling speed

Fig. 14. FOPAC DVFS operation on the RISC-V core.

Worst case static IR and Ldi/dt analysis are performed on the layout extracted industrial designs (RLC models). The average worst case voltage drop across the three industrial designs is 2.1% of the V_{dd}.

A sample operation of FOPAC DVFS operation of the RISC-V core is presented in Figure 14, prior to the presentation of the performance comparisons to prior work in literature in Tables IV and V. The switching speed between different frequency domains is <1 ns (≈3 cycles of F_M). At the start, it takes 3 ns for the ReRoC oscillations to sustain at 3.3 GHz (F_M). After which a divide by 5 is performed to generate the 660 MHz clock for the core (F_{core}) and divide by 9 to generate the 360 MHz clock (F_{mpvr}) for the MPVRs at V_{dd}= 0.98 V (nominal). The high gain comparators are clocked at F_M and nominal gain comparators are clocked at F_{mpvr}. The frequency F_{core} and voltage are scaled between different levels to validate the accuracy of the switching speed. To enable the fly capacitor reuse mode (RU_{mode}), 10 of the SCVRs are shut down and the fly capacitor is loaded to the ReRoC rings in the RISC-V core. In the RU_{mode}, it takes ≈3 ns for the frequency of the ReRoC F_M to stabilize to 3.14 GHz (with voltage scaling). Then, it takes 0.97 ns to scale F_{core} to 624 MHz and F_{mpvr} to 348 MHz to operate the RISC-V core in the RU_{mode} with V_{dd} = 0.91 V. In total, it takes

TABLE IV
POWER CONSUMPTION OF PLL DESIGN VERSUS FOPAC OPERATING AT FREQ= 825 MHz, V_{dd}= 0.98 V, AND TEMP.= 25 °C.

Design	Num. SCVRs	PLL clocked design		FOPAC		
		PLL_{clock} power (mW)	PLL_{core} power (mW)	$FOPAC_{clock}$ power (mW)	$FOPAC_{core}$ power (mW)	Num. ReRoC
AES cipher	8	18.17	57.60	5.96 (-67.19%)	37.87 (-34.25%)	4
CORTEX M0	12	26.04	73.74	9.34 (-64.13%)	45.56 (-38.21%)	6
VSCALE RISC-V	16	41.21	108.28	12.78 (-68.98%)	69.04 (-36.23%)	10
Average	-	-	-	-67%	-36%	-

3.97 ns to scale the frequency to the RU_{mode} at run time by utilizing the fly capacitor of the SCVRs.

B. FOPAC power consumption

The power consumption of the FOPAC based designs versus PLL based designs operating at 825 MHz is presented in Table IV. The PLL-based design is built with a traditional PLL from a cell library used on the ASIC implementations performed with Cadence Innovus. The designs are extracted with Mentor Graphics Calibre. Power measurements are presented for the PLL only, labeled PLL_{clock} in Table IV, and for the entire design, labeled PLL_{core} in Table IV. The power of the SCVRs, the frequency dividers, and the control circuit is included in $FOPAC_{core}$. The PLL based designs and FOPAC based designs have the same number of SCVRs. The clock source for the SCVRs in the PLL based designs are ring oscillators [15]. A total power saving of 36% is achieved for the circuits ($FOPAC_{core}$) when compared against a PLL clocked core (PLL_{core}). The clock power savings are significant for the clocks: 67% power savings ($FOPAC_{clock}$) when compared against a PLL based design (PLL_{clock}).

C. FOPAC power comparison with previous works

FOPAC is compared to prior resonant works with simulations only in Table V. The numbers reported in Table V are from SPICE simulations of the sweep of the V/f range— 0.9 to 1.2 V and 348 MHz to 1.1 GHz— over SS, FF, FS, and SF corners, and not only the results reported in Table IV. Overall, FOPAC delivers power with 77% efficiency, and achieves 25%-39% power reduction thanks to 64%-74% reduction in clock power. The voltage scaling within FOPAC is symmetric and robust with a (worst-case) $t_{response}$ of 89 ps. The DFS switching time within FOPAC utilizing a 3.3 GHz ReRoC is 0.9 ns. Overall, FOPAC demonstrates scaling of the voltage-frequency over a wide range without the need for on/off-chip inductors while re-utilizing (RU_{mode}) the fly capacitor for frequency tuning.

TABLE V
COMPARISON OF FOPAC WITH PRIOR SIMULATION WORK.

Design	Ahn [29] TCAD 2016	**This work FOPAC**
Technology	45 nm bulk	65 nm **bulk**
Results	Simulation	**Simulation**
Clock source	-	**ReRoC**
System resonant	Always	**Always**
Resonant DVFS	Yes	**Yes**
Voltage range	1.5 -1.9 V	**0.9-**1.2 V
Frequency range	2-4 GHz	348 MHz-1.1 GHz*
Inductor	On chip	**No**
Voltage regulator (VR)	No	**Yes**
DVS speed	-	7.86 V/μs
η_{max} of VR	-	**77%**
ρ (W/mm^2) @η_{max}	-	**0.17**
Power reduction	27%	**25%-39%**
Clock power reduction	-	**62%-74%**

*Resonant frequency divider topology dependent

V. CONCLUSIONS

In this paper, the fusion of resonant rotary clock with on chip voltage regulators enabling flexible on-chip power and clock is presented. FOPAC is designed and evaluated on three different industrial designs to validate the architecture. FOPAC can switch between different V/f domains in 1.9 ns with a ReRoC clock operating at 3.3 GHz. FOPAC achieves 25% - 39% power savings while offering fly capacitance re-usability to tune the ReRoC frequency at run time without any negative implications. FOPAC can provide high number of V/f domains with fast DVFS capability while consuming low-power and operating reliably, justified via evaluation on industrial designs in this work.

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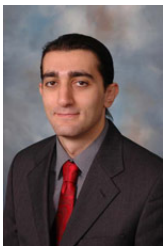

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