Electromagnetic Compatibility of CMOS On-chip Antennas

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Introduction

Radio frequency (RF) wireless interconnects are considered as a viable alternative for the distribution of global signals in semiconductor integrated circuits (ICs). The increased system complexity, density and die size of a typical IC, coupled with the reduction in the cross-sectional area of metal interconnects have increased the parasitic effects associated with the interconnects. Hence, the global interconnect lines are now considered a bottleneck to the increase in speed as the delay due to the interconnects is higher than the delay in the devices themselves [1].

One possible alternative to the global interconnects is to use wireless interconnects using on-chip antennas. Deep sub-micron semiconductor devices are capable of operating at frequencies higher than 10 GHz which enables the use of compact on-chip antennas. The study in [2] demonstrates the feasibility of establishing an intra-chip wireless communication channel for the global delivery of the clock signal. In [2–4], different antenna topologies are proposed for wireless interconnects. The signal coupling for the wireless communication channel between an on-chip antenna pair for intra-chip communication is shown to be due to wave propagation—not due to conduction through the substrate—demonstrating the true wireless behaviour of intra-chip communication [2, 3].

In [4], the effect of the presence of the metal interconnects on the transmission gain of the antenna pair is analyzed. However, the effect of the antenna radiations on the metal interconnects (there is mutual interaction) has not been critically analyzed. Since the majority of the wave propagation happens in the substrate and through surface waves [3, 5], substantial amount of power can be transmitted to the metal interconnects from the antenna radiations, causing signal integrity issues.

The novelty of this paper is in characterizing the effect of the radiations on the interconnects under varying geometries and topology. This study adheres to the typical complimentary metal oxide semiconductor (CMOS) process technologies and studies the possibility of integrating antennas on chip using standard foundry processes, which have not been considered in the majority of the previous work including [2–4]. The effects of a typical CMOS manufacturing process such as the lithographic limits on geometry and the presence of an epitaxial layer, are integrated in order to develop an accurate model for the presented finite element method (FEM) analysis.

Simulation Setup

The wireless interconnect system is analyzed for the coupling of the transmitting and receiving antennas as well as the (undesirable) coupling between the transmitting antenna and the metal interconnects. The simulations are performed in Ansoft HFSS (High Frequency Structure Simulator), a 3-D FEM based simulator [6]. The design parameters for the die are selected according to a typical 250 nm CMOS technology with the conductivity values presented in Table 1 [7]. Dipole meander antennas are designed to operate at 17 GHz with a total arm length of 2.4 mm according to the parameters presented in [8]. The wavelength of the radiated electromagnetic (EM) waves is 6.85 mm based on an approximate effective dielectric constant of 6.61 [9]. The die size is 6×4 mm^2 where the antennas are separated at a distance of 5 mm from each other. In the 3-metal layer 250 nm process, the antennas are placed in the third metal layer. The simulations are performed in the frequency range from 10 GHz to 30 GHz. The simulations are performed to observe the following:

1. The effects of the electromagnetic (EM) radiations from the antennas on interconnects considering:
   (a) Interconnect placement in the three different metal layers,
   (b) Varying width of interconnects from 2 μm to 10 μm,
   (c) Varying length of interconnects from 100 μm to 3200 μm,
   (d) Varying distance of interconnects from the transmitting antenna from 1 μm to 4.5 mm.
2. The effects of the typical CMOS manufacturing processes on the antenna design and operation characteristics:
   (a) Adherence to the 90° bend angles on the antennas as mandated by typical CMOS lithographic rules,
   (b) The presence of a high-conductivity epitaxial layer on the CMOS die.

Results and Discussions

The improvements in the accuracy of the frequency range of operation and the transmission gain over the previous work (which neglects the epitaxial layer) are shown in Figure 1. The presence of the epitaxial layer shifts the operation to a lower frequency range [Figure 1(a)]. Thus, the epitaxial layer reduces the transmission gain at the target frequency (17 GHz) by approximately 12 dB [Figure 1(b)], which is a significant reduction in signal coupling. Note that, a simulation based study of an alternate on-chip wireless interconnect system is reported in [4], where the presence of an epitaxial layer is neglected. The reported transmission gain in [4] is higher than all the results shown in Figure 1(b)—with or without the epitaxial layer. The substrate conductivity is suspected to be the primary reason for this discrepancy between the results provided in [4] and this work as no information about the substrate conductivity is provided in [4]. The substrate conductivity substantially changes the transmission gain between the antenna pair [3] and must be considered.

Between the p-type and n-type epitaxial layers, it is more desirable to use the p-type epitaxial layer for on-chip wireless interconnects both from the transmission gain and the bandwidth perspectives. Note that the (more common) p-type epitaxial layer is used for all other simulations with the frequency of operation at 15.6 GHz.

The simulation results for the coupling between the metal interconnects and the transmitting antenna show substantial variations under different geometrical sizes and placement. It is desired that the signal coupling between the transmitting antenna and the metal interconnect be low to avoid any signal integrity issues. The simulation results show that the coupling between the antenna and the interconnects:

1. Decreases with placement in different metal layers. Lower coupling is observed when interconnects are placed on metal layers further away from the layer of the antenna (Table 2),
2. Peaks at an interconnect width of 2 μm but variations are very low (approximately 0.5 dB) with varying widths of the interconnect [Figure 2(a)],
3. Is very low at short interconnect lengths. Peaks at an interconnect length of approximately a quarter of the wavelength of the EM waves [Figure 2(b)],
4. Monotonously decreases with an increasing distance from the transmitting antenna [Figure 2(c)].

Conclusion

It is shown that it is possible for a radio frequency (RF) wireless interconnects system to have good electromagnetic compatibility and low electromagnetic interference with the metal interconnects on the same die. The presence of a high-conductivity epitaxial layer, which is common in CMOS ICs but has been neglected in the previous works, is shown to decrease the transmission gain between the antenna pair by approximately 20% (21.60% and 23.78% for n-type and p-type, respectively). It is shown that the electromagnetic radiations from the antennas can cause significant coupling between the metal interconnects and the transmitting antenna depending on the geometry and placement of the interconnects. The design considerations presented in this paper must be integrated into the design process of on-chip antennas.

References

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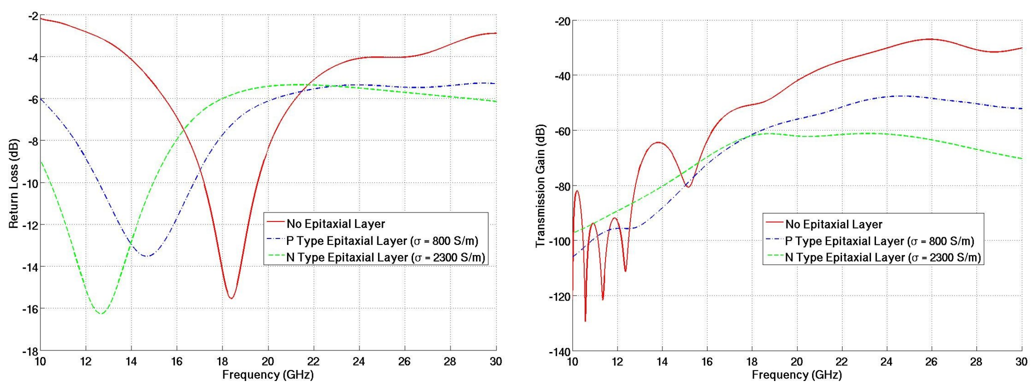
Table 1: Material characteristics of different silicon regions on a die.

Material	**Conductivity (S/m)**	**Relative Permittivity**
Silicon Dioxide	0	3.7
20 Ω-cm Substrate	5	11.9
P-type Silicon	800	11.9
N-type Silicon	2300	11.9

Table 2: Antenna coupling with a 2 μm wide, 1 mm long interconnect.

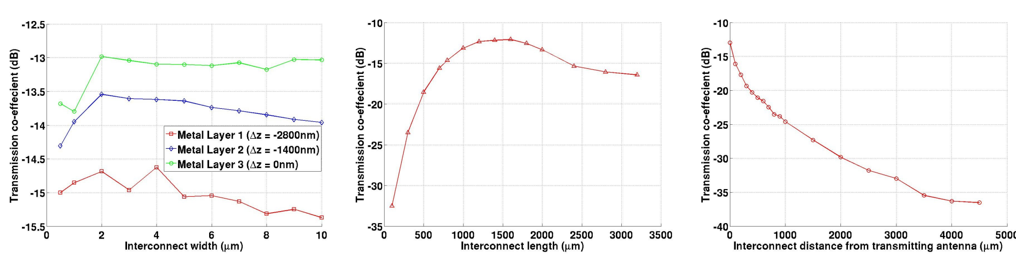
Metal Layer	**Distance from the Antenna Layer (nm)**	**Transmission S-parameter (dB)**	**% Change in the Transmission S-parameter**
M3	0	−12.98	–
M2	−1400	−13.54	4.31%
M1	−2800	−14.69	13.17%



(a) Return loss.

(b) Transmission gain.

Figure 1: Antenna characteristics for varying epitaxial layers.



(a) Interconnect width.

(b) Interconnect length.

(c) Interconnect distance to the transmitting antenna.

Figure 2: Signal coupling between the transmitting antenna and an interconnect.