

# A 900 MHz Charge Recovery Comparator With 40 fJ per Conversion

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**Abstract**—The idea of recycling part of the charge used to drive a load is well understood in digital circuits, and falls under the umbrella term of charge recovery logic (CRL). By recovering part of the charge from the load, these circuits achieve lower energy consumption with respect to static CMOS. Recently, a comparator that uses the principles of charge recovery was presented, introducing these energy advantages to the world of mixed-signal circuits. The original design has a maximum operating frequency of 1 kHz, and thus is limited to niche applications. In this work, an improved charge recovery comparator is introduced, operating at up to 900 MHz. Post-layout simulations in 65 nm technology show an energy consumption of 40 fJ per conversion, and an input offset voltage of 32 mV.

## I. INTRODUCTION

Charge recovery logic (CRL) is an active research topic for low-power applications, although it is still categorized as an emerging technology. There is a wealth of logic families that employ charge recovery principles [1], and GHz operation of charge recovery logic is demonstrated [2]. Though the principles behind charge recovery logic are well understood [3], they are relegated to digital circuits. The first mixed-signal circuit making use of charge recovery principles is presented in [4], in the form of a comparator, by the authors. The major limit of the design in [4] is the maximum operating frequency of 1 kHz. The comparator described here is capable of operating up to 900 MHz while maintaining an energy profile similar to the original design in [4].

The remainder of this article is organized as follows. Section II gives an introduction to charge recovery logic and its principles. Section III reviews the original charge recovery comparator and its limits. Section IV presents the improved charge recovery comparator. Section V shows post-layout simulation results of the proposed comparator. Section VI compares the proposed design with state-of-the-art circuits. Section VII concludes this work and highlights future research.

## II. CHARGE RECOVERY PRINCIPLES

The goal of this section is to give a general introduction to charge recovery logic and the principles that are salient to the discussion in this paper. For a more in-depth analysis of such topics, the reader is referred to [3], [5].

Charge recovery logic aims at reducing the energy consumption of a logic gate by recycling the charge delivered to the load. In a static CMOS gate, a  $1 \rightarrow 0$  transition of the output

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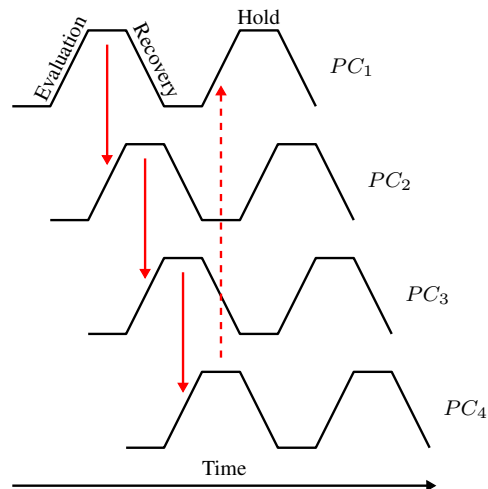


Fig. 1. The configuration of the power-clock signals of a charge recovery logic system. Each of these signals is also referred to as a power-clock phase.

node necessarily means that the charge of the load capacitance is discharged to ground. Charge recovery logic is designed to recover the charge from the output node and transfer it back to the power source. If the power source is capable of recycling this charge, the overall energy consumption is reduced. The most common way of achieving this transfer of energy is through the use of a power-clock. The power-clock is a periodic signal that goes from 0 to  $V_{DD}$  every cycle, delivering energy and timing to the charge recovery logic gates.

For the sake of simplicity, consider the power-clock to be trapezoidal, as shown in Figure 1. While the power-clock is rising, the logic gates driven by it are in the *evaluation segment*: The boolean function implemented by a CRL gate is being evaluated during this time. At the end of the evaluation segment, the CRL gate output is at the correct logic level. When the power-clock is falling, the logic gates driven by it are in the *recovery segment*: The charge that is on the load capacitance of a CRL gate is sent back to the power-clock source. When the power-clock is high, the term *hold segment* is used. Because of the charge transfer back to the power-clock source, the output of a CRL gate goes low during the recovery segment. Consequently, the output is valid only during the hold segment. The hold segment must be synchronized to the evaluation segment of the next logic gate,

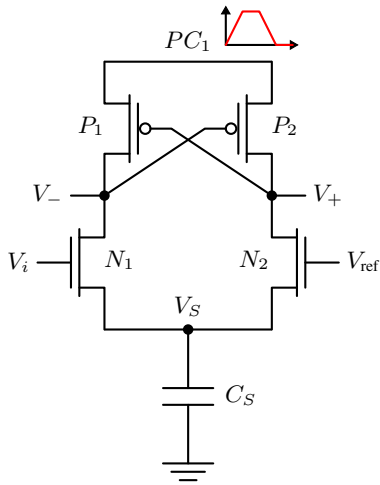


Fig. 2. The original charge recovery comparator introduced in [4].

hence another power-clock signal is needed that  $90^\circ$  out of phase with the initial power-clock signal. This principle is illustrated in Figure 1, where four  $90^\circ$  shifted signals are pipelined with a single power-clock cycle. The power-clock signals  $PC_1$ ,  $PC_2$ ,  $PC_3$ , and  $PC_4$  are usually called *phases* of the power-clock, and the terms *phase* and *power-clock* are used interchangeably throughout the literature. With these four phases of the same trapezoidal signal, an unlimited amount of gates can be cascaded: a logic gate powered by  $PC_1$  drives a gate powered by  $PC_2$ , which in turn drives a gate powered by  $PC_3$ , which drives a gate powered by  $PC_4$ , which can now drive a gate powered by  $PC_1$ , and so on. It is important to note that data moves through four power-clock phases in exactly one power-clock period, as exemplified by the dashed red arrow in Figure 1. The four-phase charge recovery configuration is used in many charge recovery logic families, including ECRL [6]. ECRL is a simple CRL family on which the original charge recovery comparator is based on [4].

In practice, it is difficult to design a trapezoidal power-clock source [3], thus most CRL circuits use sinusoidal signals as power-clock phases. Two LC-tank oscillators, connected in a quadrature configuration [7], are capable of generating four sine-waves with the required  $90^\circ$  out of phase characteristics. Intuitively, the energy is recovered from the logic gates by the inductance, as part of the LC oscillation. This setup is widely used in charge recovery logic circuits and it is reported to achieve efficiencies of up to 90% [8].

### III. REVIEW OF EXISTING COMPARATOR

The original charge recovery comparator, introduced in [4], is shown in Figure 2. A sampling cycle goes as follows. Initially the power-clock  $PC_1$  and the outputs  $V_+$  and  $V_-$  are at zero. Voltage  $V_S$  is at zero as well. During the evaluation segment, i.e. when  $PC_1$  rises, transistors  $P_1$  and  $P_2$  start to conduct, because their gate voltages are low. Assuming that  $V_i$  and  $V_{ref}$  are larger than the NMOS threshold voltage,

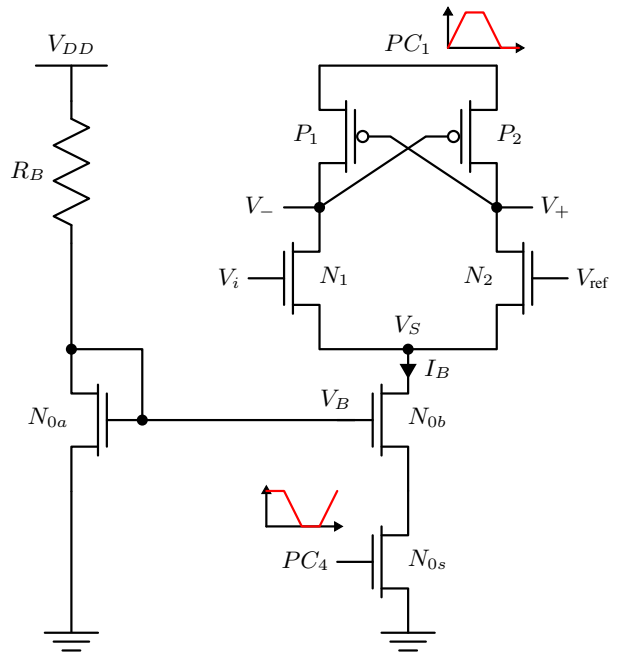


Fig. 3. The proposed charge recovery comparator

transistors  $N_1$  and  $N_2$  start to conduct as well. The difference between  $V_i$  and  $V_{ref}$  results in a difference in the currents through  $N_1$  and  $N_2$ , which is amplified by the cross-connected transistors  $P_1$  and  $P_2$ . This is similar to the action of a sense amplifier, or a latched comparator [9]. During the recovery segment, the charge on the output loads goes back to the power-clock  $PC_1$ , through transistors  $P_1$  and  $P_2$ . Capacitor  $C_S$  holds a residual charge that cannot be completely removed through  $N_1$  and  $N_2$ . The circuit of Figure 2, thanks to the capacitor  $C_S$ , maintains the source of  $N_1$  and  $N_2$  at  $V_S \approx V_{ref} - V_{TN}$ , where  $V_{TN}$  is the threshold voltage of the NMOS transistor. This characteristic allows the circuit to accommodate a large common mode input voltage range, without consuming too much energy [4]. The major drawback of such an implementation is that the current that is divided between transistors  $N_1$  and  $N_2$  depends, in a non-trivial way, on a combination of  $C_S$ ,  $V_{REF}$ , operating frequency, and transistors sizing. This makes it difficult to design the comparator of Figure 2 for a given set of specifications.

### IV. PROPOSED COMPARATOR

To overcome this limitation, the proposed comparator of Figure 3 is introduced. It is similar to the original comparator, with the addition of transistor  $N_{0b}$  acting as a current source. This effectively creates the differential pair that is ubiquitous in analog design [10]. Transistors  $N_{0b}$  and  $N_{0a}$  are in the well-known resistive current-mirror configuration [10], but the source of  $N_{0b}$  is connected to transistor  $N_{0s}$  rather than to ground. Transistor  $N_{0s}$  simply act as a switch, and it is driven by the power-clock phase that is  $-90^\circ$  out of phase with respect to  $PC_1$  (i.e. in phase with  $PC_4$ ). Therefore, the peak of

TABLE I  
TRANSISTOR DIMENSIONS

	$N_{0a}$	$N_{0b}$	$N_{0s}$	$N_1 = N_2$	$P_1 = P_2$
W ( $\mu\text{m}$ )	1	40	10	1	1.6
L ( $\mu\text{m}$ )	0.1	0.1	0.06	0.06	0.06

the bias current  $I_B$  is during the evaluation segment of  $PC_1$ . A sampling cycle of the proposed comparator is described as follows. Initially, the power-clock  $PC_1$  and the outputs  $V_+$  and  $V_-$  are at zero. Since  $PC_4$  is high,  $N_{0s}$  is fully on and acts as a closed switch, connecting the source of  $N_{0b}$  to ground. Because  $PC_1$  is at zero, there is no current that goes through  $N_{0b}$ . During the evaluation segment, transistors  $P_1$  and  $P_2$  start to conduct. Assuming that  $V_i$  and  $V_{\text{ref}}$  are large enough, transistors  $N_1$  and  $N_2$  start to behave as a differential pair, thanks to  $N_{0b}$  acting as a current mirror. The difference between  $V_i$  and  $V_{\text{ref}}$  is amplified by the cross-connected transistors  $P_1$  and  $P_2$ . During the hold segment of  $PC_1$ , the power-clock  $PC_4$  goes low, and  $N_{0s}$  is turned off. During the recovery segment, the charge on the output loads can only go back to the power-clock  $PC_1$  through transistors  $P_1$  and  $P_2$ , because  $N_{0s}$  is acting as an open switch. The fact that  $N_{0s}$  is on during the evaluation segment allows the current mirror to precisely control the bias current  $I_B$ . The maximum operating frequency can be now controlled, as in a normal differential pair, by the bias current. Assuming that the on resistance of  $N_{0s}$  is negligible, the minimum common voltage of the inputs is given by

$$V_{\text{CM,min}} = V_{\text{OV}} + V_{\text{TN}} \quad (1)$$

where  $V_{\text{OV}}$  is the overdrive voltage of transistor  $N_{0b}$  and  $V_{\text{TN}}$  is the threshold voltage of the NMOS transistors.

## V. EXPERIMENTAL RESULTS

The comparator of Figure 3 is implemented in a 65 nm standard CMOS technology, with the transistor sizes reported in Table I, and simulated using Cadence Spectre. The layout of the comparator, shown in Figure 4, has an area of about  $48 \mu\text{m}^2$ . In order to be well matched, transistors  $N_1$  and  $N_2$ , and transistors  $P_1$  and  $P_2$  are interdigitated, and each pair is inside a guard ring. Post-layout simulations shows that with a resistance  $R_B = 800 \text{ k}\Omega$ , the peak of  $I_B \approx 35 \mu\text{A}$ , which allows the comparator to operate at up to 900 MHz.

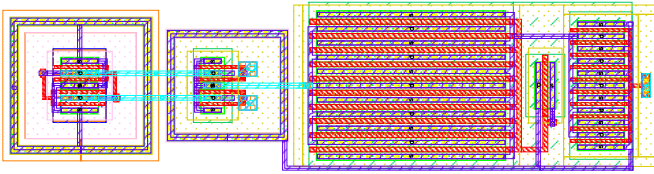


Fig. 4. The layout of the proposed comparator of Figure 3. On the left side are the two guard rings for  $P_1$ ,  $P_2$  and  $N_1$ ,  $N_2$ , while on the right side is the current mirror:  $N_{0a}$ ,  $N_{0b}$ , and  $N_{0s}$ .

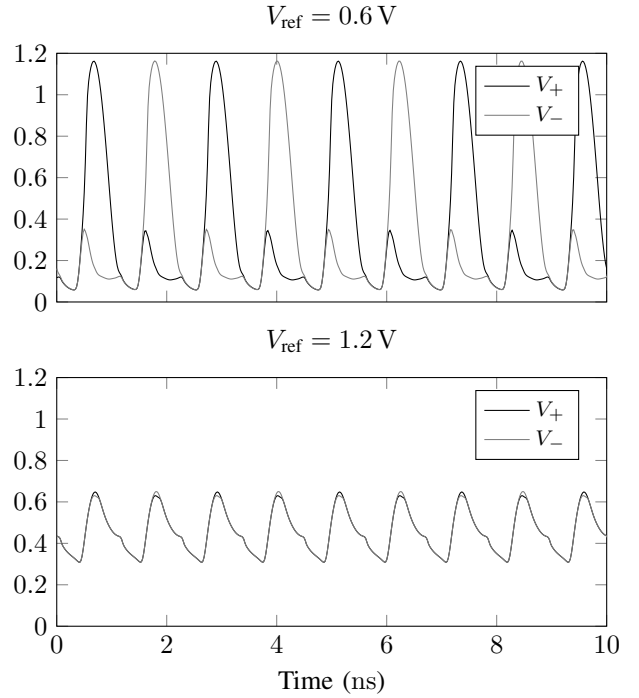


Fig. 5. The output of the comparator for different reference voltages  $V_{\text{ref}}$ , at 900 MHz and with an input  $V_i = V_{\text{ref}} \pm 5 \text{ mV}$ .

Because of the topology of the proposed comparator, the output swing is greatly affected by the reference voltage  $V_{\text{ref}}$ . For example, Figure 5 shows the outputs of the comparator operating at 900 MHz, for different reference voltages. In both cases, the input  $V_i$  is switched every power-clock period to be 5 mV higher or lower than  $V_{\text{ref}}$ . For  $V_{\text{ref}} = 0.6 \text{ V}$ , the differential voltage at the output,  $V_+ - V_-$ , is  $\approx V_{\text{DD}}$ , while for  $V_{\text{ref}} = 1.2 \text{ V}$ , the output differential voltage is only 25 mV.

The signals of Figure 5 are not suitable to drive an ECRL logic gate, especially not when  $V_{\text{ref}} = 1.2 \text{ V}$ . In order to further amplify the outputs of the comparator, a second comparator and an ECRL buffer are cascaded, as shown in Figure 6. Because there are four power-clock phases and the comparator of Figure 6 has three stages, the data has a latency of less than one power-clock period. This fact makes the proposed comparator suitable for ADC architectures that have feedback, for example a successive approximation ADC [9].

Figure 7 shows the instantaneous energy consumption of comparators  $C_1$  and  $C_2$  of the circuit of Figure 6. The wave-

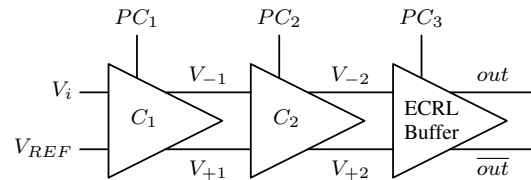


Fig. 6. The configuration of the 3-stage comparator. Both  $C_1$  and  $C_2$  are the comparator of Figure 3, while the last stage is an ECRL buffer.

TABLE II  
POWER CONSUMPTION OF THE 3-STAGE COMPARATOR, IN  $\mu\text{W}$

$V_{\text{ref}}$	ss	sf	tt	fs	ff	Average
0.6 V	23.3	22.4	24.5	26.8	25.8	24.6
0.8 V	27.6	26.6	29.8	34.7	33.0	30.4
1 V	35.5	34.2	40.6	46.8	46.2	40.7
1.2 V	44.3	44.5	49.7	52.9	54.9	49.2
Average	32.7	31.9	36.1	40.3	40	<b>36</b>

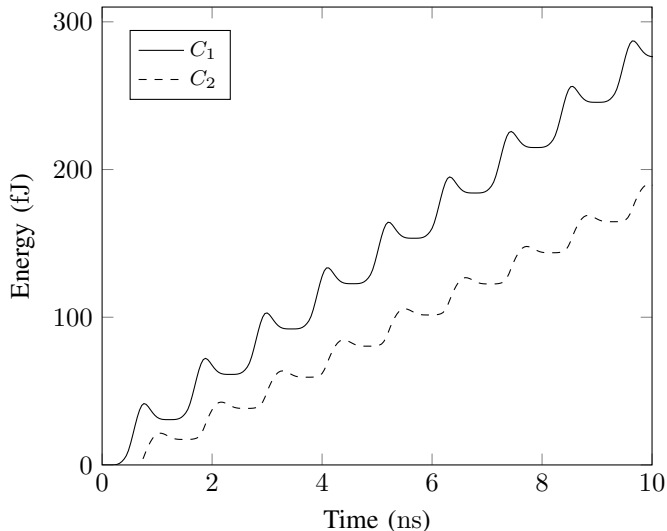


Fig. 7. The energy profiles of the comparators of the simulated circuit of Figure 6, operating at 900 MHz, with  $V_{\text{ref}} = 1.2\text{ V}$  and  $V_i = V_{\text{ref}} \pm 5\text{ mV}$ .

forms of Figure 7 show the typical profile of charge recovery logic [6], [11], demonstrating that the proposed comparator of Figure 3 achieves energy recovery under different conditions.

The power consumption of the post-layout 3-stage comparator of Figure 6 is reported in Table II, when operated at 900 MHz, across process corners and input common mode voltages,  $V_{\text{ref}}$ . The input voltage is  $V_i = V_{\text{ref}} \pm 5\text{ mV}$  for all the values of Table II. On average, the power consumption at an operating frequency of 900 MHz is  $36.2\text{ }\mu\text{W}$ . The energy per conversion is  $36.2\text{ }\mu\text{W}/900\text{ MHz} = 40\text{ fJ}$ . To guarantee operation across corners, a minimum  $V_{\text{ref}}$  of 0.6 V is needed. Such a requirement can be expected from Equation 1, and stems from the chosen differential-pair topology. The input common-mode voltage range results in  $V_{\text{DD}} - V_{\text{CM,min}} = 0.6\text{ V}$ .

In order to evaluate the input offset voltage of the proposed comparator, the method explained in [12] is applied to the circuit of Figure 3, and the results are shown in Figure 8. The resulting offset voltage, assuming a correlation coefficient of 0.75 for matched transistors, is roughly 32 mV for a  $3\sigma$  confidence interval.

## VI. COMPARISON WITH STATE-OF-THE-ART

Table III presents a comparison of the proposed 3-stage comparator with a few state-of-the-art comparators [13]–[15]. The proposed design has a lower energy per conversion figure

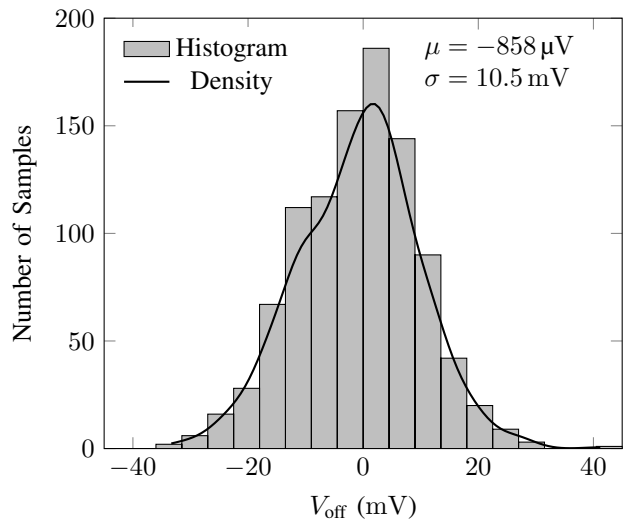


Fig. 8. Histogram and extracted density of the input offset voltage of the proposed comparator, as resulting from a 1000 runs monte carlo analysis, at 900 MHz, with  $V_{\text{ref}} = 0.6\text{ V}$ , and with a correlation coefficient of 0.75 for matched transistors.

TABLE III  
LITERATURE COMPARISON

	[13]	[14]	[15]	Proposed
Technology (nm)	65	65	120	65
Voltage (V)	1.2	1	0.5	1.2
$V_{\text{CM}}$ Range (V)	0 – 1.2	—	0 – 0.5	0.6 – 1.2
Frequency (MHz)	1800	4000	600	900
Power ( $\mu\text{W}$ )	252	455	18	36.2
Offset (mV)	5.8	3	57	32
Energy per Conversion (fJ)	140	114	30	40

of merit than state-of-the-art comparators, except for [15]. The design in [15] employs a supply voltage of 0.5 V, when the nominal voltage of that technology node is 1.5 V, hence reducing the common-mode input range by 2/3. Moreover, the proposed comparator has an input offset voltage of 32 mV, which is lower than the 57 mV reported in the design in [15].

## VII. CONCLUSION

This paper presents a low-power charge recovery comparator implemented in a bulk CMOS 65 nm technology, with a maximum operating frequency of 900 MHz. Post-layout simulations show that the comparator consumes, on average, 40 fJ per conversion. The proposed design accepts inputs in the range of 0.6 V to 1.2 V, and outputs a full-swing signal compatible with ECRL logic, with an input offset voltage of about 32 mV. Though the proposed comparator presents a promising energy profile, further research is needed to fully evaluate its true benefits and limits. In particular PVT resilience and noise characteristics are to be fully investigated. Moreover, a charge recovery comparator designed with rail-to-rail input capabilities is needed to make this new category of circuits competitive with state-of-the-art solutions.

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