A Wirelessly Powered System with Charge Recovery Logic

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***Abstract*—In this paper, charge recovery logic is proposed as an alternative to traditional or near-threshold CMOS logic for circuit systems where the power is wirelessly delivered, e.g. bio-implantable devices. This approach has two primary, complementary advantages in i) providing a wirelessly transmitted sine-wave as the power clock source to the charge recovery logic and ii) eliminating the AC/DC power stage required to provide a stable supply voltage needed in CMOS circuits. Solutions are presented to the main obstacles of this method, demonstrated with simulation results of a simple logic load designed in Efficient Charge Recovery Logic (ECRL). The designed wirelessly powered ECRL (coined WP-ECRL) system i) consumes 15.2× less power than full-swing CMOS and ii) operates at higher frequencies than near-threshold CMOS. These comparative trends in power dissipation are for the computing circuit only, and do not include the AC/DC stage that would be necessary for CMOS implementations. In terms of resilience, it is shown that logic functionality is preserved even when the coupling coefficient of the wireless link is decreased by 60% from the nominal value or when coils with very poor quality factor (down to $Q = 0.1$) are used.**

I. INTRODUCTION

Low power consumption is important in every electronic application, from supercomputing to mobile devices. Some applications, e.g. bio-implantable devices, not only have a strict power budget but also may require wireless power delivery. Although static CMOS logic, particularly when used in sub- or near- threshold, can be successfully used for such tasks, its main disadvantage is that it operates with a DC voltage. This means that a rectifier and regulator are necessary to convert the wirelessly delivered AC power to DC [1]. Even assuming an ideal wireless link, the conversion stage leads to a energy loss [2]. Moreover, in those applications where processing capabilities are important, e.g. image processing, sub-threshold CMOS logic is not feasible due to the frequency trade off used to minimize energy [3].

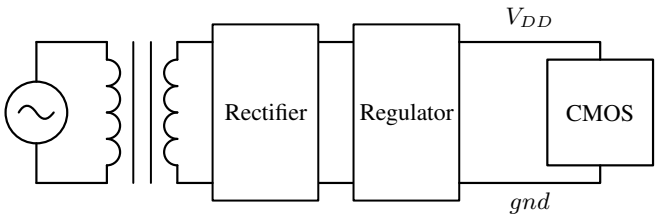
In this work, a solution is proposed that i) replaces CMOS with charge recovery logic, and ii) eliminates the rectifier and regulator, i.e. the AC/DC conversion stage. The idea is to use charge recovery logic [4], or CRL, instead of CMOS, since the former offers two advantages over the latter: i) operating with sine-waves rather than DC voltage and ii) dissipating less power. The sine-wave received from the RF link directly powers the CRL block, eliminating losses due to the AC/DC conversion necessary for CMOS circuits (i.e. for a DC supply voltage V_{DD}) and serves as a native power clocking source for CRL (i.e. eliminating the need of a local LC oscillator to generate a sine-wave power-clock signal). Moreover, CRL is inherently pipelined [5], hence eliminating the need for timing analysis.

The proposed solution is a novelty in the use of inductive link, as well, because, unlike a traditional inductor link implementation [6], the power is not transmitted at the resonant frequency. Instead, a non-resonant frequency is selected to prevent high variations in recovered voltage magnitude. Simulation results for a demonstrative circuit designed in Efficient Charge Recovery Logic (ECRL) [7] versus a static CMOS are presented for comparison of power dissipation and operating frequencies. The focus of the analysis is twofold for CMOS and near-threshold CMOS: 1) At high frequency, only traditional CMOS is feasible but with 15.2× more power consumption; 2) At low frequency, near-threshold CMOS is feasible to match the power savings of the charge-recycling at the logic component, however, still needing a rectifier and regulator. The proposed system is superior in delivering high performance wirelessly powered system performance, and no worse than a near threshold implementation at a low performance, low frequency operation mode. The drawback of the system is the need to use two inductive coils, as opposed to one. The overhead of an additional coil is considered not prohibitive, as a very low quality factor (i.e. as low as $Q = 0.1$) is shown to be sufficient for inductive coupling in the proposed system. The proposed implementation of a wirelessly powered ECRL system is coined WP-ECRL in this work.

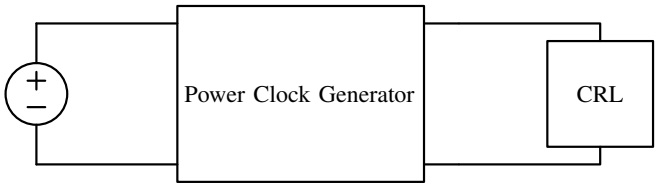
The paper is organized as follows. Section II describes the limitations of the traditional approach in wireless power delivery for CMOS-logic-based systems. Section III is a theoretical analysis of the undesirable effects of resonance, leading to the novelty in off-resonance operation in this work. Section IV highlights the main differences between the logic component design methodology of this work and traditional CRL and CMOS solutions. Section V describes the proposed WP-ECRL system and presents initial simulations to show the feasibility of the method. Section VI tackles the resilience impact of non-ideal coupling coefficient k and quality factor Q.

II. TRADITIONAL APPROACH

Typical wirelessly powered systems are composed of an inductive link power supply that powers up a CMOS circuit implementation. Figure 1(a) shows a simplified block diagram of an inductive link power supply, typically used in implantable medical devices [8]. For these applications only



(a) A typical wirelessly powered system built with an inductive link power supply, and CMOS as the logic component



(b) A traditional DC powered CRL system with a power clock generator

(c) The proposed solution

Fig. 1. Differences between CMOS and CRL traditional approaches and the proposed solution.

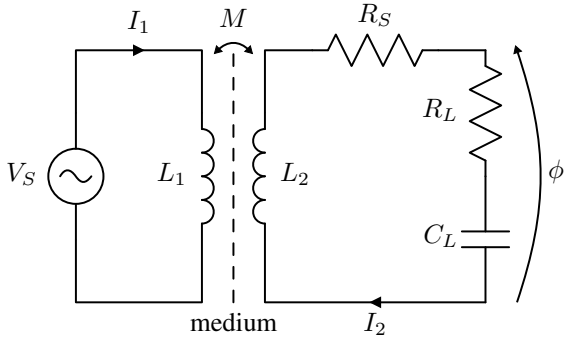


Fig. 2. The schematic of the proposed wirelessly powered system. The dashed line separates the power source, on the left, from the low-power circuit, on the right side. R_L and C_L represent the equivalent circuit of the CRL, R_S the parasitic resistance of inductor L_2, and ϕ the power clock.

the right-hand side of the system must be low-energy, so not to raise the temperature of the tissues hosting the device. To this end, this work focuses on reducing the energy consumption of the low-power portion of the system, i.e. the receiver side. The inductive link power supply of Figure 1(a) has a voltage source in the transmitter side. On the receiver side are an inductive link and the power conversion system, composed of the rectifier and regulator, to generate the DC voltage necessary for the CMOS logic component. State of the art rectifiers can have power efficiencies up to $90\,\%$, although this percentage depends on the input voltage [2], [9], hence on the quality of the wireless link. State of the art regulators present up to $90\,\%$ power efficiency as well, depending on the output voltage [10]. Consequently, a well designed power conversion system can have up to $0.9 \cdot 0.9 = 0.81$ power efficiency, meaning that roughly $20\,\%$ of the transferred power is dispersed as heat instead of being delivered to the load.

In the proposed WP-ECRL system, the CMOS logic is replaced by a charge recovery logic (with the same functionality). A typical CRL logic schematic is illustrated in Figure 1(b). The big differentiating factor from CMOS is the voltage and synchronization source of the CRL logic, which is called the power-clock ϕ. The power-clock is a sine-wave shaped signal that supplies the power source to the CRL logic, as well as synchronizing the operation of phases for the CRL logic. Figure 1(c) is a simplified schematic of the proposed solution, representing the circuit of an inductive link with a charge recovery logic load. It can be seen in Figure 1(c) that there is no rectifier and regulator nor is there a separate power-clock generator, as required in the traditional approach depicted in Figure 1(b). Instead, the incoming sinewave is directly fed to the CRL logic. In this manner, the conversion efficiency in the low-power circuit is (ideally) $100\,\%$. This represents an advantage over the traditional approach of Figure 1(a) in terms of conversion loss ($100\,\%$ vs $81\,\%$ efficiency) and implementation overhead (eliminating the rectifier, regulator, and the power clock source).

III. THEORETICAL ANALYSIS OF THE RESONANCE

One main obstacle to the proposed WP-ECRL system is that the magnitude of the transmitted voltage is susceptible to variations of the inductive link, when the system is used at the resonant frequency. This obstacle is solved through operating the inductive coil at a non-resonant frequency. Note that this is a non-typical operation, as the resonant frequency for the typical CMOS system of Figure 1(a) is the highest mode for power transfer [6]. Since this work focuses on reducing the energy consumption of receiving side of the system, overall power transfer is not a concern. Non-resonant frequency assures that the magnitude of the recovered voltage does not spike under variations of the inductive coupling.

Figure 2 is a simplified schematic of the proposed system. On the left side is the external apparatus, a voltage source and a coil. On the right side is the low-power part of the system: a coil and a simple equivalent circuit for the CRL block [11]. The resonance is formed through the inductor and the effective capacitance of the CRL circuit. This resonance is desirable in a CMOS circuit that is wirelessly powered, as the AC/DC conversion can regulate the (high) recovered voltage. However, in the absence of a regulator for the proposed CRL logic implementation, an increased voltage, i.e. due to RF link variations, could irreversibly damage the circuitry. In the following mathematical discussion, the parasitic resistance R_S of the coil is assumed to be zero, for the sake of simplicity (R_S will be reintroduced in Section VI for resilience analysis). In order to derive expressions that are useful for the resonant

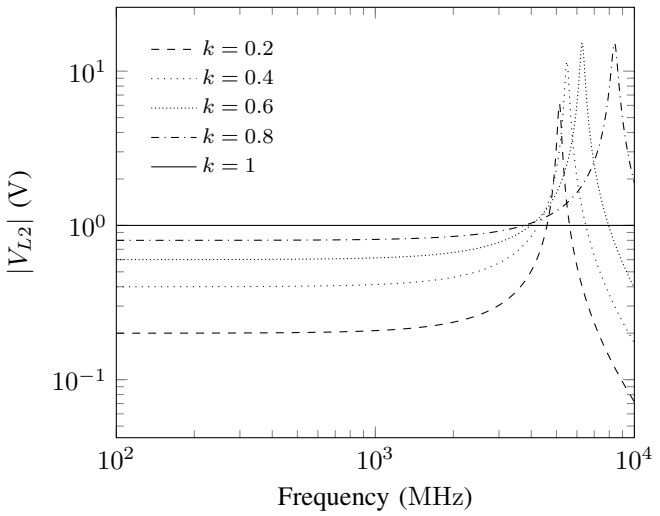


Fig. 3. Equation (2) plotted when $L_1 = L_2 = 100\,\text{nH}$, $C_L = 10\,\text{fF}$, $R_L = 100\,\Omega$, $R_S = 0$, and $V_S = 1\,\text{V}$. Note that for decreasing k the resonance frequency of the system gets closer to $1/2\pi\sqrt{L_2 C_L} \approx 5\,\text{GHz}$. Moreover, as expected from Equation (2), $V_{L2} \approx kV_S$ for frequencies well below the resonance.

frequency analysis, consider the Kirchhoff's equations in the Laplace domain for the circuit of Figure 2:

$$\begin{cases} V_{L1} = V_S \\ V_{L1} = sL_1 I_1 - sMI_2 \\ V_{L2} = -sL_2 I_2 + sMI_1 \\ V_{L2} = I_2\,(R_L + 1/sC_L) \end{cases} \tag{1}$$

where V_{L1} and V_{L2} are the voltages of inductors L_1 and L_2, respectively, R_L and C_L are the linear representation of the charge recovery logic, $M = k\sqrt{L_1 L_2}$ is the mutual inductance of the two coils, and $R_S = 0$. The solution of the system for the voltage V_{L2} on inductor L_2 is

$$V_{L2} = V_S \sqrt{\frac{L_2}{L_1}} \frac{k(sC_L R_L + 1)}{s^2 L_2 C_L (1 - k^2) + sC_L R_L + 1}. \tag{2}$$

An analysis of Equation (2) reveals that:

- L_1 does not show up in the poles of the system,
- the resonance is at $\omega_0 = 1/L_2 C_L (1 - k^2)$,
- for $k = 1$, the system does not resonate.

Equation (2) is plotted for different values of k in Figure 3. For frequencies well below $1/2\pi L_2 C_L (1-k^2)$, i.e. 5 GHz, the voltage V_{L2} has a smooth behavior. Analytically, Equation (2) can be rewritten assuming $L_1 = L_2$ and $f \ll 1/2\pi L_2 C_L (1 - k^2)$ to get

$$V_{L2} = kV_S. \tag{3}$$

In other words, well below the resonant frequency of the system, the voltage V_{L2} does not depend on frequency. This non-resonant range is the selected frequency range of operation for WP-ECRL, where a rectifier/regulator stage is not necessary and the recovered voltage level is sufficient for ECRL operation (unlike the high values necessary for CMOS).

IV. Differences with Traditional Power Clocking

Charge-recovery logic circuits are powered by a power-clock, which is ideally a sine wave that serves to synchronize the operation as well as provide the power supply to the circuit [5]. The power clock in traditional CRL systems can be built using either a capacitor or an inductor to store the recycled charge. Although special circuits, e.g. stepwise driver, can be used to transfer charge from a capacitor to another [12], the most common approach is to use one or more inductors to build a resonator [13]–[15]. The goal of this resonator is to convert the commonly available DC source to sine-waves to use as power clocks. Difficulties arise because the poor performance of integrated inductors does not allow to build high-Q resonators, and the best reported power efficiencies are around 77 % [16]. The proposed method does not rely on an additional circuitry to provide the power clock signals, thanks to the wirelessly transmitted power illustrated in Figure 2. The inductor L_2 effectively becomes an AC voltage source and the only power dissipation on the receiving side is due to the circuit load resistor R_L and the inductor parasitic resistance R_S. The circuitry overhead for power clock generation that is present in traditional CRL designs is opportunistically eliminated. Moreover, traditional inductive power transmission systems rely on the tuning of two LC-tanks in order to reach optimal efficiency [6]. The consequence is that a change in the load seen by the RF link, for example due to power gating, would affect the overall power efficiency. The proposed approach does not face this problem due to not operating under resonance conditions.

V. WP-ECRL

The wirelessly powered ECRL system proposed in this work, coined WP-ECRL, is analyzed in multiple facets. First, the amenability of a CRL logic family, ECRL [7], for the proposed WP-ECRL system is demonstrated. Next, a system level view of WP-ECRL is analyzed, demonstrating implementation specifics of using two sets of inductors, unlike the generic case in Figure 2. Finally, simulations of the system are compared to the incumbent CMOS logic; a simple inverter chain was chosen for simplicity as a logic load for demonstration purposes. The goal of this experimentation is to demonstrate that charge recovery logic can be used in wirelessly powered systems, offering several advantages over CMOS. Details on designing complex CRL functions and datapaths is presented in references such as [5], and is not included here.

A. Circuit Level

The proposed solution provides all the well-known advantages of CRL over CMOS [5]. ECRL is specifically useful in the proposed work as this logic family does not need voltage references for its operation. This is useful for cases when the receiver and the transmitter sides do not share a common ground reference. The single ECRL inverter/buffer gate is represented in Figure 4, which also serves as a register due to power clock operation. Although the transistor overhead

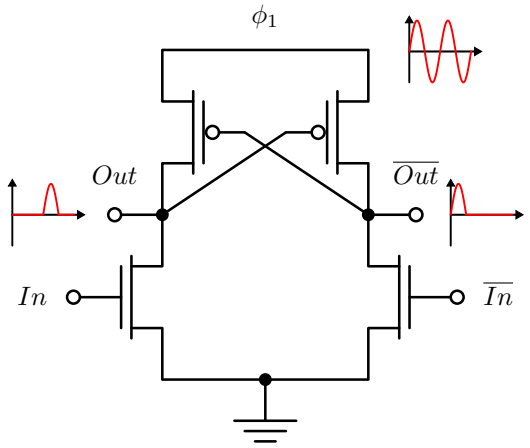


Fig. 4. The ECRL inverter/buffer used during the simulation.

is large in the case of a simple inverter, the transistor count and area are comparable if not better for more complex gates, e.g. the XOR [5]. Usually the power clocks for ECRL have a DC offset such that the ground of Figure 4 is the lowest point of ϕ_1. In order to produce this non-zero average power clock, a AC/DC stage would typically be necessary, defeating the purpose of this approach. The solution is to use sine-waves centered around zero as power clocks. As a consequence, there is no need for a AC/DC stage but a reduction in the output swing to half of the incoming voltage is observed, as shown if Figure 4. Note that this does not mean that each stage will reduce the input voltage to half of its value, hence it is perfectly possible to cascade gates, as demonstrated by the simulation of a 64-stage invert chain.

B. System Level

Figure 5 shows the proposed WP-ECRL. The system utilizes two external AC voltage sources for the generation of the four power clocks, ϕ_1, ϕ_2, ϕ_3, and ϕ_4. The voltage sources V_S and V_S' are $90°$ out of phase and each has a dedicated inductive link. The two coils on the right side of each link are configured such that their voltages are $180°$ out of phase, thus providing the four power clocks. As described in Section II, neglecting the parasitics of the inductors, there is no conversion loss in the low-power circuit, namely the right hand side of the WP-ECRL system of Figure 5. The power consumption is obtained by summing the integrals of the $v(t)i(t)$ products for the four inductors on the right side of the wireless link, and accounts for the ECRL block. As such, the simulated power consumption includes resistive power losses (i.e. over the R_L and R_S in Figure 2) and the leakage power at the selected technology node. The values for the power consumption are the same that are obtained when using an ideal voltage source in place of the inductive link, proving that there is no conversion loss in the low-power section of the WP-ECRL system.

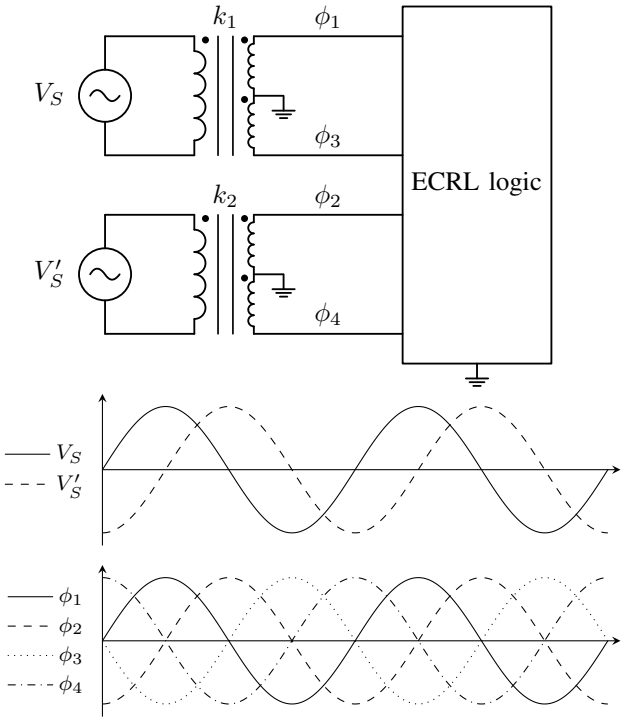


Fig. 5. The WP-ECRL system used during the simulation. The voltage supplies V_S and V_S' are $90°$ out of phase and have a dedicated RF link each. The two inductors on the right side of each link are configured such that their voltages are $180°$ out of phase, thus providing the four power clocks.

TABLE I
INVERTER CHAIN POWER CONSUMPTION

f (MHz)	WP-ECRL (nW)	CMOS (nW)	NTV-CMOS (nW)	CMOS (Normalized to WP-ECRL)	NTV-CMOS
10	58	732	52	12.6×	0.9×
50	174	2814	231	16.2×	1.3×
100	333	5417	457	16.3×	1.4×
500	1677	26240	—	15.7×	—
1000	3446	52270	—	15.2×	—
Average				15.2×	1.2×

C. Comparison against CMOS

As a proof of concept, the schematic of a 64-stage inverter chain is designed in both CMOS and ECRL using the NCSU $45\,\mathrm{nm}$ PDK and simulated with Spectre. These circuits will serve as loads for the systems of Figure 1(a) and Figure 5, respectively. Moreover, the CMOS circuit is also operated at a reduced V_{DD} in order to achieve near-threshold performance. The NTV-CMOS circuit was not optimized for minimum EDP [3] but rather operated in a power budget fashion: given roughly the same power budget as the WP-ECRL, the supply voltage V_{DD} was chosen as high as possible, namely $0.3\,\mathrm{V}$, without violating the budget. Minimum size transistors are used for simplicity and the reproducibility of the results.

The power consumption of the simulated circuits, with an activity factor of $100\,\%$ and $k_1 = k_2 = 1$, is presented in

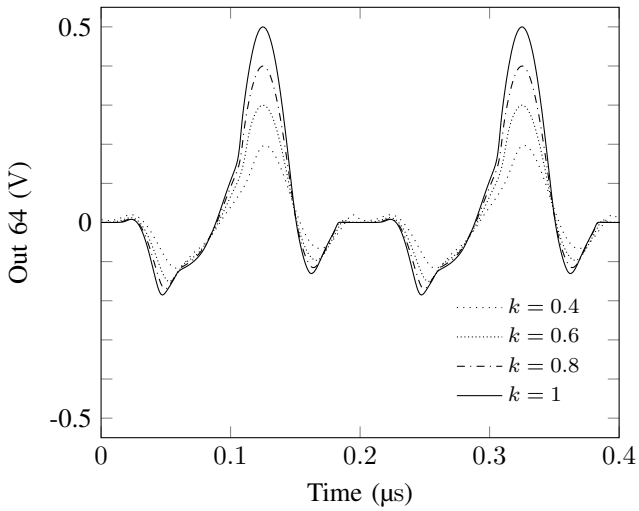


Fig. 6. The 64th output of the inverter chain of the system of Figure 5 with $k_1 = k_2 = k$, 100 nH inductors, and $V_S = 1$ V at 10 MHz with 100 % activity factor. For $k = 0.8$, $k = 0.6$, and $k = 0.4$ the output swing is reduced to 0.4 V, 0.3 V, and 0.2 V, respectively, in accordance to Equation (3).

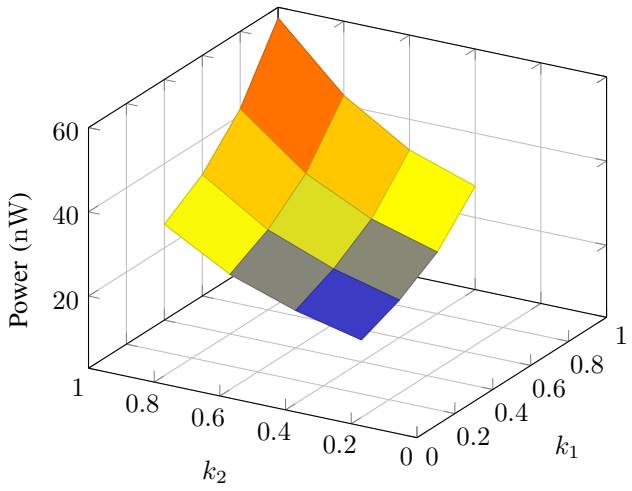


Fig. 7. Power dissipated by the WP-ECRL system of Figure 5 with 100 nH inductors and $V_S = 1$ V at 10 MHz with 100 % activity factor, under variation of the coupling coefficients k_1 and k_2. For coupling coefficients lower than 0.4, the system loses its functionality.

Table I. It is demonstrated that the WP-ECRL can deliver 15.2× power improvement over traditional CMOS, as well as delivering better frequency performance than NTV-CMOS. Table I also reports the normalized power consumption figures with respect to WP-ECRL, where it can be seen that the power savings of the proposed approach are reduced at low frequencies. This is due to leakage and it is a well-known limitation of the ECRL family [5]. Thus, the proposed technique is especially suited for relatively high frequencies. It is also important to reiterate that the reported numbers do not account for the AC/DC stage that would necessarily be present in CMOS implementations.

VI. Impact of Non-Ideal Conditions

The resilience properties of WP-ECRL are analyzed with respect to the variability of the wireless link coupling factor and the quality factor of the inductive inks.

A. Variability of the Wireless Link

Resilience is very important in many applications, e.g. in bio-implantable devices, where a change in alignment of the coils or tissue-related changes can impact on the coupling coefficient of the RF link [6]. Figure 6 shows the output of the 64th stage of the WP-ECRL inverter chain for different values of k. The functionality is maintained in each case, hence the system is reliable under variations of the coupling coefficient. In case of the proposed separate RF links for the two different sources V_S and V_S', the coupling coefficients might be dissimilar. Figure 7 shows the power consumption of the WP-ECRL system for varying k_1 and k_2, where it can be seen that functionality is maintained for coupling coefficients as low as 0.4. As anticipated from Equation (3), keeping away from the resonance guarantees that the voltage of the power clock decreases as the coupling coefficient k decreases.

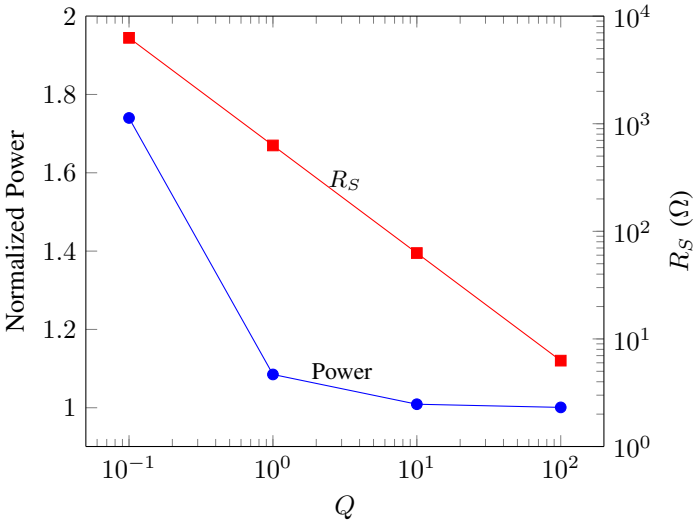


Fig. 8. Parasitic series resistance R_S and normalized power consumption for different values of Q when the system operates at 1 GHz. The power is normalized over the case when $Q = \infty$.

B. Effects of a Finite Q

In order to evaluate the parasitics of actual inductors, a series resistance R_S is added to each inductor of Figure 5, hence the quality factor Q of the coils is defined by the well known [6] equation

$$Q = \omega L / R_S. \tag{4}$$

A higher order parasitic analysis is possible such as the one in [6], but this simplified model is sufficient to highlight another key advantage of the proposed method: resilience from Q variations.

The impact of different values of Q is evaluated, in a range that extends to very pessimistic values ($Q = 0.1$). The

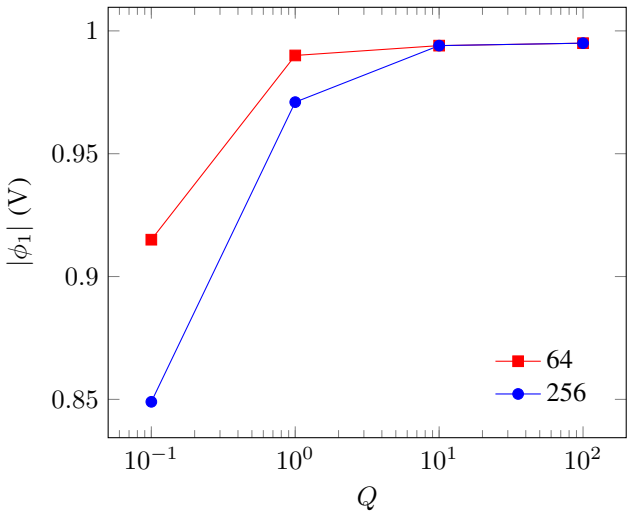


Fig. 9. Magnitude of the power clock ϕ_1 for different number of inverters as load, when the system operates at 1 GHz.

system of Figure 5 is simulated again at 1 GHz, and a non-zero R_S value is considered. Figure 8 shows values of R_S from Equation (4) for different values of Q and, as expected, R_S increases considerably as Q decreases ($R_S \approx 6\,\mathrm{k}\Omega$ when $Q = 0.1$). Observe in Figure 2 that the parasitic resistance R_S is in series with the equivalent resistance of the CRL block, R_L. Thus the parasitic resistance increases the real part of the impedance seen by L_2, which is acting as the power clock source. A higher resistive component implies a poorer charge recovery behavior or, in other words, a higher power consumption. The normalized power consumption of the system of Figure 5 with the 64 stage inverter-chain is also shown in Figure 8.

Strengthening the case for the practicality of WP-ECRL, the system maintains functionality even when $Q = 0.1$, a very pessimistic quality factor. This is possible because the proposed solution does not employ resonance to transfer power, hence a low Q only affects the magnitude of the power clocks. For example, the magnitude of the power clock, ϕ in Figure 2, can be derived simply by noticing that the circuit is a voltage divider. As expected, the power clock magnitude decreases as R_S increases. Figure 9 shows simulation results of the magnitude of the power clock $|\phi_1|$ for the system of Figure 5. The magnitude of the power clock also depends on the capacitive load, namely the number of logic gates. This important fact implies that the proposed system is functional even with poor quality inductors, such as on-chip integrated coils. Given an inductor with a certain quality factor Q, the load can be changed in order for the system to be functional.

VII. Conclusion

In this work, a wirelessly powered system that employs charge recovery logic is presented. Table II synthesizes the differences between the traditional approach of the CMOS system of Figure 1(a) versus the proposed WP-ECRL system of Figure 5. The suggested solution is 15.2× more power efficient compared to traditional CMOS and capable of operating at significantly higher frequencies than near-threshold CMOS. It is shown that if the inductive link has a drop of 60 % of its coupling coefficient, or very poor quality inductors are used (down to $Q = 0.1$), the WP-ECRL system maintains its functionality.

TABLE II
COMPARISON OF PROPOSED SOLUTION

	CMOS (Fig. 1(a))	WP-ECRL (Fig. 5)
Conversion Loss	≈ 20 %	0 %
Rectifier/Regulator	Yes	No
Load Independence	No	Yes
Link Independence	No	Yes
Q Independence	No	Yes
Single coil	Yes	No

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