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Education

Master of Science in Electrical Engineering
Drexel University — GPA:3.80/4.00
Philadelphia, PA — Graduation: June, 2011

Bachelor of Science in Electronics and Communication Engineering
Amrita School of Engineering — CGPA: 3.80/4.00
Bangalore, India — Graduated: April, 2009

Professional Experience

LSI Corporation — Allentown, PA
Read Channel Integration Team Intern — June, 2010 – Jan 2011

- Setup methodology for early power estimation that is being made part of the standard reporting structure. Reduced number of ECO's and whole design cycle as a result. The methodology developed here has been submitted and has received final acceptance and a presentation spot at SNUG San Jose 2011.
- Developing a JTAG Boundary Scan Chain - Using Synopsys design ware for the Read Channel IC and developing a test bench for the design too.
- Lint checks for various IP blocks using LEDA (Synopsys) and Spyglass (Atrenta).
- Characterizing the ViewDAC module to set a standard naming convention to support automated documentation of the same.
- Setup test methodology to use Power Artist (ApacheDA) to perform early power transient analysis, the methodology developed showed expected behavior. And is being evaluated for use in the standard design flow.
- Setup and ran formality for formal checks between different Synchronizer simulation and library models.

Texas Instruments Inc — Bangalore, India

Hardware Design Group Intern — January, 2009 – July, 2009

- Performed STA-Static Timing Analysis, Verification in order to achieve timing closure.
- Automated the process of using DC, PRIMETIME which is a highly iterative process.
- Optimized the Time required to achieve timing closure.

Research Experience

VLSI Lab, Drexel University — Philadelphia, PA

Graduate Student Research — Jan, 2011 – Present

- Evaluating existing techniques for Power Gird Analysis in IC design..
- Building a power grid analyzer (DC-Analysis) using C, Matlab interface
- Methodology and Flow development for the use of custom rotary clock oscillator in standard physical design flow (Design Compiler/ICC/Virtuoso) with the objective being high speed low power design.

Indian Institute of Science – IISc — Bangalore, India

Research Assistant at CSA - Computer Science and Automation Dept — April, 2008 – Sept, 2008

- Worked on Wireless Ad hoc Networks using game theory and mechanism design.

- Verified existing Algorithms - Developed at IISc on Network Simulator 2.
- Proof read the department's research work which was compiled into a research monograph and published by the department.

Relevant Course Work

EDA for VLSI	Microwave Engineering	CMOS integrated circuits
Special Topics VLSI	Electrical Circuit Theory	Physics of Semiconductors
Data Structures and Algorithms	Solid State Devices and Circuits	Low Power ASIC Design
Computer Architecture	Digital Design	Signal Processing

Publications

P.Vikram, S. Sharat Chandra, B.Sriram, "Fuzzy logic Based autonomous Navigation system", National Conference on Computer Vision, Artificial Intelligence and Robotics, Madras, India, Oct 3-6, 2007, Accepted.

Academic Projects

- Literature survey on adiabatic switching circuits for Low Power ASIC Design.
- Part of team at my university lab that sent a 500nm chip(rotary clock with Antennas) for manufacture - Involved creating Custom Schematic and Layout, Synthesis, Floor plan, Placement, CTS-Clock Tree Synthesis, Route and Parasitic Extraction. During this time explored the interoperability between Cadence and Synopsys tools.
- Programmed a C++ implementation of a BDD representation of Boolean function. Included ITE function for XOR, NAND and NOR.
- Executed complete RTL to GDSII flow for a SPARC processor - Using Synopsys Backend tools (DC/ICC-Star-RCXT/PT). Followed by detailed timing and power analysis using PrimetimePX.
- Programmed a Perl implementation of a SSTA to parse through a netlist and benchmark files to give us critical path information.
- Programmed a Perl Implementation of SAT solver using DPLL algorithm.
- Design Project, Amrita University, January to March, 2008 – "Defect Detecting Fully Autonomous BOT"' - Development of control algorithm for autonomous control of a BOT for use in diverse applications.

Tools and Skills

- Primetime,Primetime PX, Power Compiler, Design Compiler (DC), Integrated Circuit Compiler (ICC), Star RCXT, HSPICE, Nanosim and LEDA
- Spyglass-Lint Checker.
- Power Artist.
- Cadence Virtuoso.
- Network Simulator 2.
- NC Sim and Verdi.
- C, C++, Verilog, PERL and HTML.
- TCL, Clear Case, and LSF.
- UNIX, Sun Solaris and Windows OS's.

Honors, Awards and Affiliations

- Awarded Young student Support Program award - Design Automation Conference June 2010, Anaheim, California.
- Deans Scholar –Drexel University.
- IEEE School Secretary – During Undergraduate Studies(2007-2009)