Charge Recovery Logic for Thermal Harvesting Applications

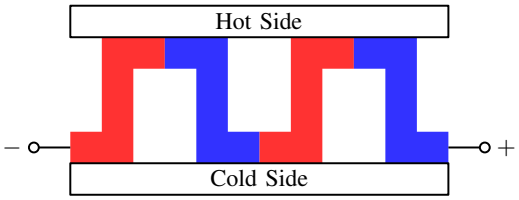
Leo Filippini and Baris Taskin
Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA 19104, USA
lf458@drexel.edu, taskin@coe.drexel.edu

***Abstract*—This paper investigates the substitution of CMOS or near-threshold CMOS with Charge Recovery Logic (CRL) in applications where energy is thermally harvested. By doing so, it is possible to eliminate the bulky DC/DC stage needed to provide the supply voltage for CMOS operation. Instead, a simple LC-tank oscillator is used to generate a power-clock suitable for CRL operation. Simulation results of a 256-stage inverter chain designed in Efficient Charge Recovery Logic (ECRL) are presented. Two additional novelties are presented i) using ECRL at a near-threshold voltage and ii) generating the four-phase power-clock by means of a quadrature oscillator. The traditional, full-swing CMOS system dissipates 18.2× the power dissipated by the proposed TP-ECRL system.**

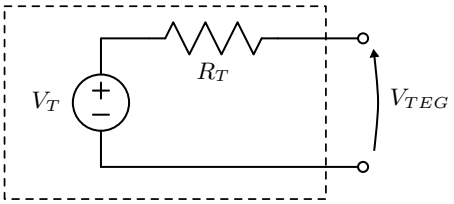
I. Introduction

In recent years, thermal harvesting has gained interest for low power applications [1] and as a way to recycle some of the power dispersed as heat by a system [2]. The majority of circuits are built with CMOS logic, which require a constant DC source. Near-threshold operation of CMOS, labeled NTV-CMOS in this paper and a popular choice in energy harvested circuit systems, also requires a DC source. The stable DC voltage must be produced from the *Thermo-Electric Generator*, or TEG. A simplified model for a TEG, also known as Seebeck generator, is represented in Figure 1. TEGs work similarly to a thermocouple, generating a small voltage in response to a temperature gradient. As an example, for a $2\,\mathrm{K}$ temperature gradient, a TEG can output up to $50\,\mathrm{mV}$ and present an equivalent thermal resistance R_T of $10\,\Omega$ [3]. Such a voltage is too low to directly power a near-threshold CMOS, let alone full swing CMOS. Stacking up many TEGs does increase the output voltage, as one would expect, however with the drawback of a larger R_T, which in turn causes problem of power transfer. In order to avoid this problem, DC/DC converters are used to boost the voltage across the TEG to a higher voltage [4], [5]. These solutions are an active research area however currently suffer from low efficiency or a large area overhead.

In this work, the use of *Charge Recovery Logic* [6], or CRL, in place of CMOS is proposed in order to i) reduce the power dissipated by the logic block and ii) eliminate circuitry for improved power efficiency and area savings. This is similar to the previous work in [7] for wirelessly powered WP-ECRL, where wireless harvesting is used as the power-clock signal and ECRL is used to replace the CMOS circuitry.



(a) Physical model: two different metals or semiconductors are connected in series such that their junctions are at different temperatures. The temperature gradient generates a potential difference between the two materials.



(b) The Thévenin equivalent, where V_T and R_T are the thermal voltage and thermal resistance, respectively.

Fig. 1. A thermoelectric generator, TEG, also known as Seebeck generator.

Many CRL families employ sinusoidal power-clock signals (i.e. for both power delivery and timing), and are known to offer lower power consumption with respect to CMOS [8]. It is shown in this paper that this sinusoidal power-clock signal can opportunistically be used to eliminate the DC/DC stage at the output of the TEG. In order to demonstrate this novel implementation, a particular CRL family is selected for simplicity. The logic family used here is *Efficient Charge Recovery Logic* [9], or ECRL, which is driven by a four phase power-clock. The simple LC-tank oscillator typically used for thermal harvesting applications [4], [5] is not capable of generating four sinewaves $90°$ out of phase. The use of a LC-tank based quadrature oscillator [10] as a power-clock is proposed in this paper for the first time.

In brief, this paper describes the use of LC-tank based quadrature oscillator powered ECRL logic for thermal energy-harvested circuits. This new methodology is named TP-ECRL,

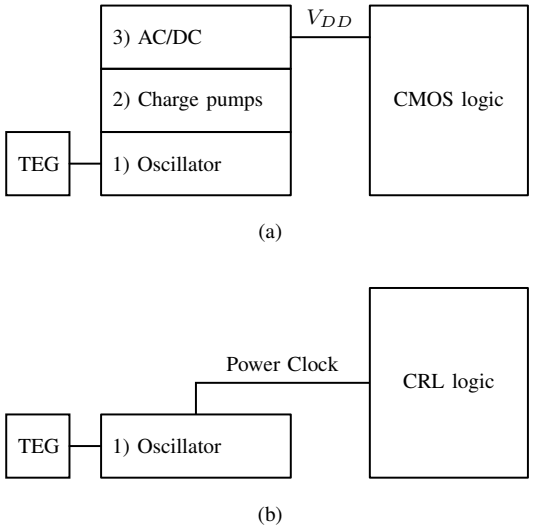


Fig. 2. Differences between a typical thermal harvesting CMOS system (a) and the proposed solution (b).

and leads to power consumption improvements over the incumbent CMOS logic, as well as area savings. The CMOS implementation consumes 18.2× the power of the TP-ECRL. The traditional thermal harvesting approach is explored in Section II. TP-ECRL is described in Section III. The design of the quadrature oscillator and simulation results of a TP-ECRL system are presented in Section IV and Section V, respectively.

II. TRADITIONAL APPROACH

An example of a traditional DC/DC converter used for thermal harvesting applications is depicted in Figure 2(a), reported, for example, in [4]. With respect to Figure 2(a), the major parts of a DC/DC converter for thermal harvesting applications are:

1) **Oscillator** transforms the low DC voltage coming from the TEG to a sinewave with a larger amplitude.
2) **Charge Pumps** increase the AC voltage to a higher magnitude.
3) **AC/DC** converts the AC signal generated by the previous stages to a continuous voltage appropriate for the CMOS logic that is employed in the system.

Each of the blocks contributes in power dissipation and area usage. The charge pump section of the system is particularly critical, since a high number of stages is required in order to boost the voltage, but in turn decreases the efficiency of the chain [11]. Such a system exhibits a very low power efficiency profile, in the order of 20 % [4], but has the advantage of being fully integrated. A promising solution for power efficiency was proposed in [5], where a high power efficiency of 73 % is reported. The high power efficiency in [5] is achieved by using a third dedicated DC/DC converter, where two additional DC/DC converters are used only to start-up the system. While this solution is promising for power efficiency, the area of the circuit is quite large at $1\,\mathrm{mm}^2$.

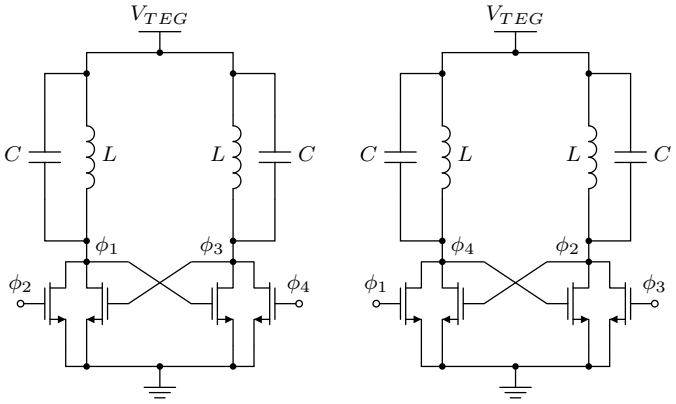


Fig. 3. The quadrature oscillator used to produce the four power-clocks.

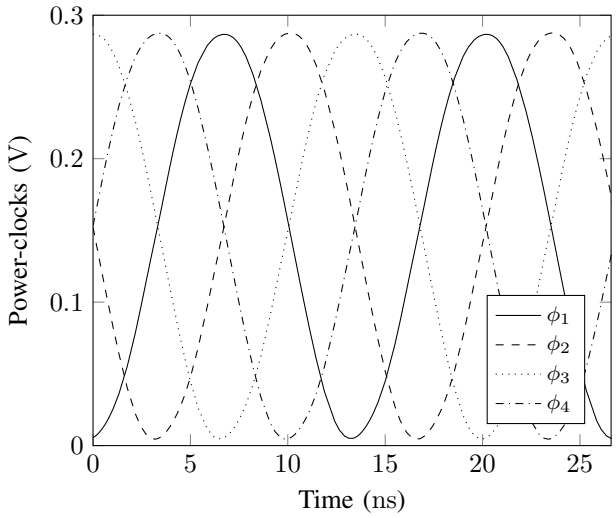


Fig. 4. The power-clocks generated by the quadrature oscillator of Figure 3, when $V_T = 150\,\mathrm{mV}$, $R_T = 10\,\Omega$, $C = 200\,\mathrm{fF}$, $L = 20\,\mu\mathrm{H}$. The measured oscillation frequency is $75.2\,\mathrm{MHz}$ and differs from the theoretical $1/\sqrt{LC} \approx 79.6\,\mathrm{MHz}$ because of the loading effect due to the ECRL logic.

III. PROPOSED SOLUTION

The proposed solution is represented in Figure 2(b), where an oscillator is directly attached to the charge recovery logic. Note how, with respect to Figure 2(a), the charge pumps and the AC/DC stages are eliminated. The job of the oscillator is to convert the DC voltage coming from the TEG to a sinewave; LC-tank oscillators naturally double the input voltage amplitude [12], making it possible to operate the CRL logic starting with a low voltage TEG. If a higher sinewave is needed, sophisticated versions of the LC-tank oscillator can be used, for instance using transformer feedback [4], [13].

IV. OSCILLATOR DESIGN PROCEDURE

If a two phase CRL family is used, it is possible to employ a simple LC-tank oscillator in order to generate the power-clock. In case of a CRL family that needs a four phase power-clock, the LC-tank oscillator is not sufficient. The quadrature oscillator [10], employs two LC-tank oscillators

coupled together as shown in Figure 3. Like any quadrature oscillator, the four outputs are sine-waves with 90° phase between each other, i.e. forming the four-phase power-clock for ECRL. The proposed design procedure, specific to charge recovery logic applications, is centered around the trade-off between frequency and minimum thermal voltage, described as follows.

As for any LC-tank oscillator, the natural frequency f_n is

$$f_n = \frac{1}{2\pi}\frac{1}{\sqrt{LC}}, \tag{1}$$

giving two degrees of freedom for the design, namely L and C. On the other hand, the startup condition for a LC-tank oscillator depends on these L and C values [5]:

$$V_{min} \propto \frac{R_S C}{k_n L} + V_{THN}. \tag{2}$$

Where V_{min} is the minimum voltage harvested from the TEG, V_{TEG}, at which the oscillator is functional, R_S is the inductor parasitic resistance, and k_n and V_{THN} are the transconductance and threshold voltage, respectively, of the NMOS transistors used in the oscillator.

Contrary to the design of an LC-tank oscillator for CMOS thermal harvesting [5], where the oscillation frequency is chosen for maximum efficiency and component availability, f_n of TP-ECRL is the operating frequency of the logic. Hence, f_n is a parameter to maximize in order to achieve the highest performance. At the same time, the minimum thermal voltage V_{min} for which oscillation occurs should be as low as possible. The design procedure to accomplish this is as follows:

1) Design specification: minimum harvested thermal voltage V_{min} and operating frequency f_n,
2) Verify that the CRL logic will work with a power clock at f_n and with magnitude $\approx 2V_{min}$,
3) Based on Equation (2) pick the smallest C,
4) Pick L based on Equation (1),
5) Size the NMOS in order to achieve oscillation.

This procedure ensures that a small capacitance and a large inductance are chosen, in order to be operational with a low V_{min}.

Another important performance parameter for a power-clock generator is the conversion efficiency [14], [15]

$$\eta = \frac{P_{CRL}}{P_{Total}} \tag{3}$$

where P_{CRL} is the power dissipated by the charge recovery logic and P_{Total} is the power consumed by the overall system (in this case the power of the TEG). Given an oscillator design, the maximum conversion efficiency is reached when the capacitor C of Figure 3 is the CRL load itself. Such systems are showed to reach efficiencies up to $77\,\%$ [15]. If an extra C is added to the CRL load, part of the current going through the transistors is not coming from the charge recovery logic but from the capacitor C, hence decreasing the conversion efficiency of the system. Although most of the power-clock generators use the CRL load as the capacitance

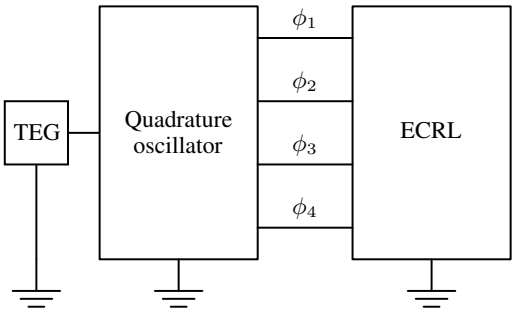


Fig. 5. An implementation of TP-ECRL.

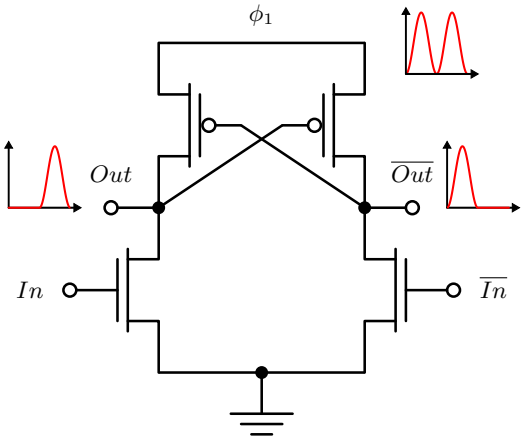


Fig. 6. The ECRL inverter/buffer used during the simulation

of the LC-tank [14], [16], the use of a lumped capacitor C simplifies the design, delivers better sine-shaped waveforms, and provides load variation immunity. The LC-tank oscillator in this work was designed with a capacitor C greater than the equivalent capacitance of the ECRL load, but still achieves efficiencies in excess of $50\,\%$.

V. Experimental Results

Figure 5 shows an ECRL based CRL circuit powered by a thermo-electrical generator, i.e. TP-ECRL. The system utilizes the quadrature oscillator of Figure 3 for the generation of the four power-clocks, ϕ_1, ϕ_2, ϕ_3, and ϕ_4. A target frequency of $80\,\mathrm{MHz}$ and a target V_{min} of $150\,\mathrm{mV}$, or a temperature gradient of $6\,\mathrm{K}$, are used. A 256-stage inverter chain is designed in ECRL [9] as a load for the oscillator. The single ECRL inverter/buffer gate is showed in Figure 6: 256 of these gates are connected in series to form a chain and offer a load to the power-clock. The system is implemented using the $45\,\mathrm{nm}$ FreePDK by NCSU, and simulated at the typical corner using Spectre.

The power consumption is obtained by integrating the current $I_T(t)$ coming from the TEG and multiplying the result by V_T. The proposed system is simulated against the CMOS system depicted in Figure 2(a). In this work, the power

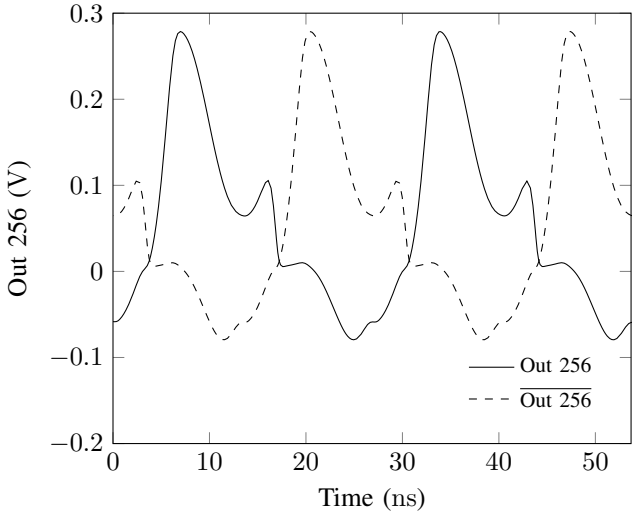


Fig. 7. The 256th output of the inverter chain of the system of Figure 5.

TABLE I
256 INVERTER CHAIN POWER CONSUMPTION, 80 MHz

	µW	Normalized to TP-ECRL
TP-ECRL	0.96	1×
CMOS	17.50	18.2×
NTV-CMOS	1.02	1.1×
WP-ECRL [7]	1.07	1.1×

consumption in the DC/DC stage is not reported quantitatively, as it is implementation specific, but the absence of the significant overhead of this converter from the presented comparisons should be noted. The CMOS system experiments are performed at two voltage levels, one at traditional operation with full V_{DD} and another at near-threshold voltage operation, indicated as NTV-CMOS. In particular, the near-threshold voltage used, namely $250\,\mathrm{mV}$, is a competitive circuit implementation for these voltage levels.

The power consumption of the simulated circuits, at a frequency of $80\,\mathrm{MHz}$, is presented in Table I. It is demonstrated that the TP-ECRL consumes $1/18$ the power of the CMOS and roughly the same as NTV-CMOS. As explained earlier, the reported numbers do not account for the DC/DC boost stage that would necessarily be present in CMOS implementations. Also, TP-ECRL is competitive with WP-ECRL [7], presenting an alternative in energy harvesting where wireless links are not feasible. Figure 7 shows the outputs of the 256th stage of the inverter chain. When the output is peaking, the distance between Out 256 and $\overline{\text{Out 256}}$ is roughly $300\,\mathrm{mV}$, hence guaranteeing good noise margins.

VI. CONCLUSIONS

In this work, charge recovery logic is proposed as an alternative to CMOS for thermal harvesting systems. In particular, ECRL is shown as a viable alternative, and the approach is named TP-ECRL.

TABLE II
THERMAL HARVESTING COMPARISON

	This work	[4]	[5]
Efficiency	57%	36%	73%
Area overhead	Small	Medium	Large

TP-ECRL consumes $1/18$ of the power of CMOS and saves area compared to NVT-CMOS, thanks to the removal of charge pumps and AC/DC converter. TP-ECRL also presents advantages in terms of area and power efficiency compared to simple thermal harvesting solutions such as [4], and efficiencies that are competitive with fully optimized systems such as [5], as shown in Table II. Further investigations entail temperature range analysis for a practical cyber-physical implementation of this promising technology.

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