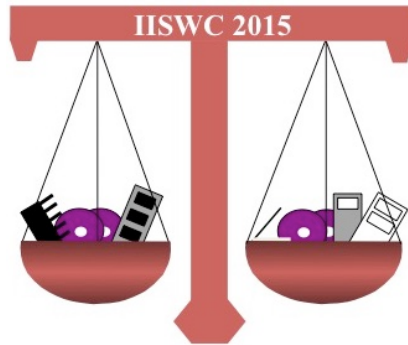


# Tutorial on Communication-Aware Workload Profiling and Memory-NoC Simulation SIGIL and SYNCHROTRACE

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**Key Topics:**  
workload profiling  
accelerator design  
design space exploration  
trace-driven simulation

## 2015 IEEE International Symposium on Workload Characterization

Understanding how CMPs, GPUs, and ASIC IPs communicate and interact to extract the most performance and efficiency out of future architectures.

### SIGIL [1]

a workload profiling toolset that enables architects to explore and investigate sources of performance bottlenecks in current and future systems.

1. Platform-independent workload behavior
2. Classification and capture of architecture agnostic metrics:
  - communication edges
  - computation operations
  - synchronization primitives
3. Accelerator selection HW/SW partitioning examples
  - How do we select the best balance of resources for future energy-constrained, bursty systems?

### SYNCHROTRACE [2]

trace-driven simulation framework for fast design space exploration; dependency- and synchronization- aware, utilizing trace generation from SIGIL.

1. Fast and accurate simulation of multi-threaded communication bound architectures
2. Addresses the emerging need and challenges of software synchronization-aware simulation
3. Synchronization-aware simulation over large design space
  - Motivates impact of capturing non-determinism of a workload
4. Network-on-Chip and memory model design exploration tutorials
  - How do we map threads to cores for the best performance?

[1] Siddharth Nilakantan and Mark Hempstead, **Platform-independent Analysis of Function-level Communication in Workloads**, IEEE International Symposium on Workload Characterization (IISWC), Portland, OR Sep 2013.

[2] Siddharth Nilakantan, Karthik Sangaiah, Ankit More, Giordano Salvador, Baris Taskin, Mark Hempstead, **SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multicore Simulation**. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), March, 2015.

<http://vlsi.ece.drexel.edu>

<http://dpac.ece.drexel.edu>

<http://github.com/dpac-vlsi>

*Drexel University VLSI & Architecture Lab*

*Drexel University Power Aware Computing Lab*

*Free and Open Source Software tools*

