3141 Chestnut St
Drexel University – ECE Dept
Philadelphia, PA 19104
☎ +1 267 439 5485
✉ lf458@gmail.com
vlsi.ece.drexel.edu

Leo Filippini

Summary I am a PhD candidate focusing on charge recovery logic and low-power VLSI systems, with a strong background in analog IC design and layout in deep-submicron CMOS. I have cleanroom and tapeout experience and a sound understanding of transistor level design and device physics.

Education

Present **PhD candidate**, *Drexel University*, Philadelphia (PA).
Electronics Engineering

2013 **Master Degree**, *University of Brescia*, Brescia (Italy), *summa cum laude*.
Electronics Engineering

2010 **Bachelor Degree**, *University of Brescia*, Brescia (Italy).
Information Engineering

Experience

Present **Research Assistant**, *Drexel University*, Philadelphia, PA (USA).
My research is focused on low-power methodologies for VLSI circuits. I am currently investigating novel implementations of charge-recovery logic, power-clock generation, and modeling of such systems.

Present **Instructor**, *Drexel University*, Philadelphia, PA (USA).
I am the co-instructor for Advanced Electronics I, a class focusing on analog design for integrated circuits.

Present **Teaching Assistant**, *Drexel University*, Philadelphia, PA (USA).
I have been the lab instructor for several undergraduate classes: Digital Electronics, Advanced Electronics I, Analog Electronics, and Electronic Devices. I conduct laboratory sessions, grade homeworks and lab reports, and I help students with the classes' final project.

Present **Senior Design Project Advising**, *Drexel University*, Philadelphia, PA (USA).
I am, along with two faculty members, advising one of the senior design teams of academic year 16/17. During our weekly meetings, we discuss research ideas and their feasibility.

2016 **Undergraduate Mentoring**, *Drexel University*, Philadelphia, PA (USA).
Drexel University STAR initiative allows undergraduate students to spend their freshman summer doing research. I was part of the team that mentored several students, one of which closely worked with me and helped me in my research.

2013 **Intern**, *Imec Belgium*, Heverlee (Belgium).
During this internship, which is also my Master's thesis, I designed an integrated transimpedance amplifier for capacitive ultrasonic transducers (CMUT).
Detailed achievements:
- Implementation of the transducer model in Cadence
- Theoretical comparison between different amplifier topologies
- Noise analysis
- Design of a topology new to the application
- Layouting and verification of a prototype IC in CMOS 180nm
- Tape-out

2010 **Intern**, *University of Brescia – Physics Department*, Brescia (Italy).
For four months I worked on my Bachelor's thesis: *Synthesis and integration of quantum dot semiconductors in third generation excitonic solar cells.* Along with my supervisors, we chemically synthesized different types of quantum-dots and realized many cells. I, in particular, took care of the substrate deposition and characterization, of the construction of the cells, and of their optical and electrical characterization. To do so, I used the following instruments: electronic load with 4-point probe, solar simulator, monochromator, lock-in amplifier (in order to measure cells' IPCE).

Languages

Italian Native

English Proficient — TOEFL iBT: 107/120

Honors & Awards

2016 Joseph and Shirley Carleone Endowed Fellowship

2011 Winner of European *Lifelong Learning Program* scholarship

Publications

[1] L. Filippini, D. Lim, L. Khuon, and B. Taskin, "Wireless Charge Recovery System for Implanted Electroencephalography Applications in Mice," in *(to appear) IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2017.

[2] L. Filippini and B. Taskin, "Charge Recovery Logic for Thermal Harvesting Applications," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 542–545.

[3] L. Filippini, E. Salman, and B. Taskin, "A Wirelessly Powered System with Charge Recovery Logic," in *IEEE International Conference on Computer Design (ICCD)*, October 2015, pp. 505–510.

[4] C. Sitik, E. Salman, L. Filippini, S. J. Yoon, and B. Taskin, "FinFET-Based Low-Swing Clocking," *ACM Journal of Emerging Technologies in Computing Systems (JETC)*, vol. 12, no. 2, September 2015.

[5] C. Sitik, L. Filippini, E. Salman, and B. Taskin, "High Performance Low Swing Clock Tree Synthesis with Custom D Flip-Flop Design," in *IEEE Computer Society Annual Symposium on VLSI*, July 2014, pp. 498–503.