# Information Package for Tenure and Promotion Review

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# Contents

# 1 Highlights

### Research achievements:

- The NSF Faculty Early Career Development (CAREER) Award, 2009.
- The "A. Richard Newton Graduate Scholarship Award", from the ACM Special Interest Group on Design Automation (SIGDA) at IEEE/ACM Design Automation Conference (DAC), 2007.
  - "*...granted to faculty investigators at universities trying to establish new programs in electronic design automation or circuit design...*", granted to one or two investigators per year.
- Co-author (with I. S. Kourtev and E. G. Friedman) of the book titled "*Timing Optimization Through Clock Skew Scheduling*" from Springer, 2009, ISBN-13: 978-0387710556.
- Author of forty-five (45) total publications in book chapters, refereed journals and conferences:
  - One (1) book chapter,
  - Eight (8) journal papers, with six (6) other manuscripts under review,
  - Thirty-six (36) conference papers (17 in 2009–2010 AY).
  - Best student paper award nominee (with S. Kurtas) at the IEEE International Midwest Symposium on Circuits and Systems, 2007.

### Teaching achievements:

- Advisor to four (4) Ph.D. students.
  - Vinayak Honkote, Ph.D., graduated in Summer 2010.
- Developer of six (6) *new* courses in the ECE curriculum:
  - 3 senior-level undergraduate Computer Engineering courses with laboratories:
    - Undergraduate (+graduate) enrollment in Fall 2007/08/09/10: 11/15/16(+5)/30.
  - 3 graduate level Computer Engineering courses.
- Advisor to one (1) B.S./Ph.D. student, six (6) M.S. students (2 graduated).
- Mentor to seven (7) undergraduate senior design teams.
  - Two (2) senior design teams are recipient of department awards.
- Average instructor rating of 4.4/5.0 for courses taught at Drexel University and Burlington County College (BCC).

### Proposal/Grant activity:

- Received a total of $984,000 in funds:

| Count and type | Agency/Organization | Req. Amount |
|---|---|---|
| 1R, 1E | National Science Foundation (NSF) | $760,000 |
| 1R | ACM SIGDA | $24,000 |
| 1R | MOSIS | $200,000 |
| 3R(esearch), 1E(ducation) | TOTAL | $984,000 |

- PI or Co-PI on forty-one (41) total proposals [Thirty-three (33) research and eight (8) educational].
- PI on two (2) NSF grants continuing through 2013 and 2014.

## Professional service:

- Member of the steering committee of IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2007–current.
- Member of the technical program committee for multiple conferences including:
  - IEEE International Conference on Computer Design (ICCD), 2010
  - IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), 2009, 2010
  - ACM Great Lakes Symposium on Very Large Scale Integrated Circuits (GLSVLSI) 2008, 2009, 2010.
- Panel discussant on the "New Performance Prediction Techniques for Interconnects" session at the $14^{th}$ International Workshop on System Level Interconnect Prediction (SLIP) 2010.
- Co-coordinator of the Association for Computing Machinery (ACM) Special Interest Group on Design Automation (SIGDA) University Booth program at the IEEE/ACM Design Automation Conference (DAC), 2008–current.

## University service:

- Advisor to the Applied Creativity Graduate Student Association (ACGSA), 2007–2009.
- Member of the ECE Faculty Recruitment Committee, 2007–current.
- Member of the campus review committee for Barry M. Goldwater scholarships, 2008.
- Member of the campus review committee for Fullbright scholarships, 2010.

## 2 Research Statement

My doctoral research at the University of Pittsburgh addressed the automation of clock skew scheduling application and the design of latch-based, non-zero clock skew integrated circuits (ICs). My current research interests still include clock skew scheduling and integrated circuit design but have expanded to address the technology challenges in implementing low-power, high-frequency IC clocking systems (e.g. clock generation, networks and interconnects). This line of research is essential for contemporary micro-electronic design, particularly during the ongoing paradigm shifts in computer architecture, design and electronic design automation methods in evolving to facilitate energy-efficient, multi-core operation. My research focus on IC clocking is a part of this trend toward energy-efficient, high-performance, many-core systems-on-chip because the clock generation and distribution (e.g. clock networks and interconnects) dictate the operating speed and are responsible for up to 50% of the overall power dissipation of the system. The first research project listed below is **High-Performance Clocking for Integrated Circuits through Resonance**. The described research project is significantly different than my doctoral research project in addressing deep-sub micron system design, implementation and simulation challenges as opposed to the design automation and optimization contributions earlier in my career. My interest in the *resonant clocking* research stems from the bigger goal in "revolutionizing the clock network design step of integrated circuit (IC) design flow": Resonant *rotary* clocking technology provides the infrastructure to achieve low-power, multi-core, multi-GHz operation while non-zero clock skew scheduling permits the implementation of this technology without timing violations. These two areas of expertise perfectly complement each other in establishing the set of knowledge necessary to accomplish the research goals.

The second research project listed below, **Low Power Clock Network Design and Timing**, is the product of my continued interest in "timing" of synchronous digital VLSI circuits. Timing analysis is the verification stage of the VLSI circuit design flow in terms of satisfying requirements based on the frequency of operation. My focus on this area spans traditional topics in VLSI timing in order to verify the operation of complex clocking techniques as well as branching out to the design of more complex, contemporary clock networks, particularly geared towards low power and variation-tolerant operation.

The third research project listed below, **Quantum-dot Cellular Automata (QCA)-based Nanocomputing**, encapsulates my efforts in the emerging area of nanoarchitectures. QCA is one of the emerging technologies proposed to replace the conventional CMOS technology for faster computation with less power dissipation and area overhead. I work on developing novel architectures and system-level design principles for QCA implementation. The broader impacts of this work are on improving the existing computing paradigm and educating the next-generation engineering workforce on nanocomputing. When QCA manufacturing becomes reliable in high volumes, QCA-based nanoarchitectures and systems will solve otherwise formidable problems with relative ease (similar to those of quantum computing regimes). This line of research in nanoarchitectures is important in providing a computer engineering perspective to the interdisciplinary nanotechnology and nanoscience research areas in emerging computing models and technologies.

The fourth project listed below, **Wireless IC interconnects**, is a recent project, partially performed in collaboration with three ECE faculty members. Wireless interconnects are composed of multiple antennas placed on the same die, operating in the RF or sub-THz range to provide a communication channel. Proposed as an alternative to global wire-based interconnects in semiconductor technologies, wireless interconnects can provide a low-cost solution to the magnified communication problems in emerging multi-core systems and 3D IC implementations. This line of research is important in proposing a novel alternative to the global communication problem on ICs with an interdisciplinary approach from the disciplines of wireless communications, antennas & propagation and electromagnetics.

These four research projects are briefly summarized below, including selected publications, graduate students under my supervision and funding activity for these projects.

## 2.1 Project 1: High-Performance Clocking for Integrated Circuits through Resonance

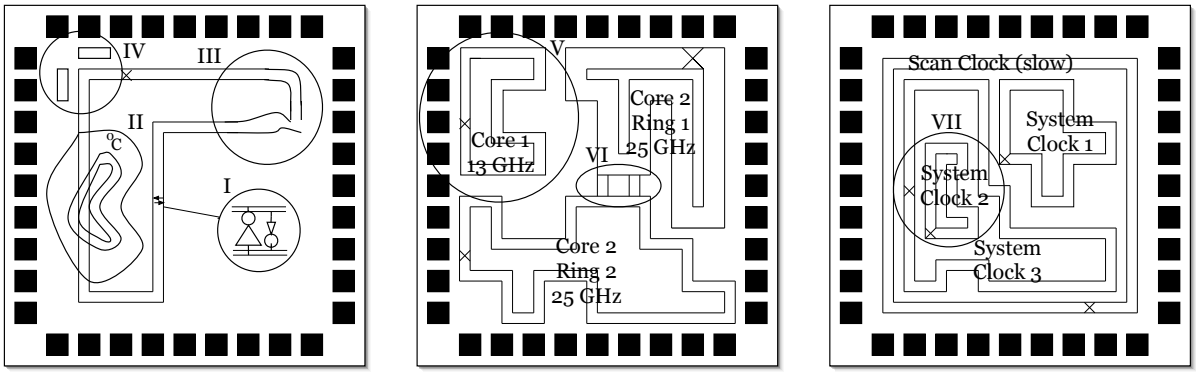
Achieving a controllable-skew, low-jitter synchronization with low power dissipation is a major objective for synchronous VLSI circuits operating at higher frequency regimes. In order to meet this objective, next-generation alternatives to conventional clocking, such as radio frequency, optical or (targeted) transmission line-based resonant clocking technologies, have been emerging. In this research project, my group is working on the design, design automation, optimization and verification challenges in order to enable the use of resonant *rotary* clocking technology to provide up to 40% reduced power dissipation (80% in the clock network) and 10X speed improvement in all integrated circuits (ICs).

Resonant clocking technologies present an alternative to complicated on-chip PLL components by generating a high frequency resonance through parasitics on chip. Based on the energy recovering *adiabatic* switching principles, resonant clocking technologies permit significant power savings. Resonant *rotary* clocking technology also permits non-zero clock skew operation, which can be used to further improve circuit performance such as providing improved *tolerance of timing to on-chip variations*.

In particular, this project entails the investigation of the design and analysis requirements of resonant rotary clocking technology for adaptability to

- manufacturing and environmental variations in nanoscale ICs,
- implementation of heterogeneous, multi-core computing systems,
- design automation through CAD implementation,
- sustainability for conventional and resonant clock network design.

The majority of the tasks are demonstrated in Figure 1. The expected outcome of this project is a novel clock network design step in IC design flow enabling low-power, multi-GHz operation with proven sustainability over nanotechnology integration. The proposed change will enable manufacturing of devices that are increasingly portable and significantly faster than current state-of-the-art, impacting all new and existing electronic products.



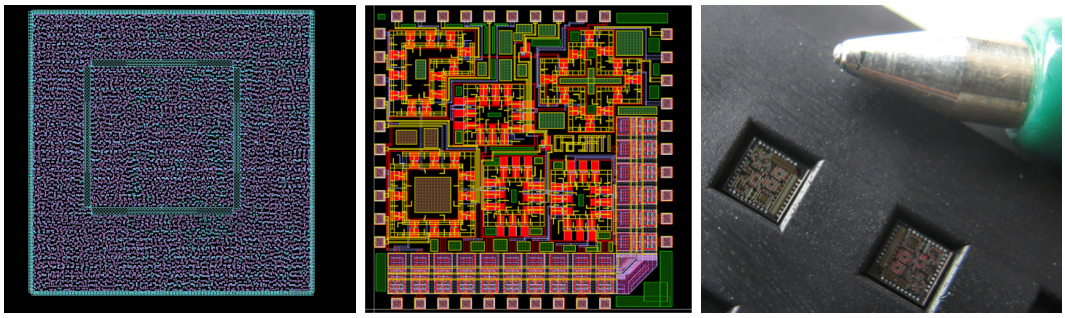

(a) I) Statistical, II) thermal, III) lithography and IV) RDR.

(b) V) Interconnect geometry, VI) interconnect synchronization.

(c) VII) Concentric rings for multiple domain and testability.

Figure 1: Nanoscale, custom multi-core and multi-domain rotary clock operation.

Demonstrated results have proved the motivation in pursuing the bigger goal that non-zero clock skewed circuits can be synchronized with ultra-low power and high frequency by resonant rotary clocking technology [JCSC09]. Two physical design flows are developed: the early one establishing a proof-of-concept [MWSCAS06b] and the recent one laying out a blueprint for an industrial scale implementation.



(a) Placement results for `s38584`. (b) 0.5$\mu$m implementation. (c) $1.5 \times 1.5$ $mm^2$ die lot.

Figure 2: Preliminary industrial CAD tool integration results and prototype silicon chip.

The proposed flow entails:

- A topology generation process for the distribution of rings for the rotary clocks [`TODAES09`],
- A custom topology clock router in order to route the rings closer to synchronous components [`MWSCAS08,ICCD08,TVLSI10`],
- Parasitic extraction [`ISLPED10`] and within 2% accurate SPICE model with transmission line models [`VLSID10,TVLSI10`],
- Capacitive balancing strategies to improve the frequency mismatch between rotary rings below 3% (from 10%) of the clock period [`MWSCAS09c,VLSID10`],
- A register synchronization through routing methodology that limits global skew to 2% of the clock period while saving 35% clock wirelength over a naive synchronization approach [`ISOCC09a,ISQED10`].

This developed physical design flow is novel in enabling the implementation of the resonant clocking technology and is elegant in permitting seamless integration into the mainstream IC design flow. These research items include the pragmatic modeling in an industrial tool flow. For these preliminary results, resonant rotary clock operation is modeled in `Synopsys`$^{TM}$environment [Figure 2(a)]. Peculiarities of rotary clocking interconnects are captured into models during simulation, design, synthesis, placement and optimization phases. Proposed project targets a *fully-integrated* placement and clock design process beyond pragmatic tool integration, which is a complicated problem due to the number of design variables. In Figures 2(b) and 2(c), my group's first silicon implementation of the CROA methodology-designed rotary clock is shown. This chip is currently under test, which will be used to demonstrate the efficacy of the proposed automation methodologies, despite at a lower frequency due to wirebonding (manufactured in a 0.5$\mu$m semiconductor process and operates at 4GHz).

Pre-silicon simulations at the 90nm node is depicted in Figure 3, demonstrating an expected frequency of 40GHz. Through device sizing, wire geometry and topology planning, higher frequencies are possible. The simultaneous challenge is to design *circuits* to operate at these higher frequencies, which is also addressed through building a special cell library.

As a part of this project, I collaborate with the following institutions: MultiGiG Inc. (Scotts Valley, CA) and Waveworks (Tustin, CA) on resonant clocking technology and CLK Design Automation (Littleton, MA) on parallel clock skew scheduling implementation.

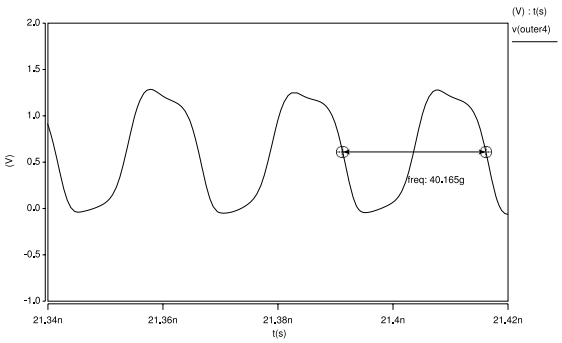
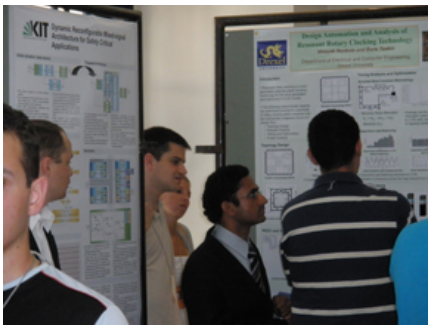



Figure 3: 40GHz rotary clock in 90nm.

(a) Accepting the A. Richard Newton Award at the IEEE/ACM Design Automation Conference in 2007.



(b) V. Honkote participating at the Ph.D. dissertation competition at the IEEE Computer Society Annual Symposium on VLSI Design in 2010.

**Selected Publications and Awards**

In recognition of these research activities and their broad impact, this work has resulted in the following awards:

- The A. Richard Newton Graduate Scholarship Award for project proposal "Routing for Resonant Clocking Technology in Multi-GHz Range" from ACM Special Interest Group on Design Automation (SIGDA) at the IEEE/ACM Design Automation Conference (DAC), 2007.
- The National Science Foundation (NSF) Faculty Early Career Development (CAREER) award, 2009.

Selected publications for the research activities of Project 1 are as follows:

- V. Honkote and B. Taskin, "CROA: Design and Analysis of Custom Rotary Oscillatory Array", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, (in pre-print).
- Y. Teng and B. Taskin, "Design Guidelines for Rotary Traveling Wave Oscillator Array Considering Skin Effects", *Journal of Low Power Electronics (JOLPE)*, (in review).
- V. Honkote and B. Taskin, "PEEC Based Parasitic Modeling for Power Analysis on Custom Rotary Rings", *IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, August 2010.
- V. Honkote and B. Taskin, "Analysis, Design and Simulation of Capacitive Load Balanced Rotary Oscillatory Array", *IEEE International Conference on VLSI Design (VLSID)*, January 2010, pp. 218–223.
- B. Taskin, J. Demaio, O. Farell, M. Hazeltine, R. Ketner, "Custom Topology Rotary Clock Router", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 14, No. 3, Article 44, May 2009.
- V. Honkote and B. Taskin, "Zero Clock Skew Synchronization with Rotary Clocking Technology", *IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2009, pp. 588–593.
- V. Honkote and B. Taskin, "Custom Rotary Clock Router", *IEEE International Conference on Computer Design (ICCD)*, October 2008, pp. 114–119.

**Supervised Graduate Students**

I supervise the following graduate students whose theses/dissertations focus on various aspects of the resonant rotary clocking technology research:

1. **Vinayak Honkote** received his Ph.D. degree in August 2010. Vinayak is the beneficiary of the "A. Richard Newton Graduate Scholarship" award and he worked on developing custom routing strategies and their automation tools for resonant rotary clock implementation. In the 2009-2010 academic year, Vinayak was one of the nine (9) Freshmen Engineering Design Fellows at the College of Engineering of Drexel University, preparing for an academic/research career. Vinayak was a finalist in the Ph.D. Dissertation Competition held at the IEEE Computer Society's Annual International Symposium on VLSI Design (ISVLSI) in July 2010.

2. **Ying Teng** is a first year Ph.D. student who expects to graduate in 2013. Ying is supported by the NSF CCF-0845270 funds at Drexel University. Her research entails the parasitic extraction of the rotary interconnects to develop accurate simulation models and application-specific integrated circuit (ASIC) design with rotary clocking.

3. **Abizer Nayeem** is a B.S./M.S. dual-degree candidate in who expects to graduate in 2010. Abizer is working on nanotube integration to the resonant clock distribution network design.

In addition to the graduate students, I supervised undergraduate research in the form of two senior design projects in 2006-2007 AY and 2009-2010 AY, and an REU student project in Summer 2010. The senior design project group in 2006-2007 completed a preliminary version of the custom clock router in Java programming language. Their work won the ECE Computer Engineering award, was presented at the University Booth at DAC 2007 and got published in TODAES in 2009. The senior design project group in 2009-2010 AY designed the first PCB-level implementation of the rotary ring to demonstrate technology scaling. Their work won the ECE Computer Engineering award.

**Funding Activity**

The project was funded in part by faculty start-up funds at Drexel University and in part by the A. Richard Newton Graduate Scholarship Award. Since September 2009, the following NSF CAREER award provides the primary source of funding:

- IEEE/ACM Design Automation Conference, "A. Richard Newton Graduate Scholarship", *Routing for Resonant Clocking Technology in Multi-GHz Range*, PI: B. Taskin, $24,000, 2007–2008.

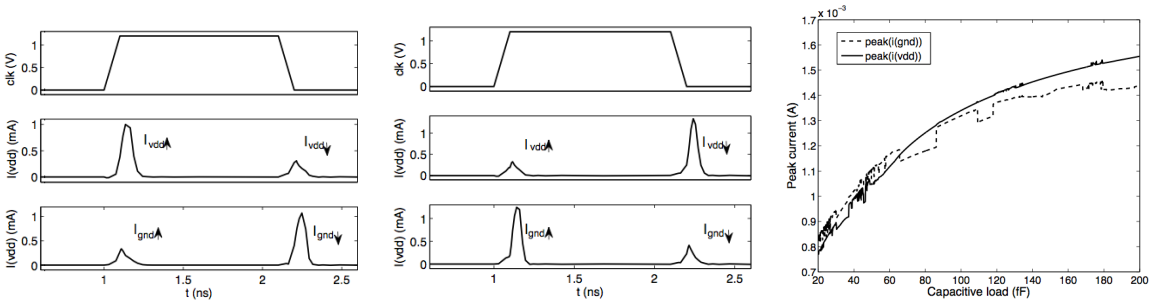
- National Science Foundation (NSF), *CAREER: Rotary Clock Technology Integration*, PI: B. Taskin, $400,000, 2009–2014.

I have developed the following pending proposals (September 2010) requesting support for extensions and equipment for this project:

- National Science Foundation (NSF), *II-New: Testbed for High Performance Interconnects*, PI:Taskin, $823,812, 2011–2014 (also impacts Project 4).

## 2.2 Project 2: Low Power Clock Distribution Network (CDN) Design and Timing

High frequency requirements and low power budgets of deep sub micron circuits make the task of clock distribution network (CDN) design quite challenging. In high performance microprocessors, up to 50% of the total power dissipation is attributed to the clock distribution network.

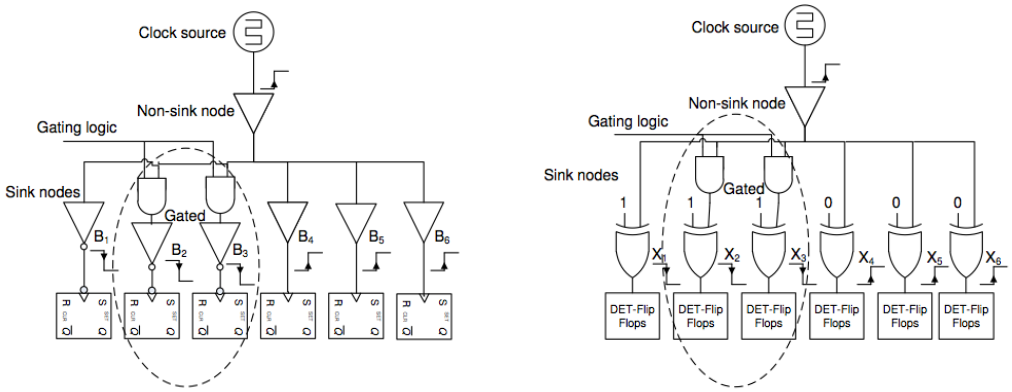



(c) Positive polarity buffer. (d) Negative polarity buffer. (e) Dependency on capacitive load.

Figure 4: Transient peak current simulations of clock buffers for peak current optimization.

Most items of research in this project extend to the *clock distribution network design* with tree and mesh-grid topologies. These aspects perfectly complement our existing work on the "verification" of complex clock distribution networks and schemes by investigating the design and improvement of the clock distribution networks themselves. My group has performed the following studies:

- **A weighted clock buffer polarity assignment method**: The simultaneous switching of the capacitance on a clock tree system draws significant amount of current from the power supplies. This current causes a fluctuation in the value of the power supply, directly proportional to the peak value of the current. "Clock polarity" assignment suggests the distribution of the switching capacitance on the clock network to two clock edges by using positive and negative polarity clock buffers as shown in Figures 4(c) and 4(d) in order to reduce the peak current. Some previous studies exist in clock polarity assignment. My group proposed a method to reduce the power/ground noise while preserving an existing clock tree topology. Our first contribution is to observe the dependence of the current drawn from the power supplies to the capacitive load of the switching elements, depicted in Figure 4(e). A method is devised where the switching elements are assigned weights based on there capacitive load, that is based on their relative strength in drawn the power supply current. Experimental results demonstrate that the peak current on the power/ground rails can be reduced by 5% to 21% more than the previous work, totaling up to 42% peak current reduction over a traditional clock tree. The average clock skew degradation is shown to be a very low 0.24X compared to the skew of the original clock tree [`ISVLSI10,TODAES10`].
- **Reconfigurable clock buffer polarity assignment:** Clock gating is a popular technique to reduce the power consumption on the clock tree by turning off the delivery of the clock signal to some parts of the distribution network. For a clock gated circuit, there are multiple modes of operation in which one or more regions of the distribution network will be cut off at any point in time. For these modes, the optimal clock polarity assignment is different. Existing clock buffer polarity assignment techniques cannot be performed dynamically at runtime. My group proposed an innovative approach for tree network design that integrates an XOR gate at the sink levels of a clock tree as illustrated in Figure 5. One of the inputs of the XOR is modulated to change the polarity of switching capacitance, enabling reconfigurable polarity. The drawback of this approach is the necessity to use dual-edge triggered FFs, which have larger area than conventional flip-flips. Experimental results demonstrate that the worst case peak current on the clock tree can be reduced by 33.3% by inserting the XOR gates at the sink levels, with an additional 12.8% through reconfiguring at the run-time based clock gating profiles. The proposed flow increases the area by 7.1% but reduces the total power consumption by 23.8% and reduces the global skew degradation (due to polarity assignment) from 19.3ps to 8.8ps [`VLSID10 (in review)`].




(a) Polarity assigned clock tree with clock gating. (b) Reconfigurable tree for a clock gated circuit.

Figure 5: Reconfigurable clock polarity assignment for clock gated trees.

- **Low power clock mesh design:** In high performance microprocessor design, the CDN is often synthesized with redundancy in order to reduce the susceptibility to on-chip variations. Clock mesh, cross-links and spines are the clock structures with redundancy. The redundancy in the typical clock mesh network permits very low skew variation at the expense of power dissipation. My group worked on a novel approach for clock mesh network synthesis and optimization called Registers On MEsh (ROME). ROME combines the placement and clock network synthesis stages of the traditional IC physical design flow. Registers are incrementally moved towards the clock mesh such that the total stub wirelength is greatly reduced. Moreover, the clock mesh can be more sparse without skew degradation because the skew introduced by the stub wirelength is minimal. A sample application of ROME on an ISCAS'89 benchmark circuit is illustrated in Figure 6, where the registers are marked for observation. In this particular benchmark circuit, a power saving of 18.8% is obtained through clock mesh and stub wirelength reduction. Experimental results on a number of benchmark circuits show that the total wirelength on the clock mesh is reduced by 36.1% on average with ROME with no degradation on the clock skew. The total power consumption of the circuit is reduced by 9.8%, which is very significant [`ASPDAC10` (in review)].

(a) Before ROME. (b) After ROME.

Figure 6: ROME moving the registers of circuit s13207 towards a 5 × 5 clock mesh to save 18.8% power.

- **Post-clock-tree-synthesis (CTS) clock tree optimization**: My group devised a delay insertion process to perform a limited version of clock skew scheduling for a scalable, practical implementation. It is shown that by a very limited amount of delay insertion, clock skew scheduling can be applied with 43% effectiveness [MWSCAS08,MWSCAS09a,JVLSI09].
- **Incremental post-CTS register placement**: We iteratively place the registers closer to each other in order to reduce the overall length of the clock tree for reduced power dissipation. Experimental results demonstrate that through this "practical" method, 2.8% reduced power dissipation is achievable without any major modifications on the existing clock tree [ISOCC09b].

The performance enhancing effects of **clock skew scheduled timing** (e.g. non-zero clock skew circuits) have been known for almost 20 years. Typically, designers employ ad hoc tricks to delay clock signals on timing violated paths to satisfy design budgets. Statistical Static Timing Analysis (SSTA) methods, which model process variations statistically as probability distribution functions (PDFs) rather than deterministically, have emerged to more accurately portray integrated circuit performance. We have performed this analysis thoroughly on traditional zero clock skew circuits where the synchronizing clock signal is assumed to arrive in phase with respect to each register. Clock skew scheduling (CSS) imparts very different timing constraints that are based, in part, on the topology of the circuit. Consequently, SSTA is applied to nonzero clock skew circuits in order to determine the accuracy improvement relative to their zero skew counterparts, and also to assess how the results of skew scheduling might be impacted with more accurate statistical modeling.

This research has shown SSTA to be of particular importance in discovering the maximum performance gain possible with clock skew scheduling. Nonzero clock skew circuits suffer from the pessimism of traditional deterministic corner based static timing analysis in three separate timing limitations. This pessimism is compounded because the frequency limits of skew scheduled circuits depend not only on the slowest paths in the circuit, but also on the quickest paths and the relative speeds between paths. Nonzero clock skew circuits are known to be *on average* 30% faster than zero clock skew circuits. An average clock period improvement of 38.25% is seen by applying statistical timing alongside clock skew scheduling, assuming a target yield of 99.73% [MWSCAS08b]. Futhermore, it has been found that the frequency limiting local data path, cycle, or reconvergent register pair in such circuits may change with more accurate statistical modeling, which would impact optimization applications.

### Selected Publications and Awards

These listed research activities have lead to a number of publications in the area, including one nominated for a best student paper award at MWSCAS 2008 and a book. Encapsulating my early timing research as well as my continued efforts at Drexel University, the book entitled "Timing Optimization through Clock Skew Scheduling" was published by Springer in 2009, shown in Figure 7:

- I. S. Kourtev, B. Taskin and E. G. Friedman, *Timing Optimization through Clock Skew Scheduling*, Springer, 2009, ISBN-13: 978-0387710556.
- S. Kurtas and B. Taskin, "Statistical Timing Analysis of Nonzero Clock Skew Circuits", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2008, pp. 605–608 [**Best student paper award nominee**].

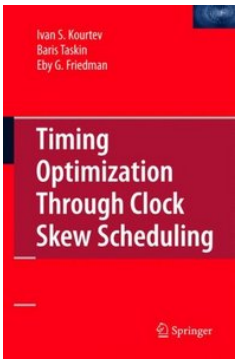



Figure 7: Timing book.

Other notable publications in this area include:

- J. Lu, Y. Teng and B. Taskin, "A Reconfigurable Clock Polarity Assigment Flow for Clock Gated Designs", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, (in review).
- J. Lu and B. Taskin, "Clock Buffer Polarity Assignment with Skew Tuning", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, (in review).
- J. Lu, Y. Aksehir and B. Taskin, "Registers On MEsh (ROME): A Novel Approach for Clock Mesh Network Synthesis and Optimization", *IEEE Asia-South Pacific Design Automation Conference (ASPDAC) 2010*, (in review).
- J. Lu and B. Taskin, "Reconfigurable Clock Polarity Assignment for Peak Current Reduction of Clock-gated Circuits", *IEEE International Conference on VLSI Design (VLSID) 2010*, (in review).
- J. Lu and B. Taskin, "Clock Tree Synthesis with XOR Gates for Polarity Assignment", *IEEE Computer Society's Annual International Symposium on VLSI (ISVLSI)*, July 2010.
- J. Lu and B. Taskin, "Clock Buffer Polarity Assignment Considering Capacitive Load", *IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2010, pp. 765–770.

**Supervised Graduate Students**

I supervise the following graduate student(s) on various aspects of this project area:

1. **Jianchao Lu** is a third year Ph.D. candidate. His research includes clocking and timing of low-power, high-performance circuits.
2. **John Vargas** is a part-time M.S. degree candidate. John is working on 3D IC package and interconnect modeling and automation.
3. **Xiaomi Mao** is a first year M.S. degree candidate who expects to continue for a Ph.D. program. Xiaomi is working on IC timing optimization through delay insertion.

In addition to the graduate students, I have advised undergraduate researchers:

- Yusuf Aksehir, a junior international summer research scholar, on low power clock mesh design.
- Dan Nguyen, as a prejunior and a junior, worked on improving clock tree topology implementation algorithms to incorporate unbalanced clock loads.
- Can Hankendi, a junior international summer research scholar, on graph algorithms for statistical timing.

**Funding Activity**

The majority of this work has been sponsored through Drexel University start-up funds.

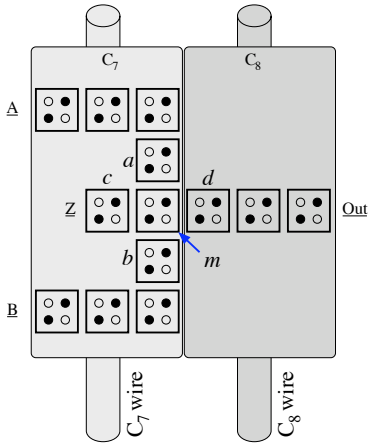
## 2.3 Project 3: Quantum-dot Cellular Automata (QCA)-based Nanocomputing

Quantum-dot cellular automata (QCA) technology is one of the emerging technologies proposed to replace conventional CMOS technology for faster computation with less power dissipation. Manufacturing of QCA devices is an open area for research, and device physicists have been working on the challenges of room-temperature operation, quantum-level modeling of QCA cells and fault-free synthesis for decades. One item that is missing in the current agenda of QCA research is a study on the layout optimization and system-level architecture design. After QCA manufacturing has matured and starts supporting massive

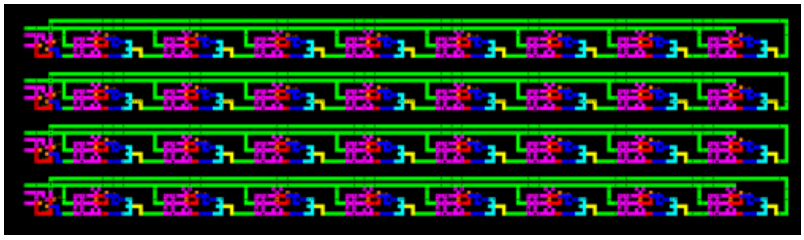
production, there will be a gap between existing QCA architecture knowledge and manufacturing potential. Also, the manufacturing of these nanoarchitectures are error-prone, thus, the study of fault-tolerant architecture and system design techniques are essential. The objective of this research is to investigate such fault-tolerant QCA architectures and advanced clocking schemes for practical implementation of QCA-based nanocomputers. Some early topics to be analyzed towards these grand goals include:

- Advanced clocking strategies to preserve the proper operation of QCA cells while permitting previously unachievable QCA device performance and fault tolerance,
- Self-sustaining, high-performance QCA memory cells,
- Comprehensive study of QCA logic and memory devices in order to realize optimal implementations for various objectives (such as area, power and speed) leading to a fault-tolerant cell library.

As a part of this research project, I have developed the fastest one-bit QCA memory cell [NANO06, TVLSI08]. Implemented with only two clock zones and two novel clocking phases, the dual-phase, line-based QCA memory cell presents improved read/write properties over conventional H-memory based QCA memory implementations. This memory cell is used as the building block for a shift-register based memory architecture, which was performed by undergraduate researchers as an extension to a senior design project in 2007 [NANOARCH07, JETC09]. The one-bit, dual-phase, line-based QCA memory cell and the shift-register-based memory are presented in Figure 8.




(a) Proposed dual-phase, line-based QCA memory where data is stored traveling along the line Z–Out. Clock wires illustrate how the clock zones are created.



(b) Shift-register-based $4 \times 8$ bit memory architecture.

Figure 8: Proposed QCA memory cell and architecture with dual-phase clocking.

The proposed outcomes of the project are on i) improving existing computing paradigm and ii) educating next-generation engineering workforce on nanocomputing. The recent results from QCA manufacturing have demonstrated the feasibility of implementation and are encouraging to system-realization in the future. Once QCA technology manufacturing has matured and starts supporting massive production, the fault-tolerant architectures and clocking schemes proposed in this project will have a major impact on the realization of QCA-based systems. Such low-cost, high-performance computing has the potential to revolutionize computing.

In the earlier stages of this project, I collaborated with Bo Hong (now at Georgia Tech).

**Selected Publications**

- B. Taskin, A. Chiu, J. Salkind, D. Venutolo, "A Shift-Register Based QCA Memory Architecture", *ACM Journal on Emerging Technologies and Computation (JETC)*, Vol. 5, No. 1, Article 4, January 2009.
- B. Taskin and B. Hong, "Improving Line-Based QCA Memory Cell Design Through Dual-Phase Clocking", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 16, No. 12, pp. 1648–1656, December 2008.

**Supervised Graduate Students**

I co-advised (with B. Hong) one graduate M.S. degree student, **Yaswanth Simhadri**, in the 2006-2007 academic year on QCA-implementation technology as a part of an independent research course. Yaswanth worked on the implementation (programming) of a QCA system simulator.

I also assign parts of the QCA project as undergraduate research and design project topics, the first two during the 2006-2007 academic year and the last one starting in Summer 2010:

- Vedant Vyas, a junior, has worked on improving the QCA memory read/write block design for two academic quarters.
- A senior design project group (2006-2007 AY) completed a memory architecture implementation using a one bit QCA memory cell. The senior design group's work was published in the ACM/IEEE NANOARCH 2007 and ACM Journal of Emerging Technologies (JETC) in 2009.
- Yi Li, a junior female student, started working on asynchronous QCA logic design.

**Funding Activity**

I have submitted to National Science Foundation (NSF) Emerging Models and Technologies (EMT) program twice but have not yet generated any funding.

## 2.4 Project 4: Wireless IC Interconnects

Increasing functionality and complexity in design of integrated circuits (ICs) require careful planning for on-chip resources such as area and power. Critical design decisions are often given based on the availability of these resources within increasingly stringent design budgets. Among these typical IC design budgets, *wire interconnects* are one of the most expensive items. Significantly impacting the timing, power and area resources, wire interconnects constitute the complex infrastructure to establish communication and synchronization within a conventional, state-of-the-art IC.

This research investigates a groundbreaking approach, where *wireless communication technology* replaces the resource-demanding, wire-based, global IC interconnects. By implementing transmitter and receiver antennas on the same chip, wireless communication will be used to communicate between distant components within a chip. Although the proposed on-chip wireless communication implementations will bear a constant overhead in area and power budgets (in order to implement the antennas and surrounding circuitry), this overhead will be much smaller than the quadratically increasing overhead of the conventional wire interconnects. As semiconductor technologies scale and die sizes increase, more space will be available on the chip for antennas, enabling better scalability of on-chip wireless communication. In the proposed research, we particularly target to replace the heavy-duty, global wires of the clock distribution network to demonstrate the on-chip wireless interconnect in addressing a major IC design challenge.

Previous research has proved the *feasibility* of implementing sub-THz IC antennas that have the capability to establish on-chip communication. There is also competing work on microstrip based and

THz range wireless interconnect designs in the literature (i.e. UCLA group). My group focuses on sub-THz, GHz range antennas for immediate integration with bulk-CMOS processes. Much work remains in performing a comprehensive analysis of either approach. My group has identified the following five challenges for GHz-range wireless interconnects:

1. Antenna characteristics under high levels of IC integration,
2. Antenna radiation effects on the metal interconnects in terms of signal integrity,
3. Antenna radiation effects on the circuit devices (e.g. transistors) in terms of leakage current,
4. Wireless system performance under switching noise from integrated digital circuitry,
5. Performance comparison of wireless interconnects with respect to wire-based global interconnects in terms of:
    - Footprint area,
    - Power consumption,
    - Delay,
    - Clock skew and jitter,
    - Bit error rate.

My group has addressed the first three challenges within the past year through 3D simulation based studies. We developed a feasibility study of our own of an intra-chip wireless interconnect system in typical operating environment. We studied the interaction of an intra-chip wireless interconnect system operating at 14 GHz with the circuit elements and local metal interconnects on the chip for 250 nm [ISQED10] and 90nm standard CMOS technologies [APS-URSI10], the former of which is shown in Figure 9. A FEM based 3-D full-wave solver, HFSS, is used to perform the electromagnetic field analysis. First, the implications of integration with standard CMOS circuits are examined, which include manufacturing process requirements such as Manhattan wiring, presence of an epitaxial layer and metal utilization bounds for lithography. These limitations of integration with standard CMOS are shown to be non-limiting to the performance of the antenna and accurate models are developed for frequency estimation [GLSVLSI10,APS-URSI10]. Next, it is shown that the transmission gain of the antennas is mostly unaffected by the presence of local metal interconnects. The transmission s-parameter between the radiating antenna and the metal interconnects is below 123.02 dB, which is very low for amplification [GLSVLSI10]. The leakage current in the sub-threshold region of the transistors, caused by the antenna radiation induced voltages, is shown to be below 2.1 fA and decreases with increasing distance from the radiating antenna [ISQED10].

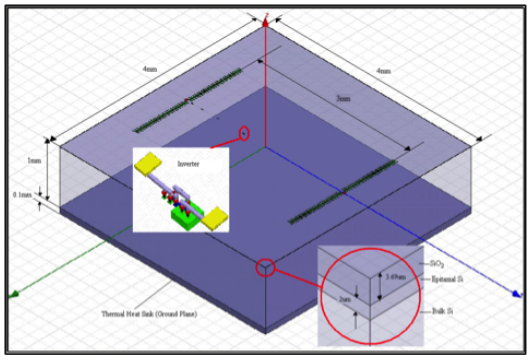
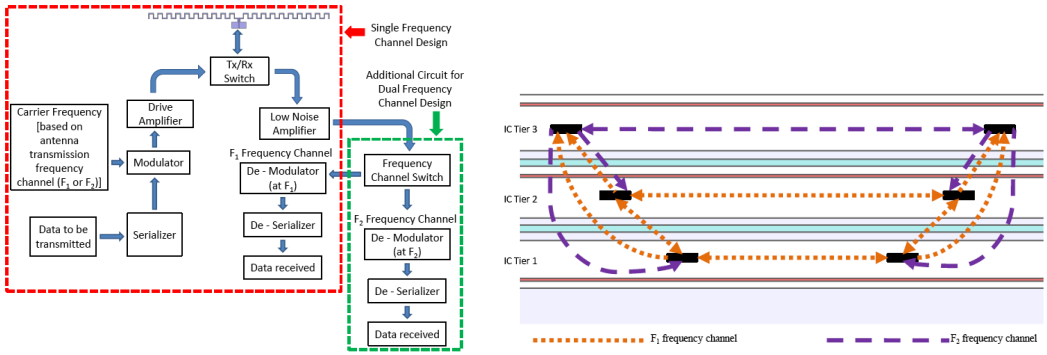


Figure 9: Simulated structure for a wireless interconnection system.

These results prove that the presence of local metal interconnects in the same metal layer as that of the antenna does not have any significant effect on the transmission gain between the antennas. Further, it is shown that the radiation from the on-chip antennas has very little effect on the circuit elements and local interconnects and therefore such a system is realizable without any detrimental effects on the existing system. We are currently working on measurements of prototype implementations that are in-house microfabricated and fabricated in a standard CMOS process in a share lot (e.g. MOSIS). These measurements will help confirm the simulation results addressing the first three challenges and provide directions to address the fourth and fifth challenges listed above.




(a) Transceiver block diagram. (b) Reconfigurability between 3 layers.

Figure 10: Wireless interconnects reconfigurable to two frequencies $F_1$ and $F_2$ in 3D ICs.

My group also recently started investigating the amenability of wireless IC interconnects for inter-tier communication on 3D ICs as demonstrated in Figure 10. IC geometry modification to 3D is one of the five options reported in 2005 ITRS roadmap (alongside signaling methods, innovative packaging, different physics and radical nano and bio technology based solutions) to improve interconnect performance. 3D ICs are formed by stacking multiple monolithic IC layers into a single package. 3D IC fabrication has not been perfected and thermal density is a grand challenge. The public information from 3D IC manufacturers is the use of 3D through-silicon-via (TSV) for communication between stacked 2D layers, however the challenge of making 3D devices with thousands of TSVs remains significant. We demonstrated in [`ISVLSI10,SOCC10`] that it is possible not only to have a strong communication channel but also to have communication in two frequency channels as shown in Figure 10. When implemented, the proposed reconfigurable hybrid 3D wireless network system with two frequency channels without the area and configuration overhead can reduce the latency and increase the network throughput.

We have also established an investigator group (with K. Dandekar and A. Petropulu) with complementary expertise to address interdisciplinary issues such as wireless communications principles in IC package media, existing antenna design knowledge and functional prototype design to monitor the contemporary issues in IC design in a cohesive manner. A. Daryoush has unoffically advised some of the research activities in electromagnetic analysis and antenna design. Manufacturing through microfabrication and measurement are performed in collaboration with a number of faculty members, including A. Daryoush, A. Fontecchio, P. Herczfeld and J. Spanier.

### Selected Publications

- A. More and B. Taskin, "Simulation Based Study of On-chip Antennas for a Reconfigurable Hybrid 3D Wireless NoC", *IEEE International SOC Conference (SOCC)*, September 2010.
- A. More and B. Taskin, "Electromagnetic Compatibility of CMOS On-chip Antennas", *IEEE AP-S International Symposium on Antennas and Propagation (APS-URSI)*, July 2010.
- A. More and B. Taskin, "Simulation Based Feasibility Study of Wireless RF Interconnects for 3D ICs", *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2010.
- A. More and B. Taskin, "Simulation Based Study of Wireless RF Interconnects for Practical CMOS Implementation", *IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2010.

- A. More and B. Taskin, "Electromagnetic Interaction of On-Chip Antennas and CMOS Metal Layers for Wireless IC Interconnects", *IEEE/ACM Great Lakes Symposium on VLSI Design (GLSVLSI)*, May 2010.
- A. More and B. Taskin, "Leakage Current Analysis for Intra-Chip Wireless Interconnects", *IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2010, pp. 49–53.

### Supervised Graduate Students

I supervise the following graduate student(s) in this research area:

1. **Ankit More** is a first year Ph.D. student. His research is on wireless interconnects for intra-chip communications. Ankit has graduated with top honors (highest GPA) in Electrical Engineering with a BS/MS degree from Drexel University.

### Funding Activity

This research area have been the theme for only a limited number of proposals so far, which were not successful. The following proposals are pending:

- National Science Foundation (NSF), *II-New: Testbed for High Performance Interconnects*, PI:Taskin, $823,812, 2011–2014 (also impacts Project 1).

# 3 Teaching Statement

From day one, my primary teaching goal at Drexel University has been to introduce VLSI Design courses at both the undergraduate and graduate level offerings of our program. Traditionally, it has been advertised that the ECE Department at Drexel University has nationally recognized research programs in several areas such as telecommunications, information networking, computer networks, imaging and signal processing, microwave and lightwave engineering, fiber optics and photonics, power systems engineering, ultrasonic and biomedical engineering. Given the size of the university and the electrical engineering department, the computer engineering program unarguably has room for significant improvement. Within the last few years, the department has been recruiting in this area in order to strengthen the computer engineering program. Being the sole faculty member with interests in VLSI design and electronic design automation (EDA), I took on the task of introducing VLSI courses into the graduate and undergraduate curricula. I have developed six (6) new courses *with laboratory components and accompanying manuals* providing students access to industry-standard design tools:

| **Course Title** | **Course Number** | **Level** | **Developed** |
|---|---|---|---|
| Custom VLSI Design | ECE-C471 | Senior/Graduate | F07-08 |
| ASIC Design I | ECE-C472 | Senior/Graduate | W07-08 |
| ASIC Design II | ECE-C473 | Senior/Graduate | Sp07-08 |
| EDA for VLSI IC Circuits | ECE-C671 | Graduate | F05-06 |
| EDA for VLSI IC Circuits II | ECE-C672 | Graduate | W05-06 |
| Deep Sub-Micron (DSM) IC Design | ECE-C673 | Graduate | Sp05-06 |

These courses complement the already existing Hardware Description Language (HDL) and FPGA design based courses in the computer engineering track and numerous microelectronics and semiconductor-level courses in the electrophysics track offered in our undergraduate and graduate curricula.

With three (3) newly developed, senior-level courses in VLSI Design, undergraduate students can now take VLSI as a *track* in their senior year. These courses are the first courses in the CE curriculum where the second course does not require the first course as a pre-requisite. The students can freely choose to take the first or the second courses, providing increased flexibility for creativity and intellectual interest in the senior year. These courses have been received very well by the undergraduate students as demonstrated in Figure 11. The enrollment for the Custom VLSI Design course, as offered in the fall quarter of each year since 2007, has increased steadily. In Fall 2010, the course is full at its classroom size limit of 30 students and graduate students are not permitted to sign up for this course.

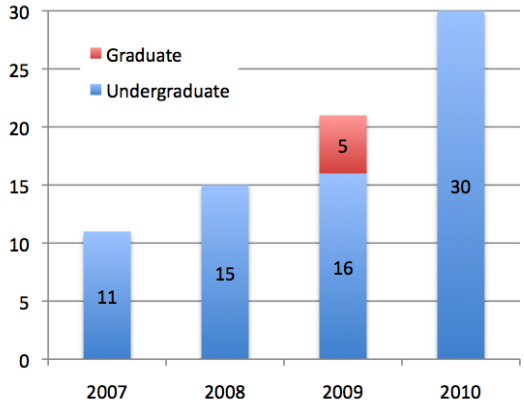



Figure 11: Enrollments for Custom VLSI Design.

In the long run, the success of the VLSI program at Drexel University will be beneficial in many respects, in providing the opportunity for:

- The students to explore (and eventually lead) VLSI research and the semiconductor industry,
- The ECE department to improve the VLSI design and nanocomputing offerings at the institution,
- The VLSI industry to recruit from the talented pool of Drexel University students,

- The semiconductor/VLSI community to receive increased participation from the individuals and resources from the traditional demographic and geographic resources of Drexel University.

### 3.1 Undergraduate Courses

I have taught seven (7) different undergraduate courses [five (5) in the ECE department and two (2) in the College of Engineering]. The courses are as follows:

| | |
|---|---|
| Recitation (2 sections) for Linear Engineering Systems (ENGR-231) | F08-09 |
| Recitation (2 sections) for Digital Logic Design (ECE-200) | Sp07-08 |
| Recitation (9 sections) for Dynamic Engineering Systems (ENGR-232) | W/S07-08, W08-09, S09-10 |
| Instructor for Custom VLSI Design (Intro. to VLSI Design) (ECE-C490) | F07-08, F08-09, F09-10 |
| Instructor for ASIC Design I (VLSI Design and Automation) (ECE-C490) | W07-08, W08-09, W09-10 |
| Instructor for ASIC Design II (Modern VLSI IC Design) (ECE-C490) | Sp07-08, Sp08-09, Sp09-10 |
| Instructor for Programming for Engineers (ECE-C203) | F07-08 |

My primary teaching goal at the undergraduate level is to ensure that all students have the understanding of the core concepts. Such understanding is crucial to provide a homogeneous learning environment and to provide a high level of quality in undergraduate education for all students. I monitor student progress daily with interactive teaching methods and weekly with laboratory assignments. In order to provide uninterrupted and complete coverage of lecture items in a 10-week span, I use electronic slides uploaded on WebCT. Students print their slides before the lectures and complete the "missing" parts in class providing interactive learning while sustaining the pace. Lecture notes also provide a medium to enable my secondary goal in teaching undergraduate classes: provide in-depth, "real-world" knowledge (as students often cite), particularly to support those students who show increased interest in the subject matter. In my VLSI classes, I often use tablet PC features to go over additional material to satisfy students' curiosities. In such a dynamic field such as microelectronics, slides (from publishers or otherwise) can quickly become outdated, thus, additional discussions are necessary to provide contemporary examples and challenges. In my programming classes, I often cite the common challenges faced by software programmers to provide the students with a deeper understanding of why the fundamentals of programming are a part of the engineering curriculum. For example, in the last week of classes for the ECE-C203 Programming for Engineers course in Fall 2007, I discussed the concepts learned throughout the quarter on a recent programming project I had completed, which generated significant amount of interest from the students.

### 3.2 Graduate Courses

I have taught six (6) graduate courses [Three (3) of them are cross-listed with undergraduate courses] in the ECE department. The courses are as follows:

| | |
|---|---|
| Instructor for Custom VLSI Design (ECE-C490) | F09-10 |
| Instructor for ASIC Design I (ECE-C490) | W09-10 |
| Instructor for ASIC Design II (ECE-C490) | Sp09-10 |
| Instructor for EDA for VLSI IC Circuits I (ECE-C690) | F05-06, F06-07, F09-10 |
| Instructor for EDA for VLSI IC Circuits II (ECE-C690) | W05-06, W06-07, W09-10 |
| Instructor for Deep Sub-Micron IC Design (ECE-C690) | Sp05-06, Sp06-07, W09-10 |

My primary teaching goal at the graduate level is to provide as much and as in-depth information as possible within a 10-week span. I differentiate graduate teaching from undergraduate teaching in *partially* letting the students determine how much "extra" information they choose to gather from the course. I

emphasize the core concepts by providing weekly homework assignments and with increased emphasis during my lecturing. My teaching plan follows that of an undergraduate class: Supported by pre-cooked slides with "missing" information (to be completed in class), regular homework assignments and design projects. These items establish the educational materials to provide the core information I expect students to get from the course. The *extra* information some students would like to get from the course, that is, the open-endedness, creativity and learning desires of students, are stimulated with design projects. I often use a grading system where learning the core material would suffice to obtain a full grade in student projects, however, bonus points are assigned for categories such as the "coolness" of the approach, significant literature research, improved testbeds etc. Also, despite the syllabus-oriented, lecture-format classes, my lecture slides often include state-of-the-art topics and open challenges to stimulate intellectual curiosity and class discussions. I find that such an approach is very effective in promoting the self-teaching habits students need to develop to stay on top of these dynamic fields upon graduation.

### 3.3 Independent Research Projects

I believe undergraduate and graduate student research education are integral parts of contemporary engineering education. I support and constantly seek students who are willing to participate in individual research projects to improve their learning experience at Drexel University. These studies take the following forms:

1. Independent research course studies,
2. Voluntary research studies,
3. Senior design projects,
4. Summer research experience (including visiting *international scholars*).

Since 2005, I have advised (or co-advised):

- four (4) undergraduate independent research courses: [Shannon Kurtas (W06-07), Daniel Levin (S06-07), Hahna Kane (F07-08), Michael Zhang (S09-10)],
- seven (7) undergraduate students voluntarily working on research: [Vedant Vyas (F06-07, W06-07), Austin Tran (W06-07,Sp 06-07), Danh Nguyen (Sp06-07–S07-08), James Kerak (Sp06-07-F06-07)], Hahne Kane (S07-08), Yi Li (S09-10),
- one (1) undergraduate student from a different university voluntarily working on research: [Bo Hyun Kim from Carnegie Mellon University (S09-10)].
- five (5) graduate independent research courses: [Yaswanth Simhadri (F06-07, W06-07, Sp06-07), Sharat C. Chandra (W09-10, Sp09-10)],
- four (4) senior design groups [out of seven (7) total] completing the research experience portion of their project [two in 06-07AY, one in 08-09AY],
- three (3) international scholars for summer research experience: [Can Hankendi (S06-07), S. Kutal Gokce (S06-07), Yusuf Aksehir (S09-10)].

I use these research project forms to educate and motivate students in becoming research scholars addressing pressing engineering needs in the cutting-edge of technology. Although each individual item in the above list demands a specific educational approach (e.g. the course credit requirements of Senior Design project must be clearly identified and established independent of the outcoming research project), the final product is often similar in improving the independence, scholarship, motivation and confidence in our students and future colleagues. I believe, students who have a positive research experience and have established a mentorship relationship with faculty will be more likely to pursue advanced degrees and become leaders in their field.

# 4 Service Statement

This section details my service activities to the research community, the ECE department and Drexel University, as well as to the public as a part of the outreach activities.

## 4.1 Service to the Research Community

The primary focus of my service related activities are service to the research community in the forms of committee memberships, coordinatorships and reviewership. I enjoy the supportive and encapsulating environment the research community provides and have benefited immensely both personally and professionally. I volunteer to provide my services to the community for the continuation of these activities where possible. Towards this end, I serve on the steering committee of one of the larger and older conferences on circuits and systems, IEEE International Midwest Symposium on Circuit and Systems (MWSCAS). I particularly enjoy the professional development component for new researchers (e.g. graduate students) within MWSCAS in providing the ideal forum to discuss early phase research. I also take responsibilities on the technical program committees of more selective conferences, such as IEEE Great Lakes Symposium on VLSI (GLSVLSI), IEEE International Conference on Computer Design (ICCD) and IEEE Symposium on Nanoscale Architectures (NANOARCH), in the VLSI and nanoarchitecture fields.

## 4.2 Service to the Department and University

My service to the department and university has been at levels appropriate to my academic standing. I am a member of the Computer Engineering (CE) Curriculum committee, which has experienced significant changes within the past five (5) years. As a group, we have implemented changes at the junior and senior levels of the undergraduate curriculum to eliminate the concept of senior sequences. This revamping and restructuring of the curriculum was motivated by a need to provide increased flexibility to students in choosing advanced technical courses. The changes compose of:

1. offering first courses in advanced topics during the junior year,
2. offering new, advanced courses at the senior level that are:
   (a) not sequences of three quarters,
   (b) building up on the technical expertise acquired at the newly offered junior-level courses.

I am the first (and to date the only) member of the CE group to develop courses at the senior level to enable the implementation of these changes. The three courses in the VLSI area that I developed have been offered since 2007, with increasing enrollment in each year. We have observed students enrolling in the Winter and Spring quarters only, which demonstrates the acceptance of the provided flexibility by our students. When courses of similar format increase in number, we will be able to have students create the program around their intellectual areas of interest.

In terms of service to the University, I served as a faculty advisor to the Applied Creativity Graduate Student Association (ACGSA) from 2007 to 2009 with Dr. Fredericka Reisman from the Goodwin College of Professional Studies. I helped supervise and organize the 2008 Fall seminar series with speakers outside Drexel University, featuring Dr. Keith Sawyer from Washington University in St. Louis.

In 2008 and 2010, I have served as a member of the campus review committees for the Barry M. Goldwater and Fullbright Scholarships, respectively. In these services, I provided feedback, critiqued and helped improve the student application and application essays for these prestigious scholarships. In the former, my expertise in the microelectronics engineering discipline was critical in organizing the application of one female undergraduate student. In the latter, my international expertise in the geographical

and educational details of the Turkey and Middle Eastern region was critical in developing fullbright scholarship applications to study in these regions.

### 4.3 Outreach Service

As a representative for the Computer Engineering group, I have participated regularly at college and departmental open houses as well as hosting individual visits for students and their parents. I participate in the Summer Engineering Experience at Drexel (SEED) events with Dr. Nagvajara in demonstrating systems design using the Roomba architectures to high-school students from the Philadelphia school districts. I also have hosted a summer high school student in Summer 2010 as a part of the Summer Mentorship Program of the College of Engineering.

My largest outreach activity takes the form of an NSF-funded REU Site. I am the PI and academic coordinator of an interdisciplinary REU Site on Computing for Power Energy (CPE). CPE is a Research Experience for Undergraduates (REU) program hosting 10 undergraduate students over 10-weeks. REU participants work on computing based research projects targeting power and energy challenges, including those in old technologies such as smart power grids, new technologies such as data centers and portable electronics and renewable technologies such as in nanosensors and energy conversion systems Starting Summer 2010 for the next three years, we bring in 10 qualified undergraduate students each year from around the nation to participate in these projects; promoting and recruiting for advanced degree programs in science, technology, engineering and mathematics (STEM) disciplines.


Figure 12: Dr. Taskin (on the left) with REU fellows of the NSF REU Site on Computing for Power and Energy in Summer 2010.

The summer 2010 cohort, pictured in Figure 12, includes students from Columbia University, RPI, UC Santa Cruz, Portland State University, UMBC, Cornell, North Carolina State University and Drexel University. This student cohort is very diverse, with three (3) African-American and two (2) Hispanic REU fellows, one (1) of whom is a female engineering student. I will look to extend and improve this trend, particularly targeting increased number of female students for the incoming cohorts.

# 5 Tabular Summary of Accomplishments and Contributions

In the following table, *Years 1 through 5* correspond to academic years 2005–2006 to 2009–2010, respectively.

| Category | Activity | Year 1 | Year 2 | Year 3 | Year 4 | Year 5 | Total |
|---|---|---|---|---|---|---|---|
| **Research** | Books and book chapters | 0 | 1 | 0 | 0 | 1 | 2 |
| | Journal papers (+ in review) | 1 | 0 | 0 | 4 | 2 (+6) | 7 (+6) |
| | Submitted journal papers | 0 | 2 | 3 | 2 | 6 | 14 |
| | Refereed conference papers | 3 | 1 | 4 | 5 | 17 | 30 |
| | Research proposals submitted | 5 | 9 | 8 | 4 | 9 | 35 |
| | Proposals funded | 0 | 0 | 1 | 0 | 2 | 3 |
| | Total external research funding | $0K$ | $0K$ | $24K$ | $0K$ | $600K$ | $624K$ |
| | Ph.D. students graduated | 0 | 0 | 0 | 0 | 1 | 1 |
| | M.S. students graduated | 0 | 0 | 2 | 0 | 2 | 4 |
| **Teaching** | Educational proposals submitted | 0 | 4 | 2 | 0 | 2 | 8 |
| | Educational proposals funded | 0 | 0 | 0 | 0 | 1 | 1 |
| | Total educational funding | $0K$ | $0K$ | $0K$ | $0K$ | $360K$ | $360K$ |
| | Senior design projects | 1 | 4 | 0 | 1 | 1 | 7 |
| | Freshman design projects | 1 | 0 | 0 | 0 | 0 | 1 |
| | Undergraduate courses taught | 0 | 0 | 10 | 7 | 5 | 22 |
| | Graduate courses taught | 3 | 3 | 0 | 0 | 6 | 15 |
| | Overall instructor rating (out of 5.0) | 4.4 | 5.0 | – | 4.0 | – | 4.4 |
| **Professional Service** | Conference technical/steering program committees | 2 | 1 | 5 | 5 | 8 | 21 |
| | Panel discussant | 0 | 0 | 0 | 0 | 1 | 1 |
| | Session chair/coordinator | 1 | 2 | 2 | 2 | 3 | 10 |
| **University Service** | Student association advising | 0 | 0 | 1 | 1 | 0 | 2 |
| | Department/college/university committees | 0 | 0 | 2 | 1 | 2 | 5 |
| | M.S. thesis committees | 2 | 1 | 2 | 0 | 0 | 5 |
| | Ph.D. candidacy/proposal committees | 1 | 1 | 0 | 2 | 3 | 7 |
| | Ph.D. defense committees | 0 | 0 | 0 | 1 | 1 | 2 |

# 6 Curriculum Vitae

## 6.1 Current position

| | |
|---|---|
| Rank: | Assistant Professor |
| Department: | Department of Electrical and Computer Engineering |

## 6.2 Contact Information


| | |
|---|---|
| Office Address: | Department of Electrical and Computer Engineering<br>Drexel University<br>3141 Chestnut Street<br>Philadelphia, PA 19104-2875<br>USA |
| Office Phone: | 1-215-895-5972 |
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| E-mail: | `taskin@ece.drexel.edu` |
| Personal URL: | `http://ece.drexel.edu/faculty/taskin/` |
| Laboratory URL: | `http://vlsi.ece.drexel.edu` |


## 6.3 Education

| | |
|---|---|
| 2005 | **Ph.D.** in Electrical Engineering<br>University of Pittsburgh, Pittsburgh, Pennsylvania<br>Advisor: Ivan S. Kourtev (now at `Google Inc.`) |
| 2003 | **M.S.** in Electrical Engineering<br>University of Pittsburgh, Pittsburgh, Pennsylvania |
| 2000 | **BS.** in Electrical and Electronics Engineering<br>Middle East Technical University (METU), Ankara, Turkey |

## 6.4 Employment

| | |
|---|---|
| 2005 – present: | **Assistant Professor**<br>Department of Electrical and Computer Engineering<br>Drexel University, Philadelphia, Pennsylvania |
| 2003 – 2004: | **Staff Engineer**<br>MultiGiG Inc.<br>Scotts Valley, California |
| 2000 – 2005: | **Teaching Assistant, Research Assistant, Teaching Fellow**<br>High Performance Integrated Circuits Laboratory<br>University of Pittsburgh, Pittsburgh, Pennsylvania |

## 6.5 Research Activities

This section details my research activities, including awards, publications, related funding activity and student advising.

### 6.5.1 Research Awards

**Total: 3**
**At Drexel: 3**
**Last 5 Years: 3**

1. 2009 Faculty Early Career Development (CAREER) Award, The National Science Foundation (NSF).

2. 2007 Best Student Paper Award Nomination, IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Knoxville, TN.

3. 2007 A. Richard Newton Graduate Scholarship Award, ACM SIGDA, IEEE/ACM Design Automation Conference (DAC).

### 6.5.2 Books and Book Chapters

**Total: 2**
**At Drexel: 2**
**Last 5 Years: 2**

1. 2009 I. S. Kourtev, B. Taskin and E. G. Friedman, *Timing Optimization through Clock Skew Scheduling*, Springer, 2009, ISBN-13: 978-0387710556.

2. 2006 B. Taskin, I. S. Kourtev and E. G. Friedman, "System Timing," *Handbook of VLSI*, $2^{nd}$ edition, W. K. Chen (Editor), CRC Press, Dec. 2006.

### 6.5.3 Refereed Journal Publications

**Total: 8**
**At Drexel: 6**
**Last 5 Years: 7**

1. 2010 V. Honkote and B. Taskin, "CROA: Design and Analysis of Custom Rotary Oscillatory Array", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems.*

2. 2010 J. Lu and B. Taskin, "Post-CTS Delay Insertion", *Journal of VLSI Design*, Article 451809, vol. 2010, February 2010.

3. 2009 B. Taskin and I. Kourtev, "Multi-Phase Synchronization of Non-Zero Clock Skew Level-Sensitive Circuit", *International Journal on Circuits, Systems and Computers (JCSC)*, Vol. 18, No. 5, pp. 899–908, July 2009.

4. 2009 B. Taskin, J. Demaio, O. Farell, M. Hazeltine, R. Ketner, "Custom Topology Rotary Clock Router", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 14, No. 3, Article 44, May 2009.

5. 2009 B. Taskin, A. Chiu, J. Salkind, D. Venutolo, "A Shift-Register Based QCA Memory Architecture", *ACM Journal on Emerging Technologies and Computation (JETC)*, Vol. 5, No. 1, Article 4, pp. 1–18, January 2009.

6. 2009 B. Taskin and B. Hong, "Improving Line-Based QCA Memory Cell Design Through Dual-Phase Clocking", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 16, No. 12, pp. 1648–1656, December 2008.

7. 2006 B. Taskin and I. S. Kourtev, "Delay Insertion Method in Clock Skew Scheduling," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems,* Vol. 25, No. 4, pp. 651–653, April 2006.

8. 2004 B. Taskin and I. S. Kourtev, "Linearization of the Timing Analysis and Optimization of Level-Sensitive Digital Synchronous Circuits", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 12, No. 1, pp. 12–27, January 2004.

### 6.5.4 Journal Publications under Review

| | |
|---|---|
| **Total:** | **6** |
| **At Drexel:** | **6** |
| **Last 5 Years:** | **6** |

1. 2010 A. More and B. Taskin, "Simulation-Based Study of On-Chip Antennas", submitted to *IEEE Transactions on Very Large Scale Integration (VLSI) Design.*

2. 2010 J. Lu, Y. Teng and B. Taskin, "A Reconfigurable Clock Polarity Assignment Flow for Clock Gated Designs", submitted to *IEEE Transactions on Very Large Scale Integration (VLSI) Design.*

3. 2010 V. Honkote and B. Taskin, "ZeROA: Zero Clock Skew Synchronization and Load Balancing with Rotary Oscillatory Array", submitted to *IEEE Transactions on Very Large Scale Integration (VLSI) Design.*

4. 2010 J. Lu and B. Taskin, "Clock Buffer Polarity Assignment", submitted to *ACM Transactions on Design Automation and Electronic Design (TODAES).*

5. 2010 Y. Teng and B. Taskin, "Design Guidelines for Rotary Travelling Wave Oscillator Array Considering Skin Effects", submitted to *Journal of Low Power Electronics (JOLPE).*

6. 2010 B. Taskin and P. Nagvajara, "Design-For-Debug in Hardware and Software Design Education", submitted to *ACM Transactions on Computing Education (TCE).*

### 6.5.5 Refereed Conference Publications

| | |
|---|---|
| **Total:** | **36** |
| **At Drexel:** | **30** |
| **Last 5 Years:** | **30** |

1. 2010 V. Honkote and B. Taskin, "Skew-Aware Capacitive Load Balancing for Low-Power Zero Clock Skew Rotary Oscillatory Array", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2010.

2. 2010 A. More and B. Taskin, "Simulation Based Study of On-chip Antennas for a Reconfigurable Hybrid 3D Wireless NoC", *Proceedings of the IEEE International SOC Conference (SOCC)*, September 2010.

3. 2010 A. More and B. Taskin, "Wireless Interconnects for Inter-tier Communication on 3-D ICs", *Proceedings of the European Microwave Integrated Circuits Conference (EuMIC)*, September 2010.

4. 2010 A. More and B. Taskin, "Effect of EMI between Wireless Interconnects and Metal Interconnects on CMOS Digital Circuits", *Mediterranean Microwave Sympoisum (MMS)*, August 2010.

5. 2010 V. Honkote and B. Taskin, "PEEC Based Parasitic Modeling for Power Analysis on Custom Rotary Rings", *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*, August 2010.

6. 2010 A. More and B. Taskin, "Electromagnetic Compatibility of CMOS On-chip Antennas", *Proceedings of the IEEE AP-S International Symposium on Antennas and Propagation (APS-URSI)*, July 2010.

7. 2010 A. More and B. Taskin, "Simulation Based Feasibility Study of Wireless RF Interconnects for 3D ICs", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2010.

8. 2010 J. Lu and B. Taskin, "Clock Tree Synthesis with XOR Gates for Polarity Assignment", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2010.

9. 2010 V. Honkote and B. Taskin, "Design Automation and Analysis of Resonant Rotary Clocking Technology", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2010.

10. 2010 A. More and B. Taskin, "Simulation Based Study of Wireless RF Interconnects for Practical CMOS Implementation", *the Proceedings of the System Level Interconnect Prediction (SLIP)*, June 2010.

11. 2010 A. More and B. Taskin, "Electromagnetic Interaction of On-Chip Antennas and CMOS Metal Layers for Wireless IC Interconnects", *Proceedings of the IEEE/ACM Great Lakes Symposium on VLSI Design (GLSVLSI)*, May 2010.

12. 2010 A. More and B. Taskin, "Leakage Current Analysis for Intra-Chip Wireless Interconnects", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2010, pp. 49–53.

13. 2010 J. Lu and B. Taskin, "Clock Buffer Polarity Assignment Considering Capacitive Load", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2010, pp. 765–770.

14. 2010 V. Honkote and B. Taskin, "Skew Analysis and Bounded Skew Constraint Methodology for Rotary Clocking Technology", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2010, pp. 413–417.

15. 2010 V. Honkote and B. Taskin, "Analysis, Design and Simulation of Capacitive Load Balanced Rotary Oscillatory Array", *Proceedings of the IEEE International Conference on VLSI Design (VLSID)*, January 2010, pp. 218–223.

16. 2009 V. Honkote and B. Taskin, "Skew Analysis and Design Methodologies for Improved Performance of Resonant Clocking", *Proceedings of the IEEE International SOC Conference (ISOCC)*, (invited to special session), November 2009, pp. 165–168.

17. 2009 J. Lu and B. Taskin, "Incremental Register Placement for Low Power CTS", *Proceedings of the IEEE International SOC Conference (ISOCC)*, November 2009, pp. 232–236 (invited to special session).

18. 2009 J. Lu and B. Taskin, "Post-CTS Clock Skew Scheduling with Limited Delay Buffering", *Proceedings of the IEEE International Midwest Sympoisum on Circuits and Systems (MWSCAS)*, August 2009, pp. 224–227.

19. 2009 V. Honkote and B. Taskin, "Design Automation Scheme for Wirelength Analysis of Resonant Clocking Technologies", *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2009, pp. 1147–1150.

20. 2009 V. Honkote and B. Taskin, "Capacitive Load Balancing for Mobius Implementation of Standing Wave Oscillator", *Proceedings of the IEEE International Midwest Symposium Circuits and Systems (MWSCAS)*, August 2009, pp. 232–235.

21. 2009 V. Honkote and B. Taskin, "Zero Clock Skew Synchronization with Rotary Clocking Technology", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2009, pp. 588–593.

22. 2008 V. Honkote and B. Taskin, "Custom Rotary Clock Router", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2008, pp. 114–119.

23. 2008 B. Taskin and J. Lu, "Post-CTS Delay Insertion to Fix Timing Violations", *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2008, pp. 81–84.

24. 2008 S. Kurtas and B. Taskin, "Statistical Timing Analysis of Nonzero Clock Skew Circuits", *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2008, pp. 605–608 [**Best student paper award nominee**].

25. 2008 V. Honkote and B. Taskin, "Maze Router Based Scheme for Rotary Clock Router", *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2008, pp. 442–445.

26. 2007 B. Taskin, A. Chiu, J. Salkind, D. Venutolo, "A Shift-Register-Based QCA Memory Architecture", *Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, October 2007, pp. 54–61.

27. 2007 P. Nagvajara and B. Taskin, "Design-for-Debug: A Vital Aspect in Education", *Proceedings of the International Conference on Microelectronic Systems Education (MSE),* June 2007, pp. 65–66.

28. 2006 B. Taskin and I. S. Kourtev, "A Timing Optimization Method Based on Clock Skew Scheduling and Partitioning in a Parallel Computing Environment," *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2006, pp. 486–490.

29. 2006 B. Taskin, J. Wood and I. S. Kourtev, "Timing-Driven Physical Design for VLSI Circuits Using Resonant Rotary Clocking", *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS),* August 2006, pp. 261–265.

30. 2006 B. Taskin and B. Hong, "Dual-Phase Line-Based QCA Memory Design", *Proceedings of the IEEE Conference on Nanotechnology (IEEE NANO)*, July 2006, pp. 302–305.

31. 2005 B. Taskin and I. S. Kourtev, "Delay Insertion in Clock Skew Scheduling", *Proceedings of the ACM International Symposium on Physical Design (ISPD)*, April 2005, pp. 47–54.

32. 2004 B. Taskin and I. S. Kourtev, "Performance Improvement of Edge-Triggered Sequential Circuits", *Proceedings of the IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, December 2004, pp. 607–610.

33. 2004 B. Taskin and I. S. Kourtev, "Advanced Timing of Level-Sensitive Sequential Circuits", *Proceedings of the IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, December 2004, pp. 603–606.

34. 2004 B. Taskin and I. S. Kourtev, "Time Borrowing and Clock Skew Scheduling Effects on Multi-Phase Level-Sensitive Circuits", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2004, Vol. 2, pp. II-617–620.

35. 2002 B. Taskin and I. S. Kourtev, "Performance Optimization of Single-Phase Level-Sensitive Circuits Using Time Borrowing and Non-Zero Clock Skew", *Proceedings of the ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, December 2002, pp. 111–117.

36. 2002 B. Taskin and I. S. Kourtev, "Linear Timing Analysis of SOC Synchronous Circuits with Level-Sensitive Latches", *Proceedings of the IEEE International ASIC/SOC Conference*, Sep. 2002, pp. 358–362.

### 6.5.6 Refereed Workshop Publications

**Total:** **1**
**At Drexel:** **0**
**Last 5 Years:** **0**

1. 2005 B. Taskin, J. Wood and I. S. Kourtev, "Timing Driven Physcial Design for Digital Synchronous VLSI Circuits Using Resonant Clocking", *Proceedings of the ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, 2005, San Francisco, CA.

### 6.5.7 Other Publications/Posters

**Total:** **13**
**At Drexel:** **13**
**Last 5 Years:** **13**

1. 2010 V. Honkote and B. Taskin, "Design Automation and Analysis of Resonant Rotary Clocking Technology", *IEEE Computer Society's Annual International Symposium on VLSI Design (ISVLSI), Ph.D. forum* poster, Finalist for best Ph.D. dissertation award.

2. 2010 Y. Teng and B. Taskin, "Physical Implementation of Rotary Travelling Wave Oscillator with 0.5um Technology", *ACM SIGDA University Booth* video, ACM/IEEE Design Automation Conference (DAC).

3. 2010 J. Lu and B. Taskin, "Clock Polarity Assignment with XOR gate using IC Compiler", *ACM SIGDA University Booth* video, ACM/IEEE Design Automation Conference (DAC).

4. 2010 Y. Ting, V. Honkote, S. C. Shekar, J. Lu and B. Taskin, "Ic Prototype of Rotary Clocking in 0.5um Semiconductor Technology", *Drexel Research Day* poster.

5. 2010 A. More and B. Taskin, "Electromagnetic Interaction of On-Chip Antennas and CMOS Metal Layers for Wireless IC Interconnects", *Drexel Research Day* poster.

6. 2009 V. Honkote and B. Taskin, "Design Automation and Analysis of Resonant Rotary Clocking Technology in Multi-GHz range", *ACM SIGDA Ph.D. forum* poster, ACM/IEEE Design Automation Conference (DAC).

7. 2009 J. Lu and B. Taskin, "Post-CTS Delay Insertion", *ACM SIGDA University Booth* poster, ACM/IEEE Design Automation Conference (DAC).

8. 2009 A. S. Kurpad, H. Kane, P. Nagvajara, B. Taskin, S. Kalidindi, J. Johnson, "Graphics Processing Units for High-Performance Computing Application in Microstructure Reconstruction Using Phase Recovery Algorithm", *Drexel Research Day* poster.

9. 2008 V. Honkote and B. Taskin, "CROA: Custom Rotary Oscillatory Array", *ACM SIGDA University Booth* poster, ACM/IEEE Design Automation Conference (DAC).

10. 2007 J. DeMaio, O. Farrell, M. Hazeltine, R. Ketner and B. Taskin, "Custom Topology Router for Rotary Clocking", *ACM SIGDA University Booth* poster, ACM/IEEE Design Automation Conference (DAC).

11. 2007 S. M. Kurtas and B. Taskin, "Statistical Timing Verification and Gate Size Optimization of Sub-100nm VLSI Circuits", *Drexel Research Day* poster.

12. 2007 J. DeMaio, O. Farrell, M. Hazeltine, R. Ketner and B. Taskin, "Custom Topology Router for Rotary Clocking", *Drexel Research Day* poster.

13. 2006 B. Taskin and B. Hong, "Towards Quantum-Dot Cellular Array (QCA) Based Nano-Computers", *Drexel Research Day* poster.

### 6.5.8 Theses

**Total: 2**
**At Drexel: 0**
**Last 5 Years: 0**

1. 2005 B. Taskin, *Advanced Timing and Synchronization Methodologies for Digital VLSI Integrated Circuits*, Ph.D. Dissertation, University of Pittsburgh, 2005.

2. 2003 B. Taskin, *Linearization of the Timing Analysis and Optimizaition of Level-Sensitive Synchronous Circuits*, M.S. thesis, University of Pittsburgh, 2003.

### 6.5.9 Funded Research Grants

**Total: 3**
**At Drexel: 3**
**Last 5 Years: 3**

1. 2009
   *Sponsor:* MOSIS
   *Title:* Wireless Integrated Circuit Interconnects for Clocking
   *PI:* B. Taskin
   *Co-Is:* None
   *Amount:* \$valued[1] at ≈ \$200,000
   *Duration:* 2009–2010

2. 2009
   *Sponsor:* National Science Foundation (NSF)
   *Title:* CAREER: Rotary Clock Technology Integration
   *PI:* B. Taskin

[1] A 4×4 mm$^2$ die in a 90nm CMOS process estimated from CMP (http://cmp.imag.fr/products/ic/?p=prices2010)

| | | | |
|---|---|---|---|
| | | *Co-Is:* | None |
| | | *Amount:* | $400,000 |
| | | *Duration:* | 2009–2014 |
| 3. | 2007 | *Sponsor:* | Association of Computing Machinery (ACM) Special Interest Group on Design Automation (SIGDA), "A. Richard Newton Graduate Scholarship", |
| | | *Title:* | Routing for Resonant Clocking Technology in Multi-GHz Range |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $24,000 |
| | | *Duration:* | 2007–2008 |

### 6.5.10 Pending Research Proposals (as of September 2010)

| | |
|---|---|
| **Total:** | **3** |
| **At Drexel:** | **3** |
| **Last 5 Years:** | **3** |

| | | | |
|---|---|---|---|
| 1. | 2010 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | II-NEW: Testbed for High Performance Interconnects |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $823,812 |
| | | *Duration:* | 2011–2014 |
| 2. | 2010 | *Sponsor:* | Department of Energy |
| | | *Title:* | Ultra-Low Power Electronics through Adiabatic Logic and Adiabatic Clocking |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $750,000 |
| | | *Duration:* | 2011-2014 |
| 3. | 2010 | *Sponsor:* | Synopsys Inc. |
| | | *Title:* | Charles Babbage Equipment Grant (effecting courses ECE-E472, ECE-C513, ECE-C661, ECE-C662, ECE-C663, ECE-C673, ECE-E520, ECE-E523) |
| | | *PI:* | Baris Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $100,000 |
| | | *Duration:* | 2010 |

### 6.5.11 Declined Research Proposals

| | |
|---|---|
| **Total:** | **29** |
| **At Drexel:** | **29** |
| **Last 5 Years:** | **29** |

| | | | |
|---|---|---|---|
| 1. | 2010 | *Sponsor:* | Semiconductor Research Corporation (SRC) |
| | | *Title:* | Adiabatically Clocked Adiabatic Circuit Design |

| | | | |
|---|---|---|---|
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $300,000 |
| | | *Duration:* | 2010–2013 |
| 2. | 2010 | *Sponsor:* | Semiconductor Research Corporation (SRC) |
| | | *Title:* | On-Chip Wireless Interconnects |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $450,000 |
| | | *Duration:* | 2010–2013 |
| 3. | 2009 | *Sponsor:* | The Technology Collaborative, Inc. (TTC) |
| | | *Title:* | Prototyping Ultra-Low Power Electronics with Adiabaticity |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $200,584 |
| | | *Duration:* | 2010–2011 |
| 4. | 2009 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | SHF:Small:Wireless IC Interconnects |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | K. R. Dandekar and A. P. Petropulu |
| | | *Amount:* | $528,744 |
| | | *Duration:* | 2010–2013 |
| 5. | 2009 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | SHF:Small:Adiabatic Circuit Design with Adiabatic Clocking |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $486,895 |
| | | *Duration:* | 2010–2013 |
| 6. | 2009 | *Sponsor:* | Synopsys Inc. |
| | | *Title:* | Charles Babbage Equipment Grant (effecting courses ECE-E472, ECE-C513, ECE-C661, ECE-C662, ECE-C663, ECE-C673, ECE-E520, ECE-E523) |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $100,000 |
| | | *Duration:* | 2009 |
| 7. | 2009 | *Sponsor:* | Department of Energy (DoE) |
| | | *Title:* | CAREER: Integrated Adiabatic Switching and Clocking for Ultra-Low Power, Multi-GHz Electronics |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $757,616 |

| | | | |
|---|---|---|---|
| | | *Duration:* | 2010–2015 |
| 8. | 2009 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | II-New: Testbed for Post-CMOS Interconnects |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | K. R. Dandekar and A. P. Petropulu and J. E. Spanier |
| | | *Amount:* | $405,985 |
| | | *Duration:* | 2010–2013 |
| 9. | 2009 | *Sponsor:* | Department of Energy (DoE) |
| | | *Title:* | ARRA: Ultra-Low Power, Multi-GHz Electronics with Nanowired Resonant Clocking |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | J. Spanier |
| | | *Amount:* | $299,774 |
| | | *Duration:* | 2009–2010 |
| 10. | 2009 | *Sponsor:* | Semiconductor Research Corporation (SRC) |
| | | *Title:* | Nanoengineered Resonant Clock Technologies and Networks |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | J. Spanier |
| | | *Amount:* | $40,000 |
| | | *Duration:* | 2009–2010 |
| 11. | 2008 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | IGERT: Wireless Communications As An Alternative to Wired Interconnects Inside a Chip (Internal Competition) |
| | | *PI:* | A. P. Petropulu |
| | | *Co-Is:* | B. Taskin, M. Barsoum, K. Dandekar, A. Fontecchio, A. Daryoush, P. Nagvajara, D. De Carollis, D. Urias, S. Cox |
| | | *Amount:* | $– |
| | | *Duration:* | 2008–2013 |
| 12. | 2008 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | On-Chip Wireless Interconnects |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | K. R. Dandekar, A. P. Petropulu |
| | | *Amount:* | $468,230 |
| | | *Duration:* | 2008–2011 |
| 13. | 2008 | *Sponsor:* | Office of Naval Research (ONR) |
| | | *Title:* | Low-Power, High-Speed Electronics through Resonant Clocking |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $306,895 |
| | | *Duration:* | 2008–2011 |
| 14. | 2007 | *Sponsor:* | Semiconductor Research Corporation (SRC) |

| | | | |
|---|---|---|---|
| | | *Title:* | Improving Power Reduction and Robustness with Clock Skew Scheduling Implemented on a Parallel/Multi-Core Platform |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $300,000 |
| | | *Duration:* | 2008–2011 |
| 15. | 2007 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | CPA-DA: Skew Scheduling for Deep Sub-Micron IC Design |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $373,712 |
| | | *Duration:* | 2008–2011 |
| 16. | 2007 | *Sponsor:* | Synopsys Inc. |
| | | *Title:* | Charles Babbage Equipment Grant (effecting courses ECE-E472, ECE-C513, ECE-C661, ECE-C662, ECE-C663, ECE-C673, ECE-E520, ECE-E523) |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $100,000 |
| | | *Duration:* | 2008 |
| 17. | 2007 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | CAREER: A Roadmap for High Performance Clocking through Resonance and Nanotechnology Integration |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $509,677 |
| | | *Duration:* | 2008–2013 |
| 18. | 2007 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | CI-TEAM: Scientific Computing at Home (Internal Competition) |
| | | *PI:* | P. Nagvajara |
| | | *Co-Is:* | B. Taskin, C. Nwankpa, J. Johnson, S. Kalidindi |
| | | *Amount:* | $– |
| | | *Duration:* | 2007 |
| 19. | 2007 | *Sponsor:* | Semiconductor Research Corporation (SRC) |
| | | *Title:* | Resonant Clock Domains for Multi-Core Processors |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $40,000 |
| | | *Duration:* | 2007–2008 |
| 20. | 2007 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | EMT: Innovative Circuit Design and Synchronization Schemes for QCA-based Computing |

| | | | |
|---|---|---|---|
| | | *PI:* | B. Hong |
| | | *Co-Is:* | B. Taskin |
| | | *Amount:* | $369,602 |
| | | *Duration:* | 2007–2010 |
| 21. | 2007 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | CSR–CPS: Distributed Cyber Physical Architecture for Large-scale State Estimation |
| | | *PI:* | P. Nagvajara |
| | | *Co-Is:* | B. Taskin, C. Nwankpa, J. Johnson |
| | | *Amount:* | $376,607 |
| | | *Duration:* | 2007–2010 |
| 22. | 2006 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | CRI: IAD Computing Platform for Multi-Threaded VLSI CAD |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | B. Hong |
| | | *Amount:* | $223,249 |
| | | *Duration:* | 2007–2010 |
| 23. | 2006 | *Sponsor:* | PA state, GRID: Tobacco Funds |
| | | *Title:* | A Parallel, Reconfigurable Hardware Platform for Health-Related Graph Clustering Problems |
| | | *PI:* | B. Hong |
| | | *Co-Is:* | B. Taskin |
| | | *Amount:* | $76,175 |
| | | *Duration:* | 2006–2007 |
| 24. | 2006 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | CPA: Integrated Circuit Clock Network Design in a Parallel Computing Environment |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | None |
| | | *Amount:* | $278,649 |
| | | *Duration:* | 2007–2010 |
| 25. | 2006 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | EMT: Towards QCA-based Nano-Computers: Exploring Innovative Circuit Design and Synchronization Strategies |
| | | *PI:* | B. Taskin |
| | | *Co-Is:* | B. Hong |
| | | *Amount:* | $345,436 |
| | | *Duration:* | 2006–2009 |
| 26. | 2006 | *Sponsor:* | Association of Computing Machinery (ACM) Special Interest Group on Design Automation (SIGDA) |
| | | *Title:* | A. Richard Newton Scholarship: Delay Insertion for Non-Zero Clock Skew Physical Design |

| | | |
|---|---|---|
| *PI:* | B. Taskin |
| *Co-Is:* | None |
| *Amount:* | $24,000 |
| *Duration:* | 2006–2007 |

27. 2006

| | |
|---|---|
| *Sponsor:* | Association of Computing Machinery (ACM) Special Interest Group on Design Automation (SIGDA) |
| *Title:* | A. Richard Newton Scholarship: Clock Skew Scheduling in a Parallel Computing Environment |
| *PI:* | B. Taskin |
| *Co-Is:* | None |
| *Amount:* | $24,000 |
| *Duration:* | 2006–2007 |

28. 2006

| | |
|---|---|
| *Sponsor:* | Semiconductor Research Corporation (SRC) |
| *Title:* | Resonant Rotary Clocking for Low-Power High-Speed Synchronization |
| *PI:* | B. Taskin |
| *Co-Is:* | None |
| *Amount:* | $375,000 |
| *Duration:* | 2006–2009 |

29. 2006

| | |
|---|---|
| *Sponsor:* | Semiconductor Research Corporation (SRC) |
| *Title:* | Buffer Insertion for Non-Zero Clock Skew Physical Design |
| *PI:* | B. Taskin |
| *Co-Is:* | None |
| *Amount:* | $225,000 |
| *Duration:* | 2006–2009 |

### 6.5.12 Students Supervised to Graduation

| | |
|---|---|
| **Total:** | **4** |
| **At Drexel:** | **4** |
| **Last 5 Years:** | **4** |

**Graduated Ph.D. Students**

1. 2010 Vinayak Honkote, Dissertation title: *Design Automation and Analysis of Resonant Clocking, 08/2010.*

**Graduated M.S. Students**

1. 2010 Jianchao Lu, Research: *Timing Optimization of High-Speed Logic Data Paths*, (continuing Ph.D.).

2. 2007 Shannon M. Kurtas, Thesis title: *Statistical Static Timing Analysis of Non-zero Clock Skew Circuits.*

3. 2007 Yaswanth Simhadri, Research: *Simulator for Quantum-Dot Cellular Automata.*

### 6.5.13 Current Graduate Students

| | |
|---|---|
| **Total:** | **8** |
| **At Drexel:** | **8** |
| **Last 5 Years:** | **8** |

**Current Ph.D. Students:**

1. 2007 Jianchao Lu, Ph.D. candidate, expected 2011, Topic: *Low-power Clock Network Synthesis and Timing.*

2. 2009 Ankit More, Ph.D. candidate, expected 2013, Topic: *Wireless IC Interconnects.*

3. 2009 Ying Teng, Ph.D. candidate, expected 2013, Topic: *Resonant Adiabatic Clocking and Adiabatic Circuit Design.*

4. 2009 Matthew Zimmerman, B.S./Ph.D. student, Topic: *Memristor based logic design.*

**Current M.S. Students:**

1. 2009 Xiaomi Mao, M.S., expected 2011, Topic: *IC Timing Optimization through Delay Insertion*

2. 2009 Sharat C. Shekar, M.S., expected 2011, Topic: *Ultra-Low Power Adiabatic Circuits*

3. 2007 Abizer Nayeem, B.S./M.S., expected 2010, Topic: *Nanotube modeling on Resonant Rotary Clocking Network .*

4. 2006 John Vargas, M.S. (part-time), Topic: *Physical Design for 3D Ic Interconnects.*

### 6.5.14 Undergraduate Student Research Supervision

| | |
|---|---|
| **Total:** | **13** |
| **At Drexel:** | **13** |
| **Last 5 Years:** | **13** |

1. 2010 Yi Li (female), *Quantum-dot cellular automata architectures.*

2. 2010 Michael Edoror (REU scholar from University of Maryland, African-American), *Automation of Rotary Clock Router.*

3. 2010 Abdalla Musmar (REU scholar from An-Najah University, Arab-American), *Block-based adiabatic logic design.*

4. 2010 Yusuf Aksehir (international summer scholar from Sabanci University), *Clock network design.*

5. 2010 Bo Hyun Kim (summer scholar from Carnegie Mellon University, graduate school at Columbia University, female), *Transistor-level adiabatic logic design.*

6. 2008 S. Kutal Gokce (international summer scholar from Middle East Technical University, graduate school at Koc University and the University of Texas, Austin), *Rotary clock design.*

7. 2008 Can Hankendi (international summer scholar from Sabanci University, graduate school at the University of Southern California), *Reconvergence check in graphs.*

8. 2007 Daniel Levin, *Graphic Processing Units in Computing Fourier Representation of Microstructure Distribution Functions* [co-advised with P. Nagvajara].

9. 2007 James Kerak, *QCA logic design.*

10. 2007 Hahne Kane (female), *FFT implementation using GPUs* [co-advised with P. Nagvajara].

11. 2006–2007 Danh Nguyen (graduate school at Drexel University), *Non-zero clock skew clock tree synthesis algorithms.*

12. 2006–2007 Austin Tran (graduate school at Drexel University), *Grid-topology clock networks.*

13. 2006–2007 Vedant Vyas, *Quantum-dot cellular automata architectures.*

## 6.6 Teaching Activities

This section details my teaching activities, including courses taught, developed, supervised design activities (senior/freshman design), educational funding activity (current, pending, declined proposals) and teaching awards.

### 6.6.1 Summary of Courses Taught and Student Evaluations

| | |
|---|---|
| **Total:** | **34** |
| **At Drexel:** | **34** |
| **Last 5 Years:** | **34** |

The following lists the courses taught in Fall (F), Winter (W), and Spring (Sp) terms of each of the years since the beginning of the academic year 2005–2006. Graduate courses and undergraduate courses are denoted as G and UG respectively. Course evaluation data is provided using both the mean and standard deviation of the "overall instructor rating" for the respective course.

| | Term | Level | Number | Title | Particip. Students | Avg. Eval. | Std. Dev. |
|---|---|---|---|---|---|---|---|
| S | 2009–10 | UG | ENGR 232 | Dynamic Engineering Systems | 23 | –[2] | – |
| S | 2009–10 | UG | ENGR 232 | Dynamic Engineering Systems | 24 | – | – |
| Sp | 2009–10 | G | ECE-C673 | DSM IC Design | 8 | – | – |
| Sp | 2009–10 | G | ECE-C690 | ASIC Design II | 5 | – | – |
| Sp | 2009–10 | UG | ECE-4690 | ASIC Design II | 10 | – | – |
| W | 2009–10 | G | ECE-C672 | EDA for VLSI Circuits II | 7 | – | – |
| W | 2009–10 | G | ECE-C690 | ASIC Design I | 6 | – | – |
| W | 2009–10 | UG | ECE-C490 | ASIC Design I | 10 | – | – |
| F | 2009–10 | G | ECE-C671 | EDA for VLSI Circuits I | 9 | – | – |
| F | 2009–10 | G | ECE-C690 | Custom VLSI Design | 5 | – | – |
| F | 2009–10 | UG | ECE-C490 | Custom VLSI Design | 18 | – | – |
| | | | | | | | |
| Sp | 2008–09 | UG | ECE-C490 | Modern VLSI IC Design | 2/9 | 5.0/5.0 | 0.00 |
| W | 2008–09 | UG | ECE-C490 | VLSI Design and Automation | 5/16 | 2.6/5.0 | 0.28 |
| W | 2008–09 | UG | ENGR 232 | Dynamic Engineering Systems | 15/28 | 4.5/5.0 | 0.04 |
| W | 2008–09 | UG | ENGR 232 | Dynamic Engineering Systems | 11/27 | 3.8/5.0 | 0.01 |
| F | 2008–09 | UG | ENGR 231 | Linear Engineering Systems | 28 | – | – |
| F | 2008–09 | UG | ENGR 231 | Linear Engineering Systems | 29 | – | – |
| F | 2008–09 | UG | ECE-C490 | Introduction to VLSI Design | 14 | – | – |
| | | | | | | | |
| S | 2007–08 | UG | ENGR 232 | Dynamic Engineering Systems | 30 | – | – |
| S | 2007–08 | UG | ENGR 232 | Dynamic Engineering Systems | 30 | – | – |
| Sp | 2007–08 | UG | ECE-200 | Digital Logic Design | 24 | – | – |
| Sp | 2007–08 | UG | ECE-200 | Digital Logic Design | 17 | – | – |
| Sp | 2007–08 | UG | ECE-C490 | Modern VLSI IC Design | 7 | – | – |
| W | 2007–08 | UG | ECE-C490 | VLSI Design and Automation | 7 | – | – |
| W | 2007–08 | UG | ENGR 232 | Dynamic Engineering Systems | 28 | – | – |
| W | 2007–08 | UG | ENGR 232 | Dynamic Engineering Systems | 13 | – | – |
| F | 2007–08 | UG | ECE-C490 | Introduction to VLSI Design | 11 | – | – |

[2]Courses wihout evaluation numbers either were not available due to technical problems in the system or did not have enough participation for reporting.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| F | 2007–08 | UG | ECE-C203 | Programming for Engineers[3] | 9 | – | – |
| Sp | 2006–07 | G | ECE-C673 | Deep Sub-Micron IC Design | 2/9 | 5.0/5.0 | 0 |
| W | 2006–07 | G | ECE-C672 | EDA for VLSI Circuits II | 1/5 | 5.0/5.0 | 0 |
| F | 2006–07 | G | ECE-C671 | EDA for VLSI Circuits I | 3/8 | 5.0/5.0 | 0 |
| Sp | 2005–06 | G | ECE-C673 | Deep Sub-Micron IC Design | 1/7 | 4.0/5.0 | 0 |
| W | 2005–06 | G | ECE-C672 | EDA for VLSI Circuits II | 4/10 | 4.5/5.0 | 0.5 |
| F | 2005–06 | G | ECE-C671 | EDA for VLSI Circuits I | 5/11 | 4.8/5.0 | 0.4 |

### 6.6.2 Undergraduate Courses Taught (as lecturer)

**Total:** **4**
**At Drexel:** **4**
**Last 5 Years:** **4**

1. **Programming for Engineers (ECE-C203)**
   This course presents an introduction to programming with a special emphasis on engineering applications. *One of the first courses* taught at Burlington County College (BCC) as a part of the "Drexel at BCC" initiative by a faculty member of the Drexel ECE Department and *the only one to be ever taught by a tenure-track assistant professor*. Course includes lectures and laboratory sessions.

2. **Custom VLSI Design (previously Introduction to VLSI Design) (ECE-C490)**
   This course is an introductory course in the field of Very Large Scale Integration (VLSI) circuits and system design. Systematic understanding, design and analysis of VLSI integrated circuits are covered. The course begins with a review of CMOS transistor operation and semiconductor manufacturing process. Logic design with CMOS transistors and circuit families are described. Layout, design rules and circuit simulation are addressed. The course includes lectures and laboratory sessions. Laboratory manuals are developed on the use of custom VLSI circuit schematic/layout design, extraction and simulation tools.

3. **ASIC Design I (previously VLSI Design and Automation) (ECE-C490)**
   This is course in the field of VLSI circuits and systems design. Design and analysis of VLSI integrated circuits are covered from a systems design perspective. The course exclusively covers digital CMOS design for application-specific-integrated circuit (ASIC) implementations. Integrated circuit physical design flows are presented. System timing principles and arithmetic building blocks are presented. Electronic design automation principles are covered through hands-on practive using VLSI CAD tools in the required laboratory sessions. Laboratory manuals are developed for the use of CAD tools in ASIC logic synthesis, floorplanning, placement, routing, clock tree synthesis and timing verification.

4. **ASIC Design II (previously Modern VLSI IC Design) (ECE-C490)**

[3]Course taught at the Burlington County College (BCC) as a part of the "Drexel at BCC" program.

This is a project-oriented course in the field of VLSI circuit and system design targeted towards a digital ASIC implementation. A quarter-long, high-complexity project is assigned to students working in teams. Team-work, task assignment and team communication are mediated in an industry setting, simulating a realistic design environment. Design tasks cover the entire IC design flow range, from system specification to RTL description to verification. Successful designs are send to MOSIS for fabrication. Laboratory manuals are developed to utilize the ASIC physical design tools to perform high-complexity projects, such as a floating point unit or a microprocessor.

### 6.6.3 Graduate Courses Taught (as lecturer)

| | |
|---|---|
| **Total:** | **6** |
| **At Drexel:** | **6** |
| **Last 5 Years:** | **6** |

1. **EDA for VLSI Circuits I (ECE-C671)**
This course is the first of a two-course-sequence that focuses on the electronic design automation techniques in the physical design process of digital VLSI circuits. In this course, electronic design automation (EDA) techniques are discussed in theory and implementation in order to build CAD tools for VLSI design (instead of using/analyzing commercially available tools). In this first quarter of the course, algorithms, techniques and heuristics structuring the foundations of contemporary VLSI CAD tools are presented. Within this context, common data structures used for computer manipulation of circuit design data are analyzed. Optimization, satisfiability, graph theory and boolean algebra topics are presented.

2. **EDA for VLSI Circuits II (ECE-C672)**
This course is the second of a two-course-sequence that focuses on the electronic design automation techniques in the physical design process of digital VLSI circuits. In this course, electronic design automation (EDA) techniques are discussed in theory and implementation in order to build CAD tools for VLSI design (instead of using/analyzing commercially available tools). In this second quarter of the course, the emphasis is on the fundamentals and design automation of the VLSI physical design flow. Various physical design flow steps including technology mapping, partitioning, floorplanning, placement, routing and timing are analyzed in detail. Team-based, small-to-medium scale programming projects are an integral part of the course.

3. **Deep Sub-Micron IC Design (ECE-C673)**
This course focuses on the design challenges of digital VLSI integrated circuits in deep sub-micron (e.g. nanometer) manufacturing technologies. Topics of interest include electronic design automation (EDA) challenges due to increased design complexities and high-performance circuit design techniques such as low-power and variation-aware design. The impacts of nanometer scaling on CMOS technology are discussed extensively within the contexts of interconnect planning, buffer insertion, signal integrity, power distribution, clock tree synthesis, low power circuit design and design for manufacturing (DFM). The course is structured on recent presentations, articles and tutorials from the industry and academia; advancing the discussions to state-of-the-art VLSI design techniques. The course material is delivered in a lecture format.

4. **Custom VLSI Design (ECE-C490)**
Starting Fall 2009, this course is crosslisted for graduate students due to increasing demand.

5. **ASIC Design I (ECE-C690)**
Starting Winter 2010, this course is crosslisted for graduate students.

6. **ASIC Design II (ECE-C690)**
Starting Spring 2010, this course is crosslisted for graduate students.

### 6.6.4 New Courses Developed

| | |
|---|---|
| **Total:** | **6** |
| **At Drexel:** | **6** |
| **Last 5 Years:** | **6** |

1. 2005-06 **EDA for VLSI Circuits I (ECE-C 671)**
This course is the first of a two-course-sequence that focuses on the electronic design automation techniques in the physical design process of digital VLSI circuits.

2. 2005-06 **EDA for VLSI Circuits II (ECE-C 672)**
This course is the second of a two-course-sequence that focuses on the electronic design automation techniques in the physical design process of digital VLSI circuits.

3. 2005-06 **Deep Sub-Micron IC Design (ECE-C 673)**
This course focuses on the design challenges of digital VLSI integrated circuits in deep sub-micron (e.g. nanometer) manufacturing technologies.

4. 2007-08 **Custom VLSI Design (ECE-C490/690)**
This course is an introductory course in the field of Very Large Scale Integration (VLSI) circuits and system design. The course was initially developed as "Introduction to VLSI Design", renamed and crosslisted as a graduate course in AY 2009-10.

5. 2007-08 **ASIC Design I (ECE-C490/690)**
This is course in the field of VLSI circuits and systems design. Design and analysis of VLSI integrated circuits are covered from a systems design perspective. The course was initially developed as "VLSI Design and Automation", renamed and crosslisted as a graduate course in AY 2009-10.

6. 2007-08 **ASIC Design II (ECE-C490/690)**
This is a project-oriented course in the field of VLSI circuit and system design targeted towards a digital ASIC implementation. The course was initially developed as "Modern VLSI IC Design", renamed and crosslisted as a graduate course in AY 2009-10.

### 6.6.5 Senior Design Projects Supervised

| | |
|---|---|
| **Total:** | **7** |
| **At Drexel:** | **7** |
| **Last 5 Years:** | **7** |

1. *Title:* Scalability of Rotary Traveling-wave Oscillators 2009–2010
*Students:* Eric Fargnoli, Colby Weingarten
*Recognition:* Drexel ECE award

| | | | |
|---|---|---|---|
| 2. | *Title:* | Design of an Addressable Internetworked Microscale Sensor | 2008–2009 |
| | *Students:* | Daniel Oakum, Gerre Strait, Kyle Yencha, Matthew Zofchak | |
| | *Recognition:* | IEEE International Conference on Computer Design (ICCD) 2010 paper (submitted) | |
| 3. | *Title:* | Serial Memory Design Using QCA Nanoarchitectures | 2006–2007 |
| | *Students:* | Andy Chiu, Jonatan Salkind, Daniel Venutolo | |
| | *Recognition:* | ACM Journal of Emerging Technologies in Computing Systems (JETC) Vol. 5, No. 1, Article 4, January 2009; IEEE Symposium on Nanoscale Architectures (NANOARCH) 2007 publication | |
| 4. | *Title:* | Automated Clock Signal Router for the 36 GHz Processor | 2006–2007 |
| | *Students:* | Joseph DeMaio, Owen Farrell, Michael Hazeltine, Ryan Ketner | |
| | *Recognition:* | ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 14, No.3, Article 44, May 2009; SIGDA University Booth Presentation at the IEEE/ACM Design Automation Conference 2007; Drexel ECE Computer Engineering Award | |
| 5. | *Title:* | Scalable Implementation of Graph Clustering Algorithms Using the IBM Cell Processor [co-advised with B. Hong] | 2006–2007 |
| | *Students:* | Mary Vuong, Ana L. Silva, Nemanja Milosavljevic, Jonathan Gevaryahu | |
| | *Recognition:* | IBM Cell Processor Programming Challenge Entry | |
| 6. | *Title:* | Realizing Arbitrary Boolean Functions with Threshold Logic Units [co-advised with B. Katz] | 2006–2007 |
| | *Students:* | James Cantwell, Matthew Kordbegli, Jason Meyers, Scott Meyers | |
| 7. | *Title:* | Software Implementation of Logic Gate Sizing | 2005–2006 |
| | *Students:* | David Dimm, Roshani Patel | |

### 6.6.6 Freshman Design Projects Supervised

**Total:** **1**
**At Drexel:** **1**
**Last 5 Years:** **1**

| | | | |
|---|---|---|---|
| 1. | *Title:* | Pressure Sensitive Brake Light System | 2005–2006 |
| | *Students:* | John Burke, George D'Andrea, Dave Grunwald, Jeffrey C. Lenger, Michael Zacharkow | |

### 6.6.7 Funded Educational Grants

**Total:** **1**
**At Drexel:** **1**
**Last 5 Years:** **1**

| | | | |
|---|---|---|---|
| 1. | 2009 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | REU Site: Computing for Power and Energy: The Old, The New and The Renewable |

*PI:* Baris Taskin
*Co-Is:* None
*Amount:* $360,000
*Duration:* 2010–2013

### 6.6.8 Pending Educational Proposals (as of September 2010)

**Total:** **1**
**At Drexel:** **1**
**Last 5 Years:** **1**

1. 2010
   *Sponsor:* National Science Foundation (NSF)
   *Title:* BPC-A: Collaborative:Scratch Me In: Computer Science Instruction and Mentoring for High School Students Traditionally Underrepresented in Computing Professions
   *PI:* N. Kandasamy
   *Co-Is:* A. K. Fontecchio, J. R. Johnson, B. Taskin, D. Mosse'
   *Amount:* $870,324
   *Duration:* 2010–2013

### 6.6.9 Declined Educational Proposals

**Total:** **6**
**At Drexel:** **6**
**Last 5 Years:** **6**

1. 2008
   *Sponsor:* HP Inc.
   *Title:* HP Technology for Teaching Grant Initiative
   *PI:* B. Taskin
   *Co-Is:* None
   *Amount:* $77,000
   *Duration:* 2008

2. 2007
   *Sponsor:* National Science Foundation (NSF)
   *Title:* REU Site: Scientific Computing with Exotic Architectures
   *PI:* B. Taskin
   *Co-Is:* P. Nagvajara
   *Amount:* $367,496
   *Duration:* 2008–2011

3. 2008
   *Sponsor:* National Science Foundation (NSF)
   *Title:* Effective Learning Techniques for Diagnostic Design
   *PI:* P. Nagvajara
   *Co-Is:* F. K. Reisman, B. Taskin
   *Amount:* $208,412
   *Duration:* 2008–2010

4. 2007
   *Sponsor:* National Science Foundation (NSF)
   *Title:* CCLI: Course Modules in Electronic Design for Manufacturing and Sustainability
   *PI:* P. Nagvajara

| | | | |
|---|---|---|---|
| | | *Co-Is:* | B. Taskin, C. Nwankpa |
| | | *Amount:* | $149,991 |
| | | *Duration:* | 2007–2009 |
| 5. | 2007 | *Sponsor:* | National Science Foundation (NSF) |
| | | *Title:* | CPATH CB: A Plan to Revitalize Computer Engineering Education |
| | | *PI:* | Prawat Nagvajara |
| | | *Co-Is:* | B. Taskin, B.C. Chang, C. Nwankpa, J. Wen |
| | | *Amount:* | $396,798 |
| | | *Duration:* | 2007–2009 |
| 6. | 2006 | *Sponsor:* | Department of Education |
| | | *Title:* | GAANN–BRIDGE: Biological Research in Inter-Disciplinary Graduate Education (internal competition) |
| | | *PI:* | Mohana Shankar |
| | | *Co-Is:* | B. Taskin, H. Sethu, T. Kurzweg, N. Kandasamy, B. Hong, Y. Kim, and G. Rosen |
| | | *Amount:* | $1,036,848 |
| | | *Duration:* | 2007–2010 |

### 6.6.10 Teaching Awards

| | |
|---|---|
| **Total:** | **2** |
| **At Drexel:** | **2** |
| **Last 5 Years:** | **2** |

| | **Date** | **Award** |
|---|---|---|
| 1. | 2009–2010 | ECE Department “ECE” Senior Design Advisor Award |
| 2. | 2006–2007 | ECE Department “Computer Engineering” Senior Design Advisor Award |

## 6.7 Professional Service Activities

This section details my professional service activities, including society memberships, conference/workshop services, personal development and reviewing activity.

### 6.7.1 Professional Society Membership

| | |
|---|---|
| **Total:** | **2** |
| **At Drexel:** | **2** |
| **Last 5 Years:** | **2** |

| | Date | Activity |
|---|---|---|
| 1. | 2005–pres. | Member, Association of Computing Machinery (ACM)–Special Interest Group on Design Automation (SIGDA) |
| 2. | 2000–pres. | Member, Institute of Electrical and Electronics Engineers (IEEE) |

### 6.7.2 Conference/Workshop Committee Memberships

| | |
|---|---|
| **Total:** | **21** |
| **At Drexel:** | **21** |
| **Last 5 Years:** | **21** |

**Steering Committee Membership**

| | | |
|---|---|---|
| 1. | 2007–pres. | International Midwest Sympoisum on Circuits and Systems (MWSCAS) |

**Track Chair**

| | | |
|---|---|---|
| 2. | 2009, 2010 | International Midwest Symposium on Circuits and Systems (MWSCAS) "*CAD*" track chair |
| 3. | 2008 | International Midwest Symposium on Circuits and Systems (MWSCAS) "*VLSI*" track co-chair |

**Technical Program Committee Membership**

| | | |
|---|---|---|
| 4. | 2011 | IEEE Microelectronics Systems Education (MSE) |
| 5. | 2010 | IEEE International Conference on Computer Design (ICCD) |
| 6. | 2010 | IEEE/ACM Asia Symposium on Quality Electronic Design (ASQED) |
| 7. | 2009, 2010 | International Symposium on Nanoscale Architectures (NANOARCH) |
| 8. | 2008, 2009, 2010 | International Great Lakes Symposium on VLSI (GLSVLSI) |
| 9. | 2008 | Int'l Conference on Modeling, Simulation and Applied Optimization (ICMSAO) |
| 10. | 2006 | First International Workshop on Future Computing Technologies |

**Local Arrangements Committee Membership**

| | | |
|---|---|---|
| 11. | 2006 | IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI) |

**Academic Coordinator**

| | | |
|---|---|---|
| 12. | 2008, 2009, 2010 | ACM Special Interest Group on Design Automation (SIGDA) University Booth |

### 6.7.3 Panel Discussant at Conference/Workshop

**Total:** **1**
**At Drexel:** **1**
**Last 5 Years:** **1**

1. 2010 International Workshop on System Level Interconnect Prediction (SLIP)
   New Performance Prediction Techniques for Interconnects

### 6.7.4 Conference/Workshop Sessions Chaired/Organized

**Total:** **10**
**At Drexel:** **10**
**Last 5 Years:** **10**

1. 2011 IEEE International Conference on Computer Design (ICCD)
   "*Power and Thermal Analysis and Optimization*" session chair

2. 2010 IEEE International Great Lakes Symposium on VLSI (GLSVLSI)
   "*Emerging Technologies*" session chair

3. 2010 IEEE International Conference on Quality Electronic Design (ISQED)
   "*Clocking Strategy for Modern Low Power Multi-Core and Structured ASICs*" session chair

4. 2009 International Midwest Symposium on Circuits and Systems (MWSCAS)
   "*CAD and Layout*" session chair

5. 2009 International IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)
   "*Session III*" session chair

6. 2008 International Midwest Symposium on Circuits and Systems (MWSCAS)
   "*SOC Design*" session chair

7. 2008 International Midwest Symposium on Circuits and Systems (MWSCAS)
   "*VLSI Architectures*" session chair

8. 2007 International Midwest Symposium on Circuits and Systems (MWSCAS)
   "*VLSI Architectures*" session chair

9. 2007 International Midwest Symposium on Circuits and Systems (MWSCAS)
   "*Digital Circuits Design*" session chair

10. 2006 International Midwest Symposium on Circuits and Systems (MWSCAS)
    "*Digital Circuits Design*" session chair

### 6.7.5 Professional Development Conferences

**Total:** **3**
**At Drexel:** **2**
**Last 5 Years:** **3**

| | Date | Conference |
|---|---|---|
| 1. | 2006 | Grant Writing Workshop, Drexel University, Philadelphia, PA<br>1-day workshop intended for NIH, DoE and other governmental agencies |
| 2. | 2005 | NSF Regional Grants Workshop, Orlando, FL<br>3-day workshop which is "...a must, particularly for new faculty, researchers, educators, and administrators who want to gain key insight into a wide range of important and timely issues at NSF: the state of current Grants; the proposal and award process; and current and recently updated policies and procedures." |
| 3. | 2004 | Grantspersonship Workshop, Pittsburgh, PA<br>2-day workshop intended for all governmental and military agencies |

### 6.7.6 Reviews and Panels

| | |
|---|---|
| **Total:** | **39** |
| **At Drexel:** | **34** |
| **Last 5 Years:** | **39** |

| | | |
|---|---|---|
| 1. | 2010 | IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI) |
| 2. | 2010 | ACM Journal of Emerging Technologies (JETC) |
| 3. | 2010 | Elsevier Microelectronics Journal |
| 4. | 2010 | Elsevier Integration, the VLSI Journal |
| 5. | 2010 | IET Electronic Letters |
| 6. | 2010 | ACM/IEEE International Symposium on Nanoscale Architectures (NANOARCH) |
| 7. | 2010 | Asia Pacific Conference on Circuits and Systems (APCCAS) |
| 8. | 2010 | Journal of Zheijang University |
| 9. | 2010 | Kuwait Journal of Science and Engineering |
| 10. | 2010 | National Science Foundation (NSF) panel 2 of 2 in 2010 |
| 11. | 2010 | National Science Foundation (NSF) panel 1 of 2 in 2010 |
| 12. | 2009 | ACM/IEEE International Symposium on Nanoscale Architectures (NANOARCH) |
| 13. | 2009 | European Conference on Circuit Theory and Design (ECCTD) |
| 14. | 2009 | IEEE International Conference on VLSI Design (VLSID) |
| 15. | 2009 | IEEE International Symposium on VLSI Design (ISVLSI) |

16. 2009 IEEE International Great Lakes Symposium on VLSI (GLSVLSI)
17. 2008 IEEE Transactions on Nanotechnology (TNANO)
18. 2008 Elsevier Microelectronics Journal
19. 2008 ACM Journal of Emerging Technologies (JETC)
20. 2008 IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)
21. 2008 IEEE International Conference on VLSI Design (VLSID)
22. 2008 ACM Transactions on Design Automation of Electronic Systems (TODAES)
23. 2008 IEEE International Great Lakes Symposium on VLSI (GLSVLSI)
24. 2008 National Science Foundation (NSF) panel
25. 2007 National Science Foundation (NSF) panel
26. 2007 IEEE Transactions on Education (T.Ed.)
27. 2007 IEEE Transactions on Nanotechnology (TNANO)
28. 2007 IEEE International Symposium on VLSI Design (ISVLSI)
29. 2007 ACM Transactions on Design Automation of Electronic Systems (TODAES)
30. 2006 International Journal of Computers and Their Applications (J. Comp.)
31. 2006 IEEE Asia Pacific Conference on Circuits and Systems (ASPCAS)
32. 2006 Gazi University Technical Journal
33. 2006 International Workshop on Future Computing Technologies
34. 2006 Springer Book Review
35. 2005 International Journal of Computers and Their Applications (J. Comp.)
36. 2004 IEEE International Symposium on Circuits and Systems (ISCAS)
37. 2004 ACM/IEEE International Workshop on Timing Issues (TAU)
38. 2004 IEEE International Conference on Electronics, Circuits and Systems (ICECS)
39. 2003 IEEE Transactions on Very Large Scale Integration (VLSI) systems (TVLSI)

## 6.8 University Service Activities

This section details my university service activities, including responsibilities in departmental and graduate student committees, CoE outreach activities, student group advising and received service awards.

### 6.8.1 Member of Department Committees

**Total:** **1**
**At Drexel:** **1**
**Last 5 Years:** **1**

| | Date | Position |
|---|---|---|
| 1. | 2007–pres. | Faculty Recruitment Committee |

### 6.8.2 Member of University Committees

**Total:** **2**
**At Drexel:** **2**
**Last 5 Years:** **2**

| | Date | Position |
|---|---|---|
| 1. | 2008 | Barry M. Goldwater Scholarship Review Committee |
| 2. | 2010 | Fullbright Scholarship Review Committee |

### 6.8.3 M.S. Thesis Committees Served

**Total:** **5**
**At Drexel:** **5**
**Last 5 Years:** **5**

| | Date | Student [Advisor (if other)] |
|---|---|---|
| 1. | 2008 | Nakul Jain [Advisor: N. Kandasamy] |
| 2. | 2008 | Shahab Ahmad [Advisor: N. Kandamsamy] |
| 3. | 2007 | Shannon M. Kurtas |
| 4. | 2006 | Zayd Hammoudeh [Advisors: N. Kandasamy & M. Kam] |
| 5. | 2005 | Jeng L. Yang [Advisor: P. Nagvajara] |

### 6.8.4 Ph.D. Candidacy Exam and Proposal Committees Served

**Total:** **7**
**At Drexel:** **7**
**Last 5 Years:** **7**

| | Date | Student [Advisor (if other)] |
|---|---|---|
| 1. | 2010 | Scott Haney [L. Hrebien and M. Kam] |
| 2. | 2009 | Ying Teng |
| 3. | 2009 | Ankit More |
| 4. | 2009 | Takashi Nakamura [C. Chang] |
| 5. | 2009 | James Shackleford [N. Kandasamy] |
| 6. | 2007 | Jianchao Lu |

| | | |
|---|---|---|
| 7. | 2006 | Vinayak Honkote |

### 6.8.5 Ph.D. Defense Committees Served

**Total:** **2**
**At Drexel:** **1**
**Last 5 Years:** **2**

| | | |
|---|---|---|
| 1. | 2010 | Vinayak Honkote<br>Dissertation title: *Design Automation and Analysis of Resonant Clocking* |
| 2. | 2008 | Atanu Chattopadhyay (McGill University) [Z. Zelic]<br>Dissertation title: *Dual Reference Signal, Post-Silicon Reconfigurable Clock Distribution Networks* |

### 6.8.6 University Outreach Activities

**Total:** **8**
**At Drexel:** **8**
**Last 5 Years:** **8**

| | **Date** | **Activity** |
|---|---|---|
| 1. | 2010 | "NSF REU Site: Computing for Power and Engineering" PI and academic coordinator hosting ten (10) undergraduate students from the nation in three (3) departments (ECE, MEM, MSE) |
| 2. | 2007–2010 | College of Engineering open houses |
| 3. | 2009–2010 | Computer Engineering representative for ECE student visits |
| 4. | 2009 | Summer Engineering Experience at Drexel (SEED) Program (Lego-bot experiments with P. Nagvajara) |
| 5. | 2010 | Drexel Research Day Judge |
| 6. | 2008 | Drexel Research Day Judge |
| 7. | 2007 | Drexel Research, Innovation, Scholarship and Creativity (RISC) Day Judge |
| 8. | 2006 | Drexel Research, Innovation, Scholarship and Creativity (RISC) Day Judge |

### 6.8.7 University Student Group Advising

**Total:** **1**
**At Drexel:** **1**
**Last 5 Years:** **1**

| | **Date** | **Activity** |
|---|---|---|
| 1. | 2007–2009 | Applied Creativity Student Association (ACSA), Advisory Board Member |

### 6.8.8 University Service Awards

**Total:** **1**
**At Drexel:** **0**
**Last 5 Years:** **1**

| | **Date** | **Award** |
|---|---|---|
| 1. | 2005 | "Student Leadership Award", Student Government Board, University of Pittsburgh, Pittsburgh, PA |

# 7 Student Comments

*The following lists a sampling of anonymous comments provided by students through course evaluation surveys conducted by Drexel University in courses taught by Baris Taskin.*

### General Engineering Courses – Linear Algebra and Differential Equations: ENGR 231, ENGR 232

- "Taskin is really good at explaining the actual math behind everything we did on the labs. He is very easy to talk to and ask questions"
- "Strengths - Challenged students and provided good information following lecture to be aware of. Weaknesses - Required far too in depth justification of methods used."
- "Taskin should be the instructor for the lectures. I believe he would have done a much better job"
- "Strengths - Insanely helpful, does not just give away answers, but makes you think. Also, asks you to explain answers to prove what you are learning and relate it back to classroom material"
- "Strengths: Was very knowledgable and was able to answer any questions I had. Was able to explain concepts to me which I didn't not learn from lecture."
- "Baris Taskin was a good teacher. He understood the labs and what we needed to accomplish."
- "Baris was great. I learned a lot because he made me work through problems instead of telling me the answers."
- "Baris is a good guy, funny. [TA] is very nervous, she makes me feel anxious. but that's ok. they both try very hard. A+"

### Computer Engineering Undergraduate and Graduate Courses – VLSI and EDA: ECE-C490/ECE-C690, ECE-C671, ECE-C672, ECE-C673

- "Strengths: Extremely knowledgeable Very helpful and friendly Clear and understandable explainations Weaknesses: None"
- "Prepared for lectures. Open for discussion. Slides could be better prepared / organized."
- "Healthy workload, but very relevant and current material. We need more VLSI at this school"
- "Strengths: The only course–part of a course sequence actually– on VLSI CAD algorithms at Drexel, taught very well, by a great instructor."
- "Course is not for the feignt of heart. Requires a solid background in digital design and computer structures."
- "We need more of this kind of courses."
- "Knowledgeable, fair, energetic."
- "Strengths: Knowledgable, able to explain clearly"
- "He is really concentrated in teaching this class and humorous."
- "Strengths: - Good communication skills - Takes personal interest in making sure students keep-up with the course"
- "Prof Taskin always seems to have the time to address the students problems. Accessible, Intense/interesting lecture delivery, Encourages full class participation."
- " Strengths: Helpful and approachable. Great Oratory skills. Very Encouraging & open to discussion any time. Great Motivator."
- "Full of passion."
- "Engages the students very well, makes the course interesting"

- "strengths: Pays excellent individual attention to every student, encourages individual/group research work, makes the class very interesting and interactive."
- "Strengths: – Listens to student's concerns/complaints, however, is uncompromising in terms of expected workload. – Talented lecturer"
- "Gives a good overview of objectives of the course"
- "Strengths: Reflect the current trend in EDA in depth"
- "Dr. Taskin is very well prepared for class and can answer questions on-the-fly. However, he could work at speeking more clearly and slowly."
- "This class is close to real application and it is useful."
- "Strengths: Perfect logical flow. Concise and to the point. Clear goals. Perfectly supplemented by having projects that make us implement methodologies that are relevant today and 5 years from now."

# 8 Syllabi for the Six (6) New Courses

| | | |
|---|---|---|
| 1. | ECE-C 490/690 | Special Topics: Custom VLSI Design |
| 2. | ECE-C 490/690 | Special Topics: ASIC Design I |
| 3. | ECE-C 490/690 | Special Topics: ASIC Design II |
| 4. | ECE-C 671 | EDA for VLSI Circuits I |
| 5. | ECE-C 672 | EDA for VLSI Circuits II |
| 6. | ECE-C 673 | Deep Sub-Micron VLSI Design |

ECE-C 490/690 ST: Custom VLSI Design — Syllabus
Fall 2009 — Lec: Mon 10:00-11:50am
Prof. Baris Taskin — Lab: Wed 9:00am-10:50am

## Course Information

| | |
|---|---|
| Course Title: | ST: Custom VLSI Design |
| Course Type: | Undergraduate/Graduate cross listing |
| Credits: | 3 credits |
| Duration: | Fall Quarter |

## Audience

This course is intended for **senior-level ECE undergraduate students** and **graduate students**. Workload for graduate and undergraduate students will be different and two parties will be evaluated independently.

## Prerequisites

Knowledge of digital logic design (**ECE 200**) and introductory electronics (**ECE-L 301-302**) is required. Previous exposure to transistors and semiconductor devices would be useful but not required. These introductory topics will be discussed in early stages of the course to provide necessary technical background to all students from EE and CE.

## Course Description

This is an introductory course in the field of *Very Large Scale Integration (VLSI) circuit and systems design*. Systematic understanding, design and analysis of VLSI integrated circuits will be covered. This course will focus exclusively on digital CMOS VLSI circuit and systems design, although some issues in mixed-signal mode will also be addressed.

The course will begin with a review of CMOS transistor operation and semiconductor manufacturing process. Logic design with CMOS transistors and circuit families will be described. Specifically, layout, design rules, and circuit simulation will be addressed towards the coverage of custom VLSI design principles.

Course objectives include:

- To learn the basic concepts of modern VLSI circuit design by studying logic design, physical structure and fabrication of semiconductor devices and how they are combined to build systems for efficient data processing,
- To learn the interface of logic and electronics through analyzing electrical and design characteristics of transistors and gates for high-performance integrated circuits,
- To understand the role of computer-aided design (CAD) tools in automating the design flow and providing improved productivity in VLSI systems design,
- To understand the relationship between semiconductor technology, transistors and architecture, addressing all levels of hierarchy in VLSI system design flow.

## Course Structure

| | |
|---|---|
| Laboratory: | Once a week for 1 hour, six (6) assignments |
| Exam(s): | One (1) final examination. |
| Homework(s): | Two (2) homeworks will be assigned. |
| Project(s): | *None* |

This is a senior level undergraduate level/graduate level class and the evaluation criteria is established accordingly. The evaluation process will encompass the monitoring of not the quality of individual work but also participation in group projects and lectures. The final grade will be calculated as follows:

| | | |
|---|---|---|
| Final | → | 30% |
| Homework(s) | → | 20% |
| Lab assignment(s) | → | 50% |
| *Total* | | *100%* |

Note that this course is cross-listed as a graduate level course. Graduate and undergraduate course work will be *different* and students will be evaluated *independently*. Graduate students will have more questions on the homeworks and examinations.

## Textbook

Following is a list of suggested textbooks for this course, starting with the *required* textbook by J. M. Rabaey, A. Chandrakasan and B. Nikolic. The additional textbooks 1 through 3 provide much additional information and can be quite useful.

**Required Textbook:** J. M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits*, Prentice Hall, $2^{nd}$ edition, 2003, ISBN:0130909963.

**Additional Reading:**
1. N. H. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective,* Addison-Wesley, $2^{nd}$ ed., 2004.
2. John P. Uyemura, *Introduction to VLSI Circuits and Systems: A Design Perspective,* Prentice-Hall, Inc., 2002.
3. S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits Analysis & Design,* McGraw-Hill Inc., 2002.

## Laboratory

Weekly design and simulation assignments using Cadence CAD tools. Specifically, Cadence Virtuoso tool for layout, Analog Artist using simulators Spice and Spectre for simulation and Diva/Accura for DRC will be used.

Weekly assignments will include:

- CMOS Inverter
- CMOS NAND and NOR gates
- XOR and MUX gates
- Learning about data paths: A simple sequential circuit (i.e. 2-bit adder with storage)

## Tentative Schedule

| Week | Lecture | Chapter | Lab |
|---|---|---|---|
| 1 | Introduction to VLSI Systems | 1 | |
| 2 | CMOS Fabrication | 2 | |
| 3 | The Devices: NMOS and PMOS | 3 | CMOS inverter design |
| 4 | The Wire | 4 | CMOS NAND and NOR |
| 5 | Static CMOS Inverter: Speed, Area, Scaling | 5 | Inverter Chain |
| 6 | Static CMOS Inverter and Layout Techniques | 5 | HW #1 |
| 7 | CMOS Design Techniques | 6 | CMOS XOR and MUX |
| 8 | Logical Effort | 6 | |
| 9 | Static CMOS | 6.2 | 2-bit Adder |
| 10 | Dynamic CMOS | 6.3 | HW #2 |
| 11 | Sequential Logic 1: Registers | 7 | D Latch and DFF |
| 12 | Sequential Logic 2: Clock, Timing | 7 | |
| | **Final Examination** (Date TBA) | | |

ECE-C 490/690 ST: ASIC Design I — Syllabus

Baris Taskin
Office: Bossone 413F

Lecture: Mon 10:00-11:50am
Lab: Wed 10:00am-11:50am

## Course Information

| | |
|---|---|
| Course Type: | Undergraduate–senior, cross-listed as a graduate course |
| Credits: | 3 credits |
| Duration: | Winter Quarter 2009–2010 AY |
| Meeting Times: | Lectures: Once a week for 1h 50 minutes in Bossone 605 |
| | Laboratory: Once a week for 1 hour (1h:50m is reserved) in Bossone 605 |
| Teaching Assistant: | Mr. Jianchao Lu (jl597@drexel.edu), Bossone 324 |
| Succession: | ECE-C 490/690 ASIC Design II |

## Prerequisites

Knowledge of digital logic design (**ECE 200**) and computer organization & architecture (**ECEC 3XX**) is required.

## Course Description

This is a course in the field of *Very Large Scale Integration (VLSI) circuit and systems design*. Design and analysis of VLSI integrated circuits will be covered from a system design perspective. This course will focus exclusively on digital CMOS Application Specific Integrated Circuit (ASIC) systems design and automation. The ASIC physical design flow, including logic synthesis, floorplanning, placement, clock tree synthesis and routing will be presented. These back-end physical design flow steps will also be covered through hands-on practice using industrial VLSI CAD tools.

Course objectives include:

- To learn the advanced concepts of modern VLSI circuit and system design, including differences between ASICs and FPGAs, standard cells, cell libraries, IPs etc.
- To have experience with a logic synthesis tool for mapping RTL onto a cell library,
- To understand the back-end physical design flow, including floorplanning, placement, CTS and routing,
- To get accustomed to VLSI CAD tools and their usability,
- To understand the role of computer-aided design (CAD) tools in automating the design flow and providing improved productivity in VLSI systems design,

Course topics include:

1. Implementation Strategies for Digital ICs
2. Logic Synthesis
3. Floorplacement and P/G routing
4. Placement
5. Clock tree synthesis
6. Routing
7. Multi-corner/multi-mode analysis
8. IC Interconnects

## Course Structure

Laboratory: Once a week for 1 hour, multiple lab assignments
Exam(s): One (1) take-home midterm and one (1) final examination
Project(s): *None*

This is a senior level undergraduate level/graduate level class and the evaluation criteria is established accordingly. The evaluation process will encompass the monitoring of not only the quality of individual work but also participation in group projects and lectures. The final grade will be calculated as follows:

| | | |
|---|---|---|
| Final | → | 30% |
| Midterm | → | 25% |
| Lab assignment(s) | → | 40% |
| Participation | → | 5% |
| *Total* | | *100%* |

Note that this course is cross-listed as a graduate level course. Graduate and undergraduate course work will be *different* and students will be evaluated *independently*. Graduate students will have more or different questions on the homeworks and examinations.

## Textbook

Following is a list of suggested textbooks for this course, starting with the *required* textbook by J. M. Rabaey, A. Chandrakasan and B. Nikolic. The additional textbooks 1 through 5 provide much additional information and can be quite useful.

**Required Textbook:** J. M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits*, Prentice Hall, 2003, ISBN:0130909963.

**Additional Reading:**
1. John P. Uyemura, *Introduction to VLSI Circuits and Systems: A Design Perspective* Prentice-Hall, Inc., 2002.
2. N. H. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective,* Addison-Wesley, 2nd ed., 2004.
3. S.M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits Analysis & Design,* McGraw-Hill Inc., 2002.
4. H. Bhatnagar, *Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and PrimeTime*, 2nd edition, 2001
5. P. Kurup and T. Abbasi, *Logic Synthesis using Synopsys*, 2nd edition, 1997

## Laboratory

Weekly design and simulation assignments using `Synopsys` CAD tools. Specifically, Synopsys tools will be used for logic synthesis, placement, routing and timing verification. HSPICE simulator will be used when necessary.

Weekly assignments will include synthesis, placement, routing and verification examples/tutorials using various tools. These tutorials will have existing HDL inputs and step-by-step instructions to learn the tools, which will lay the groundwork for a project implementation next quarter.

## Tentative Schedule

| Week | Lecture | Lab |
|---|---|---|
| 1 | Introduction to ASIC design | |
| 2 | FPGA and ASIC design | Logic Synthesis setup |
| 3 | No class (MLK day) | Logic Synthesis lab + $1^{st}$ Assignment |
| 4 | Introduction to Physical Design | Intro physical design lab |
| 5 | Floorplanning | Floorplanning lab |
| 6 | Placement | Placement lab, Midterm |
| 7 | No class (President's Day) | Midterm discussion |
| 8 | Routing | Routing lab |
| 9 | Multi-mode, Multi-corner Analysis | $2^{nd}$ Assignment |
| 10 | Coping with Interconnect | |

ECE-C 490/690 ST: ASIC Design II — Syllabus

Baris Taskin
Office: Bossone 413F

Lecture: Mon 10:00-11:50am
Lab: Wed 10:00am-11:50am

## Course Information

| | |
|---|---|
| Course Title: | ST: ASIC Design II |
| Course Type: | Undergraduate – senior, cross-listed as a graduate course |
| Credits: | 3 credits |
| Duration: | Spring Quarter |
| Meeting Times: | Lectures: Once a week for 1:50 hour meetings |
| | Laboratory: Once a week for 1 hour (1h:50m reserved) |

## Prerequisites

Prerequisite for this course is **ECE-C 472 VLSI Design and Automation**. Knowledge of a Hardware Description Language (HDL) such as `VHDL` or `Verilog HDL` and *Unix* operating system is useful.

## Course Description

This is a project-oriented course in the field of *Very Large Scale Integration (VLSI) circuit and systems design*. Design and analysis of Application Specific Integrated Circuits (ASICs) will be covered from a circuits and systems design perspective. To this end, system timing principles and verification after ASIC back-end will be presented. Also, efficient ASIC implementations of arithmetic building blocks and memory architectures will be discussed. A quarter-long, keystone project will be assigned to students working in teams. Team-work, task assignment and team communication will be mediated in an industry setting, stimulating a realistic design environment. Design tasks will cover the back-end IC design flow range, from RTL description to timing and power verification. Successful designs can be sent to MOSIS for fabrication.

Course objectives include:

- To understand the challenges of ASIC timing verification in nanometer regimes, particularly due to variations,
- To get familiar with arithmetic building blocks of VLSI circuits and their performance characterizations,
- To get familiar with memory building blocks and their performance characterizations,
- To get accustomed to VLSI CAD tools and their usability,
- To perform first-hand ASIC system design from RTL description to tape-out,
- The ability to work in teams on a high complexity engineering project.

Course topics include:

1. Timing Issues in Digital Circuits
2. Design Verification
3. Designing Arithmetic Building Blocks
4. Designing Memory and Array Structures
5. Integrated Circuit Tape-out Process

## Course Structure

Laboratory: Once a week for 1 hour
Homework(s): One (1) homework
Exam(s): One (1) midterm
Project(s): One (1) keystone project

This is a senior level undergraduate/graduate level class and the evaluation criteria is established accordingly. The evaluation process will encompass the monitoring of not the quality of individual work but also participation in group projects and lectures. The final grade will be calculated as follows:

| | | |
|---|---|---|
| Project | → | 50% |
| Homework | → | 10% |
| Midterm | → | 30% |
| Participation | → | 10% |
| *Total* | | *100%* |

Note that this course is cross-listed as a graduate level course. Graduate and undergraduate course work will be *different* and students will be evaluated *independently*. Graduate students will have more or different questions on the homeworks and examinations.

## Textbook

Following is a list of suggested textbooks for this course, starting with the *required* textbook by J. M. Rabaey, A. Chandrakasan and B. Nikolic. The additional textbooks 1 through 3 provide much additional information and can be quite useful. **Additional reading materials (*e.g.* about the project) will be provided by the instructor.** If you are planning to get into this field seriously, you may also want to consider periodical publications, such as additional reading reference #4.

**Required Textbook:** J. M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits*, Prentice Hall, 2003, ISBN:0130909963.

**Additional Reading:**
1. John P. Uyemura, *Introduction to VLSI Circuits and Systems: A Design Perspective* Prentice-Hall, Inc., 2002.
2. N. H. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective,* Addison-Wesley, 2nd ed., 2004.
3. S.M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits Analysis & Design,* McGraw-Hill Inc., 2002.
4. IEEE Transactions on VLSI Systems.
5. IEEE Transactions on Computer-Aided Design.
6. IEEE Transactions on Circuits and Systems, Part II-Systems.
7. IEEE Transactions on Computers.

## Laboratory

A quarter-long, keystone design project will be assigned. Students will be separated into design groups or hierarchical design teams. Laboratory sessions will be used to synchronize design teams, similar to weekly progress meetings in an industrial setting. Interface specifications and issues will be addressed. Progress reports and presentations will be performed.

Synopsys CAD tools will be used to complete the physical design of a high-complexity RTL design, such as a processor or a co-processor.

## Tentative Schedule

| Week # | Lecture | Lab |
|---|---|---|
| 1 | Project Description, Team and Task Assignments | Timing Lab 1 |
| 2 | Timing Issues in ASICs | Timing Lab 2 |
| 3 | Timing Issues in ASICs | Timing Lab 3 |
| 4 | Timing Verification using Static Timing Analysis | |
| 5 | Timing Verification using Static Timing Analysis | (Project Synthesis + Physical Design) |
| 6 | Arithmetic Circuits I | Midterm |
| 7 | Arithmetic Circuits II | (Project Verification + Optimization) |
| 8 | Progress/Proposal Presentations | |
| 9 | Memory Design I | Homework |
| 10 | Memory Design II | |
| 11 | Final Presentations | |
| 12 | No Final Exam | |

**ECE-C 671 EDA for VLSI Circuits I** **Syllabus**
Fall 2009 Drexel University
Prof. Baris Taskin ECE

## Course Information

| | |
|---|---|
| Course Title: | EDA for VLSI Circuits I |
| Credits: | 3 credits |
| Meeting Times: | 6:00 PM - 8:50 PM Friday |
| Room: | CAT 77 |
| Succession: | EDA for VLSI Circuits II in Winter (and DSM IC Circuits in Spring) |

## Instructor and TA Information

| | |
|---|---|
| Instructor: | Prof. Baris Taskin |
| Office: | Bossone 413F |
| Office Phone: | 215.895.5972 |
| E-mail: | `taskin@coe.drexel.edu` |
| Office Hours: | By appointment only |
| Note: | I am accessible to discuss class-related issues at most times. |
| Teaching Assistant: | *None* |

## Course Structure

| | |
|---|---|
| Recitations: | *None* |
| Laboratory: | *None* |
| Exam(s): | One (1) final examination. |
| Homework(s): | Three (3) homeworks will be assigned. |
| Project(s): | Two (2) projects will be assigned. |
| Paper Review(s): | One (1) paper review will be assigned. |

## Textbook

There are no *required* textbooks for this course. There is a list of supplementary textbooks which might be used to supplement the lecture notes that will be provided for each class. I plan to deliver the class on slides, and a copy of lecture notes will be provided to you either in electronic format (check prior to class) or in hard copy (in class). The list of supplementary books is:

- *Synthesis and Optimization of Digital Circuits*, G. De Micheli, 1994, ISBN: 0-07-016333-2
- *Electronic Design Automation: Synthesis, Verification, and Test*, L-T. Wang, Y-W. Chang and K-T. Cheng, 2009, 0123743648
- *EDA for IC Implementation, Circuit Design, and Process Technology*, L. Lavagno, L. Scheffer and G. Martin, 2006, 0849379245
- *Logic Synthesis*, S. Devadas, A. Ghosh and K. Keutzer, 1994, ISBN: 0-07-016500-9
- *Algorithms for VLSI Physical Design Automation*, N. A. Sherwani, 1995, ISBN: 0-79-239592-1
- *VLSI Physical Design Automation*, S. M. Sait and H. Youssef, 1999, ISBN: 9-81-023883-5
- *Introduction to Algorithms*, $2^{nd}$ Edition, T. H. Cormen, C. E. Leiserson, R. L. Rivest and C. Stein, 2001, ISBN: 0-26203293-7

## Website

The course materials (lecture notes, homework assignments, etc.) will be made available through the WebCT website. Time permitting, the lecture notes will be placed on WebCT prior to class. The students should check the site by *noon of each lecture day* to get the lecture notes for that day. If the notes are not available by noon, hard copies will be distributed in the class.

For WebCT information, including features, access and usage details, see `http://www.drexel.edu/IRT/services/webct/index.html`.

## Course Content and Prerequisites

This course is the first of a two-course-sequence that focuses on the electronic design automation techniques in the physical design process of digital VLSI circuits. In this course, electronic design automation (EDA) techniques are discussed in theory and implementation in order to build CAD tools for VLSI design (instead of using/analyzing commercially available tools). In this first quarter of the course, algorithms, techniques and heuristics structuring the foundations of contemporary VLSI CAD tools are presented. Within this context, common data structures used for computer manipulation of circuit design data are analyzed. Optimization, satisfiability, graph theory and boolean algebra topics are presented. There are no prerequisites for this course, however, some background on digital VLSI circuit design, data structures and algorithms are required. Previous exposure to VLSI CAD tools is not necessary.

For reference, the emphasis in the second quarter of the course is on the fundamentals and design automation of the VLSI physical design flow. Various physical design flow steps including synthesis, technology mapping, partitioning, floorplanning, placement, routing and timing are analyzed in detail. Individual and team-based, small-to-medium scale programming projects are an integral part of the course. The prerequisite for this course is ECEC 671 (EDA for VLSI Circuits I) or the consent of the instructor.

A third course titled "Deep Sub-Micron IC Design" is offered in the spring term which focuses on the design challenges of digital VLSI integrated circuits in deep sub-micron (e.g. nanometer) manufacturing technologies. Topics of interest include electronic design automation (EDA) challenges due to increased design complexities and high-performance circuit design techniques such as low-power and variation-aware design. The impacts of nanometer scaling on CMOS technology are discussed extensivelywithin the contexts of interconnect planning, buffer insertion, signal integrity, power distribution, clock tree synthesis, low power circuit design and design for manufacturing (DFM). The course is structured on recent presentations, articles and tutorials from the industry and academia; advancing the discussions to state-of-the-art VLSI design techniques. The course material is delivered cohesively in a lecture format (not as a training session or a discussion from a list of papers). There are no prerequisites for this course, however, some background on digital VLSI circuit design is required.

There are *no prerequisite courses* for the EDA for VLSI Circuits I course. However, having some level of confidence in one or more of the following backgrounds would be beneficial:

- Basic CS data structures and algorithms,
- High-level computer programming languages (C/C++ preferred),
- Scripting languages (Tcl/Tk, Perl etc.), operating systems (Unix, GNU/Linux etc.),
- Basic digital design, combinational and sequential system design knowledge,
- Exposure to VLSI CAD tools and VLSI design process in general.

## Evaluation of Student Performance

This is a graduate level class and the evaluation criteria is established accordingly. The evaluation process will encompass the monitoring of not the quality of individual work but also participation in group projects and lectures. The final grade will be calculated as follows:

| | | |
|---|---|---|
| Final | → | 30% |
| Project(s) | → | 25% |
| Homework(s) | → | 30% |
| Paper Review | → | 15% |
| Participation | → | 5% |
| *Total* | | *105%* |

Note that the percentages above add up to *105%* for improved flexibility. The flexibility is intended to allow the graduate students to adopt their own schedules (instead of having to complete class work during busy paper deadline weeks, etc.) and still be able to get a perfect grade.

**Final:** The final examination will be conducted on the date and time as announced by the university (typically the same day/time of the course during the final's week). The final examination will cover the topics discussed in the class. No exceptions will be made for the adjustment of final examination date and time, so plan your winter travels accordingly.
**Project(s):** Two (2) projects will be assigned throughout the course. Both projects will aim to help canalize the information gathered in the course to practice. The first project will be an introductory programming project that affects 5% of the total grade. The second project will be a more complex project that involves a selected tool development problem, and will affect 20% of the total grade.
**Homework(s):** Three (3) homeworks will be assigned at regular intervals in order to observe the level of progress in the class. The allocation of grade percentages to the homeworks will be announced on homeworks. The students will be given *at least one calendar week* for each homework assignment. Collaborations on homeworks are *allowed*, unless specifically stated. Under any circumstances, *each student should submit their individual work*. When $n$ students submit the same solutions (exact copy), each one of the $n$ students will receive $1/n$ of the earned grade. In certain instances (for larger homeworks), only a fraction of the total assigned problems will be graded. The students will not know in advance which questions will be graded. Late homeworks will receive an automatic 10% reduction of the total earned grade per time unit (decided by the instructor) passed, and no late homeworks will be accepted after the solutions are announced.
**Paper Review:** One (1) technical paper (proceedings or transaction) will be assigned for review. The students will be asked to briefly summarize and comment on the contributions of the paper. The deliverables of this review process will be a short four page report paper. The goal is to have the students assimilate the information gathered in class and have them reflect this information on work that has been published in the field.
**Participation:** Participation grades will be granted on the discretion of the instructor. Participation reflects the overall engagement of the student to the course, through participation in and outside the class times.

## Academic Integrity

All students must agree to the standard academic integrity code as set forth by Drexel University. In order to review the code, see `http://www.drexel.edu/cchc/studentlife/Judicial/code/acadintegrity.html`.

## Disability

Students with disabilities (including learning disabilities) are encouraged to contact the instructor in a timely manner in order to provide necessary needs. For a list of services provided by Drexel University, see `http://www.drexel.edu/edt/disability/`.

## Disclaimer

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## Tentative Schedule

| Week # | Topic | Assignment |
|---|---|---|
| 1 | Introduction to Course | |
| 2 | Advanced Boolean Algebra | Project #1, Homework #1 |
| 3 | Binary Decision Diagrams (BDDs) | |
| 4 | Binary Decision Diagrams (BDDs) | Homework #2 |
| 5 | Satisfiability (SAT) Solvers | |
| 6 | Formal Verification | |
| 7 | 2-Level Logic Synthesis | Paper Review #1 |
| 8 | Multi-Level Logic Synthesis | Project #2 |
| 9 | Multi-Level Logic Synthesis | Homework #3 |
| 10 | *Thanksgiving* | |
| 11 | Multi-Level Logic Synthesis | |
| 12 | **Final Examination** (Date TBA) | |

**ECE-C 672 EDA for VLSI Circuits II** **Syllabus**
Department of Electrical and Computer Engineering Week 1
Drexel University 8 January 2010

## Course Information

| | |
|---|---|
| Course Title: | EDA for VLSI Circuits II |
| Course Type: | Graduate |
| Credits: | 3 credits |
| Duration: | Winter Quarter 2009-2010 AY |
| Meeting Times: | 6:00 PM - 8:50 PM Friday |
| Room: | Lebow 133 |

## Instructor and TA Information

| | |
|---|---|
| Instructor: | Prof. Baris Taskin |
| Office: | Bossone 411F |
| Office Phone: | 215.895.5972 |
| E-mail: | `taskin@coe.drexel.edu` |
| Office Hours: | By appointment only |
| Teaching Assistant: | *None* |

## Course Structure

| | |
|---|---|
| Recitations: | *None* |
| Laboratory: | *None* |
| Exam(s): | One (1) final examination will be given. |
| Homework(s): | One (1) homework will be assigned. |
| Project(s): | One (1) project will be assigned. |
| Paper Review(s): | Two (2) paper reviews will be assigned. |

## Textbook

There are no *required* textbooks for this course. There is a list of supplementary textbooks which might be used to supplement the lecture notes that will be provided for each class. I deliver the class on slides, and a copy of lecture notes will be provided to you either in electronic format (check prior to class) or in hard copy (in class). The list of supplementary books, in specific order, is:

- *Electronic Design Automation: Synthesis, Verification, and Test*, L-T. Wang, Y-W. Chang and K-T. Cheng, 2009, 0123743648
- *EDA for IC Implementation, Circuit Design, and Process Technology*, L. Lavagno, L. Scheffer and G. Martin, 2006, 0849379245
- *Algorithms for VLSI Physical Design Automation*, N. A. Sherwani, 1995, ISBN: 0-79-239592-1
- *VLSI Physical Design Automation*, S. M. Sait and H. Youssef, 1999, ISBN: 9-81-023883-5
- *Introduction to Algorithms*, $2^{nd}$ Edition, T. H. Cormen, C. E. Leiserson, R. L. Rivest and C. Stein, 2001, ISBN: 0-26203293-7

## Website

The course materials (lecture notes, homework assignments, etc.) will be made available through the WebCT website. Time permitting, the lecture notes will be placed on WebCT prior to class. The students should check the site by *noon of each lecture day* to get the lecture notes for that day. If the notes are not available by noon, hard copies will be distributed in the class.

For WebCT information, including features, access and usage details, see `http://www.drexel.edu/IRT/services/webct/index.html`.

## Course Content and Prerequisites

This course is the second of a two-course-sequence that focuses on the electronic design automation techniques in the physical design process of digital VLSI circuits. In this course, electronic design automation (EDA) techniques are discussed in theory and implementation in order to build CAD tools for VLSI design (instead of using/analyzing commercially available tools). In this second quarter of the course, the emphasis is on the fundamentals and the design automation of the VLSI physical design flow. Various physical design flow steps including technology mapping, partitioning, floorplanning, placement, routing and timing are analyzed in detail. Individual and team-based, small-to-medium scale programming projects are an integral part of the course. *The prerequisite for this course is ECEC 690-502 (ST: EDA for VLSI Circuits I) or the consent of the instructor.*

For reference, emphasis in this first quarter of the course is on algorithms, techniques and heuristics structuring the foundations of contemporary VLSI CAD tools are presented. Also, a third course titled "Deep Sub-Micron IC Design" is offered in the spring term which focuses on the design challenges of digital VLSI integrated circuits in deep sub-micron (e.g. nanometer) manufacturing technologies. Topics of interest include electronic design automation (EDA) challenges due to increased design complexities and high-performance circuit design techniques such as low-power and variation-aware design. The impacts of nanometer scaling on CMOS technology are discussed extensivelywithin the contexts of interconnect planning, buffer insertion, signal integrity, power distribution, clock tree synthesis, low power circuit design and design for manufacturing (DFM). The course is structured on recent presentations, articles and tutorials from the industry and academia; advancing the discussions to state-of-the-art VLSI design techniques. The course material is delivered cohesively in a lecture format (not as a training session or a discussion from a list of papers). There are no prerequisites for this third course, however, some background on digital VLSI circuit design is required.

Similar to the first course of the sequence, some level of confidence in one or more of the following backgrounds would be beneficial:

- Basic CS data structures and algorithms,
- High-level computer programming languages (C/C++ preferred),
- Scripting languages (Tcl/Tk, Perl etc.), operating systems (Unix, GNU/Linux etc.),
- Basic digital design, combinational and sequential system design knowledge,
- Exposure to VLSI CAD tools and VLSI design process in general.

## Evaluation of Student Performance

This is a graduate level class and the evaluation criteria is established accordingly. The evaluation process will encompass the monitoring of not the quality of individual work but also participation in group projects and lectures. The final grade will be calculated as follows:

| | | |
|---|---|---|
| Final | → | 20% |
| Project(s) | → | 35% |
| Homework(s) | → | 15% |
| Paper Review(s) | → | 30% |
| Participation | → | 5% |
| *Total* | | *105%* |

Note that the percentages above add up to *105%* for improved flexibility. The flexibility is intended to allow the graduate students to adopt their own schedules (instead of having to complete class work during busy paper deadline weeks, etc.) and still be able to get a full grade.

**Final:** The final examination will be conducted on the date and time as announced by the university. The final examination will cover all the topics discussed in the class starting from the midterm until the last class. No exceptions will be made for the adjustment of final examination date and time.
**Project(s):** One (1) project will be assigned throughout the course. The project will aim to help canalize the information gathered in the course to practice. The project will be of medium complexity, with an option to participate in group work for a more significant product.
**Homework(s):** One (1) homework will be assigned in order to observe the level of progress in the class. The allocation of grade percentages to the homeworks will be announced at a later date. If such information is not announced, all homeworks will equally affect the total grade. The students will be given *at least one calendar week* for each homework assignment. Collaborations on homeworks are *allowed*, unless specifically stated. Under any circumstances, *each student should submit their individual work*. When $n$ students submit the same solutions (exact copy), each one of the $n$ students will receive $1/n$ of the earned grade. In certain instances (for larger homeworks), only a fraction of the total assigned problems will be graded. The students will not know in advance which questions will be graded. Late homeworks will receive an automatic 10% reduction of the total earned grade, and no late homeworks will be accepted after the solutions are announced.
**Paper Review(s):** Two (2) technical papers (proceedings or transaction) will be assigned for review. The students will be asked to briefly summarize and comment on the contributions of the paper. The deliverables of this review process will be a short report paper. The goal is to have the students assimilate the information gathered in class and have them reflect this information on work that has been published in the field.
**Participation:** Participation grades will be granted on the discretion of the instructor. Participation reflects the overall engagement of the student to the course, through participation in and outside the class times.

## Academic Integrity

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## Disability

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## Tentative Schedule

| Month | Date | Week # | Topic | Assignment |
|---|---|---|---|---|
| January | 8 | 1 | Review and Introduction | |
| January | 15 | 2 | Technology Mapping | Paper Review #1 |
| January | 22 | 3 | Static Timing Analysis (STA) | Paper Review #2 |
| January | 29 | 4 | Statistical Timing Analysis (SSTA) | Project |
| February | 5 | 5 | Electrical Timing | |
| February | 12 | 6 | Placement – Simulated Annealing | |
| February | 19 | 7 | Placement – Partitioning | |
| February | 26 | 8 | Placement – Direct | Homework #1 |
| March | 5 | 9 | Routing I | |
| March | 12 | 10 | Routing II | |
| March | 17–22 | 11 | **Final Examination** | |

**ECE-C 673 Deep Sub-Micron IC Design** **Syllabus**
Department of Electrical and Computer Engineering Week 1
Drexel University Winter 2010

## Course Information

| | |
|---|---|
| Course Title: | Deep Sub-Micron Integrated Circuit (DSM IC) Design |
| Course Type: | Graduate |
| CRN: | 32533 |
| Credits: | 3 credits |
| Duration: | Spring Quarter |
| Meeting Times: | Thursday 6:00-8:50pm |
| Room: | Curtis 455 |

## Instructor and TA Information

| | |
|---|---|
| Instructor: | Prof. Baris Taskin |
| Office: | Bossone 413F |
| Office Phone: | 215.895.5972 |
| E-mail: | `taskin@coe.drexel.edu` |
| Teaching Assistant: | *None* |

## Course Structure

| | |
|---|---|
| Recitations: | *None* |
| Laboratory: | *None* |
| Exam(s): | One (1) midterm exam will be assigned. |
| Homework(s): | *None* |
| Project(s): | One (1) project will be assigned. |
| Paper Review(s): | Two (2) paper reviews will be assigned. |

## Textbook

There are no *required* textbooks for this course. There is a list of supplementary textbooks which might be used to supplement the lecture notes that will be provided for each class. I plan to deliver the class on color foils (or slides), and a copy of lecture notes will be provided to you either in electronic format (check prior to class) or in hard copy (in class). The list of supplementary books, in specific order, is:

- *Synthesis and Optimization of Digital Circuits*, G. De Micheli, 1994, ISBN: 0-07-016333-2
- *Logic Synthesis*, S. Devadas, A. Ghosh and K. Keutzer, 1994, ISBN: 0-07-016500-9
- *Algorithms for VLSI Physical Design Automation*, N. A. Sherwani, 1995, ISBN: 0-79-239592-1
- *VLSI Physical Design Automation*, S. M. Sait and H. Youssef, 1999, ISBN: 9-81-023883-5
- *Introduction to Algorithms*, $2^{nd}$ Edition, T. H. Cormen, C. E. Leiserson, R. L. Rivest and C. Stein, 2001, ISBN: 0-26203293-7

## Website

The course materials (lecture notes, homework assignments, etc.) will be made available through the WebCT website. Time permitting, the lecture notes will be placed on WebCT prior to class. The students should check the site by *noon of each lecture day* to get the lecture notes for that day. If the notes are not available by noon, hard copies will be distributed in the class.

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## Course Content and Prerequisites

This course focuses on the design challenges of digital VLSI integrated circuits in deep sub-micron (e.g. nanometer) manufacturing technologies. Topics of interest include electronic design automation (EDA) challenges due to increased design complexities and high-performance circuit design techniques such as low-power and variation-aware design. The impacts of nanometer scaling on CMOS technology are discussed extensively within the contexts of interconnect planning, buffer insertion, signal integrity, power distribution, clock tree synthesis, low power circuit design and design for manufacturing (DFM). The course is structured on recent presentations, articles and tutorials from the industry and academia; advancing the discussions to state-of-the-art VLSI design techniques. The course material is delivered cohesively in a lecture format (not as a training session or a discussion from a list of papers). **There are no prerequisites for this course, however, some background on digital VLSI circuit design is required.**

## Evaluation of Student Performance

This is a graduate level class and the evaluation criteria is established accordingly. The evaluation process will encompass the monitoring of not the quality of individual work but also participation in group projects and lectures. The final grade will be calculated as follows:

| | | |
|---|---|---|
| Project(s) | → | 40% |
| Exam | → | 30% |
| Paper Review(s) | → | 30% |
| Participation | → | 5% |
| *Total* | | *105%* |

Note that the percentages above add up to *105%* for improved flexibility. The flexibility is intended to allow the graduate students to adopt their own schedules (instead of having to complete class work during busy paper deadline weeks, etc.) and still be able to get a perfect grade.

**Exam:** A take-home midterm examination will be conducted on the date and time as announced on the syllabus. The examination will cover all the topics discussed in the class. No exceptions will be made for the adjustment of examination date and time.

**Project(s):** One (1) project will be assigned throughout the course. The project will aim to help canalize the information gathered in the course to practice. The project will be of medium-to-high complexity, with an option to participate in group work for a more significant product.

**Paper Review(s):** Two (2) technical papers (proceedings or transaction) will be assigned for review. The students will be asked to briefly summarize and comment on the contributions of the paper. The deliverables of this review process will be a short report paper. The goal is to have the students assimilate the information gathered in class and have them reflect this information on work that has been published in the field.

**Participation:** Participation grades will be granted on the discretion of the instructor. Participation reflects the overall engagement of the student to the course, through participation in and outside the class times.

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## Tentative Schedule

| Week # | Topic | Assignment |
|---|---|---|
| 1 | Review and Introduction | |
| 2 | Nanoscale CMOS Design I | Paper Review #1 |
| 3 | Nanoscale CMOS Design II | Project |
| 4 | Interconnect Planning | |
| 5 | Clock Tree Synthesis | Paper Review #2 |
| 6 | Signal Integrity | |
| 7 | Low Power Design I | Exam #1 |
| 8 | Low Power Design II | |
| 9 | **Presentations** | |
| 10 | Design for Manufacturing (DFM) | |
| 11 | —Finals— | |

# 9 Selected Publications for Project 1 to Project 4

1. V. Honkote and B. Taskin
   "CROA: Design and Analysis of Custom Rotary Oscillatory Array"
   *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*
   Pre-print in 2010.
   (Project 1)

2. J. Lu, Y. Teng and B. Taskin
   "A Reconfigurable Clock Polarity Assignment Flow for Clock Gated Designs"
   *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*
   In review, 2010
   (Project 2)

3. B. Taskin, A. Chiu*[4], J. Salkind* and D. Venutolo*
   "A Shift-Register Based QCA Memory Architecture"
   *ACM Journal on Emerging Technologies and Computation (JETC)*
   Vol. 5, No. 1, Article 4, pp. 1–18, January 2009
   (Project 3)

4. A. More and B. Taskin
   "Simulation Based Study of On-chip Antennas for a Reconfigurable Hybrid 3D Wireless NoC"
   *Proceedings of the IEEE International SOC Conference (SOCC)*
   September 2010
   (Project 4)

[4]The symbol * denotes an undergraduate author.

# CROA: Design and Analysis of the Custom Rotary Oscillatory Array

Vinayak Honkote, *Student Member, IEEE*, and Baris Taskin, *Member, IEEE*

***Abstract*—Rotary clocking is a resonant clocking technology for clock network design and distribution in high performance digital VLSI circuits. Rotary clocking technology offers an attractive alternative to the conventional clocking with high frequency clock signal generation at a low power dissipation rate. Traditionally, rotary clocking has been implemented using a regular array (grid) topology called rotary oscillatory arrays (ROA). In this paper, a *custom* rotary oscillatory array (CROA) topology is proposed for the generation and distribution of rotary clocking. The issues related to timing closure are addressed and the simulation-based analysis of the custom rotary rings is presented. The CROA design methodology is tested on the IBM `R1-R5` benchmark circuits. Compared to the traditional ROA, custom ROA results in 39.25% of tapping wirelength savings. The parasitic effects due to the customization of the topology—computed with partial element equivalent circuit (PEEC) analysis—are incorporated and the CROA topologies are simulated in SPICE. The simulation results show that, with additional parasitics due to the topological factors, the resultant clock frequency is observed to be 8.79% slower (assuming the tapping wirelength remains the same) than the expected frequency of operation without considering the topological factors.**

***Index Terms*—Partial element equivalent circuits, resonant clocking, traveling-wave oscillator, simulation.**

## I. Introduction

High frequency requirements and low power budgets of the DSM circuits cause the task of clock signal distribution to be quite challenging. In high performance applications, up to 40% of the total power dissipation is attributed to the clock distribution network [1]. The prevailing methodology to generate high-frequency clock signals is to use on-chip frequency multiplication with a phase-locked loop (PLL). The on-chip PLL components occupy significant chip area and clock distribution leads to problems with signal reflections, capacitive loading and power dissipation that effectively limit the maximum operating frequency. These trends point to a need for novel clocking methodologies, which can achieve high frequency with timing closure and low power dissipation.

To this end, adiabatic switching [2] offers an appealing solution by circulating the used energy back in the circuit. Resonant clocking technologies, which work on adiabatic switching principles, can generate very high frequency clock signals at a very low power dissipation rate. Furthermore, the resonant clocking technologies [3]–[10] eliminate the necessity to use a complicated on-chip PLL component. Resonant clocking is categorized into the following four main types, based on the resonating components and the generated clock signal pattern:

1) coupled LC oscillator [3];
2) standing wave oscillator [4], [5];
3) distributed oscillator [6];
4) rotary traveling wave oscillator [7].

Out of these technologies, the resonant *rotary* traveling wave oscillator technology provides constant magnitude, varying phase clock signals. The rotary clocking oscillators rely on the wave traveling principle on the transmission line wires to generate high frequency clock signals. These oscillators store the energy in the inductors during the discharging stage so that the stored energy can be recirculated during the charging stage-thereby minimizing the dynamic power consumption. A rotary traveling wave at 18 GHz frequency is implemented in [11], and up to 70% power savings are reported in [8].

A number of studies have been performed on the rotary clocking technology with regards to the physical design flow and design automation [8], [12]–[14]. In all of the previous research, the focus is on devising a design automation scheme for rotary clocking technology by placing the synchronous components with respect to a grid of *preplaced regular square* rings of the ROA topology. In this paper, a custom rotary oscillatory array (CROA) topology is proposed for rotary clocking. The novel CROA topology is proposed on the following premises:

1) rotary rings are permitted to have non-regular, custom shapes;
2) rotary rings are not fixed at the geographical center but are drawn to cover the high register density areas, in order to reduce the tapping wirelength;
3) synchronous circuit is built as a non-zero skew system in order to be synchronized by the multi-phase ring.

The design of the custom routes for the differential transmission lines in the CROA topology requires the analysis of parasitics due to the dependance of the oscillation frequency on the parasitics. To this end:

1) a detailed parasitic analysis on the rotary ring topologies incorporating the impacts of custom topologies is presented using PEEC analysis;
2) an improved SPICE simulation model is proposed for the CROA topology where the parasitics due to the topological factors are incorporated for increased accuracy in simulation.

The rest of this paper is organized as follows. In Section II, the rotary clocking technology is reviewed. In Section III,

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Digital Object Identifier 10.1109/TVLSI.2010.2057265

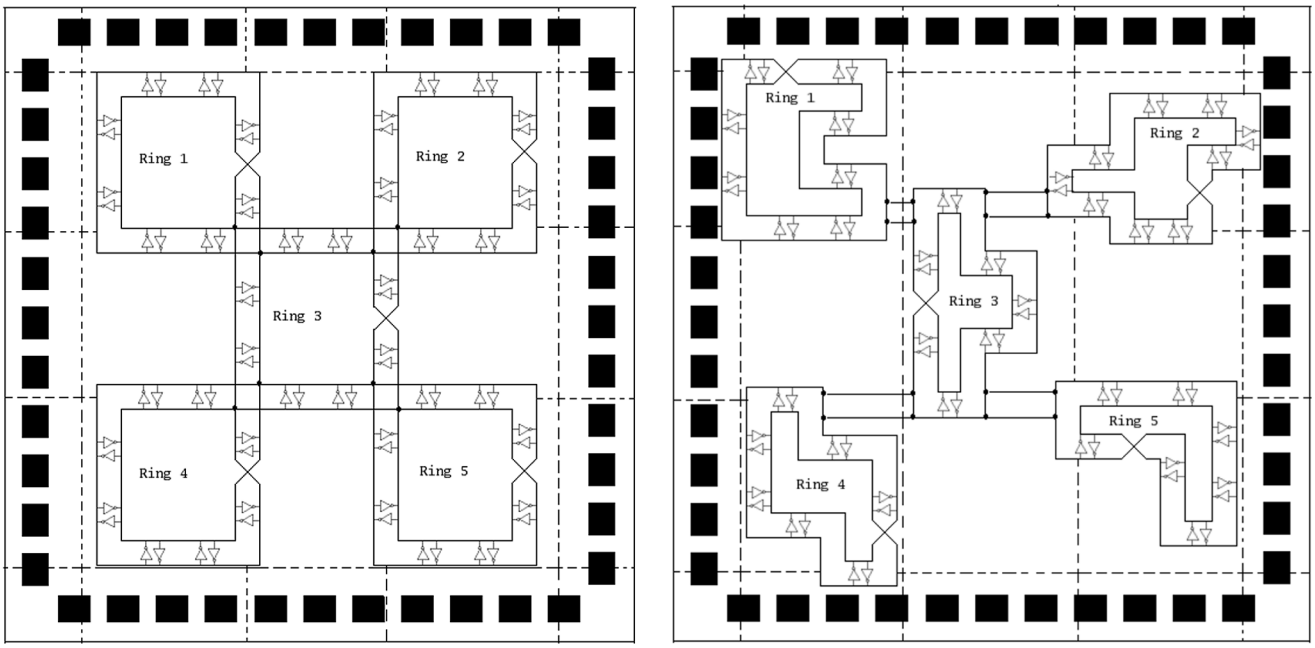


Fig. 1. Two different array topologies for the design and distribution of the rotary clocking technology. (a) Standard rotary clock array (ROA). (b) Custom rotary clock array (CROA).

the proposed design methodology for CROA is explained. In Section IV, a detailed parasitic analysis for the custom rotary ring operation is presented. In Section V, the experimental results for the CROA design methodology tested on the IBM `R1-R5` circuits are presented. The interpretation of the results is presented in Section VI. In Section VII, a conclusion of the work is presented.

## II. Rotary Clocking Technology

Rotary clocking technology is traditionally implemented with a regular array (grid) topology, as shown in Fig. 1(a). ROAs are generated on the cross-connected transmission lines formed by regular integrated circuit (IC) interconnects. An oscillation can start spontaneously upon any noise event or stimulated by a start up circuit for controlled operation [7]. When the oscillation is established, a square wave signal can travel along the ring without termination. Oscillations on the rings are locked in phase on the ROA, minimizing the effects of jitter. The anti-parallel inverter pairs between the interconnects [as shown in Fig. 1(a)] serve to sustain the signal propagation on the wires and aid in the charge recovery process. Such rotary-oscillator-generated-square-waves present low jitter, controllable skew and phase properties.

For the rotary clocking implementation, the phase and the frequency information are critical. For the phase information, an arbitrary point on the ring is identified as the reference point with a clock signal delay $t = 0$ and phase $\theta = 0°$. The clock signal travels along the ring and reaches back the reference point with a phase $\theta = 360°$. A phase of 360° is defined for notational convenience and is associated with a clock delay equivalent to the clock period. For example, 90° of phase corresponds to $T/4$ units of delay, where $T$ is the clock period. At any point on the ring, the clock signal delay $t$ and the clock signal phase $\theta$ are correlated through

$$\frac{\theta}{360} = \frac{t}{T}. \tag{1}$$

For the frequency information of the rotary clock signal, the capacitive and inductive properties of the rotary rings need to be identified. A simplification is offered in [7] in modeling the rotary ring as an LC circuit where the total inductance and capacitance of the rotary ring are lumped into $L_T$ and $C_T$, respectively. Assuming a uniform distribution of inductance and capacitance along the ring for simplicity [7], the phase velocity $v_p$ of the wave is calculated using the per-unit-length differential inductance $L_l$ and capacitance $C_l$ as

$$v_p = \frac{1}{\sqrt{L_l C_l}} \tag{2}$$

where $L_l$ and $C_l$ are computed from the lumped *LC* model of the entire rotary ring. Since the traveling wave requires two rotations to complete a clock period, the oscillation frequency is approximated as

$$f_{\text{osc}} \approx \frac{v_p}{2l} = \frac{1}{2\sqrt{L_T C_T}} \tag{3}$$

where $l$ is the length of the rotary ring [7]. Note that, a distributed *LC* model can be used to compute the local phase velocity for improved accuracy. In this work, the simplification of the lumped *LC* model and the uniform phase distribution are adopted for the ease of presentation. Extension of the current model to the distributed *LC* model is trivial.

In (3), the total inductance $L_T$ is estimated as in [7]

$$L_T \approx \frac{P\mu_0}{\pi} \log\left[\left(\frac{\pi s}{w+t}\right) + 1\right] \tag{4}$$

where $P, s, w, t$, and $\mu_0$ are the perimeter of the ring, wire separation, wire width, wire thickness, and permeability in vacuum, respectively. The total capacitance $C_T$ is estimated by

$$C_T \approx \sum C_{\text{reg}} + \sum C_{\text{inv}} + \sum C_{\text{ring}} + \sum C_{\text{wire}} \quad (5)$$

where $C_{\text{reg}}$, $C_{\text{inv}}$, $C_{\text{ring}}$, and $C_{\text{wire}}$ are capacitances contributed by the registers, the inverters between the differential transmission lines, the ring transmission line interconnects and the register tapping wires, respectively. The capacitances $C_{\text{reg}}$ and $C_{\text{inv}}$ are defined based on the types and sizes of the register and inverter components, respectively. The ring capacitance $C_{\text{ring}}$ includes the self and coupling capacitances between the transmission line interconnects. The tapping wire capacitance $C_{\text{wire}}$ depends on the distance between the rotary ring and the registers (clock sinks). The wires used in rotary clocking technology are wide and thick enough such that the wire resistance is negligible.

The physical design flow and design automation methodologies for rotary clocking technology have been investigated in [8], [12]–[14]. In [12], a pioneering physical design flow with circuit partitioning and register placement is presented. In [13], an incremental placement and skew optimization algorithm is presented, where the register components are placed at near optimal locations with respect to a regular rotary ring. In [14], the design of rotary based circuits is proposed using retiming and padding concepts to satisfy the timing requirements of register components. In [8], regular rotary ring structures are analyzed in detail with the objective of power minimization. In all these previous works [8], [12]–[14], as well as the pioneering work in rotary clocking [7], the regular rotary ring is placed at the geographical center of the chip area using the ROA. In register synchronization with the ROA, the registers are either moved closer or away from the preplaced ring such that when connected to the tapping points on the ring, the register timing constraints are satisfied. Such design methodologies provide no flexibility in the clock network design and require incremental optimization at the placement and routing stages.

## III. Design of CROA

The CROA topology is implemented on an array-based scheme similar to the conventional ROA topology as shown in Fig. 1(b). The number of rings in the array is chosen so as to cover the whole chip area. Note that, if the array does not cover the whole chip are or the number of rings in the array is reduced, then the register tapping wirelength increases resulting in increased power dissipation and potential wire congestion. The perimeter $P_r$ is selected based on (3)–(5) to maintain a constant frequency $f_r$ on each ring. In Section III-A, the algorithm for the custom ring implementation is presented. In Section III-B, the synchronization aspects of the custom rings are discussed.

### A. Algorithm for the Custom Ring Implementation

The custom ring implementation is inspired from the popular maze router algorithm [15]. Based on the perimeter $P_r$ and the placement information for each synchronous component (e.g., clock sink), the circuit is partitioned into major square grids.

```
S(x,y) FindSource( minor grids, vector < x,y > ) {
        for (j = 1; j <minor grids; j++){
            b[phase][j] ← form b phase bins;
        }
        S(x,y) ← max_{∀ phase,j} {b[phase][j]};
    }
vector < Rings >FormRings(S(x,y), minor grids, perimeter p)
{
        create wavefronts starting from source S(x,y);
        form closed paths of length p by tracing the source S(x,y) back;
        vector < Rings >← consolidate all the rings with perimeter p;
    }
struct(WL_min, Ring_i) Wirelength(vector < Rings >, minor grids) {
        for (k = 1;k < vector < Rings >.size(); k++){
            determine tapping points;
            WL_k ← compute total tapping wirelength;
        }
        WL_min ← min_{∀ k}{WL_k};
        Ring_i ← Ring with the min tapping wirelength WL_min;
    }
int main (int argc, char* argv[]) {
    ...
        for (i = 1;i <major grids; i++){
            S(x,y) = FindSource(minor grids, vector < x,y >);
            vector < Rings > = FormRings(S(x,y), minor grids, perimeter
    p);
            WL_min = Wirelength(vector < Rings >, minor grids);
        }
    ...
    }
```

Fig. 2. Pseudo-code for the custom router, including an excerpt from the main function and the three functions FindSource, FormRings, and Wirelength.

The CROA topology is implemented on the major square grids, where each major grid holds one custom rotary ring. The objective of the original maze router algorithm is to find the shortest path from a source node to a target node on a gridded plane. A novel custom router algorithm is developed in order to find a closed path (ring) for the given path length on a gridded plane. The proposed custom router algorithm has similar mechanics and same complexity [$O(mn)$ for a grid with $m$ rows and $n$ columns] as the original maze router.

The well known, original maze router algorithm [15] comprises of three stages. The first stage, *wave propagation*, consists of expanding a wave from the source node to the target node. The second stage, *backtrace*, consists of tracing back a path from the target node to the source node. The third stage, *clean up*, consists of removing all the cells that are not a part of the path found in *backtrace* stage. In order to facilitate a maze router based implementation, each major grid is further divided into minor square grids. The granularity of the minor grid plane is determined based on the number of tapping points on the custom ring. The minimum number of minor grids is limited by the number of tapping points, such that each minor grid holds exactly one tapping point, permitting the application of a maze-router-like strategy. Higher number of minor grids can be used in order to increase the quality of the final result.

The proposed custom router algorithm comprises of three stages. The three stages of the algorithm, implemented as shown in the pseudo-code in Fig. 2, perform the following functions:

1) `FindSource`: Identifying the source grid;
2) `FormRings`: Generating all possible rings;

3) `Wirelength`: Computing the wirelengths to find the best possible custom ring.

In the `FindSource` stage, a source grid $S(x, y)$ is identified among the minor grids in each major grid. In the original maze router algorithm [15], the waves are grown from the source node towards the target node. To incorporate a similar style, a source cell is heuristically identified in the custom router. In each major grid (i.e., custom rotary ring), for the given register placement *vector* $\langle x, y\rangle$ and the phase information $b[\text{phase}][j]$, the minor grid with the most number of registers having the same phase requirement is selected as the source cell $S(x, y)$.

The `FormRings` stage of the proposed custom router algorithm is similar to the *wave propagation* stage of maze routing. Waves from the source grid $S(x, y)$ are propagated exhaustively over the entire minor grid structure in each major grid, until the source grid is traced again, thus forming a closed path. The entire solution space consisting of all possible custom rings for the perimeter $p$ is consolidated in *vector* $\langle Rings\rangle$.

The `Wirelength` stage of the custom router is similar to the *cleanup* stage of maze routing. In order to identify the "best" ring, first the registers are connected to all the possible rings in the solution space, at a fixed number of points marked as tapping points. Then, the total register tapping wirelengths for all the possible rings are computed. The best ring $\text{Ring}_i$ is defined as the ring that requires the minimum total register tapping wirelength $\text{WL}_{\min}$.

The three stages of the custom ring implementation algorithm are designed to provide the best possible clock phases to the synchronous components. The proposed CROA design methodology involves non-zero clock skew system design, where the required clock delay at each synchronous component can be different. The required clock phases are provided by "tapping" the synchronous components onto the ring depending on the phase of the clock signal around the ring and the tapping wire.

On the custom ring of the CROA topology, a fixed number of points are marked as potential tapping points. The definition of tapping points helps in simplifying the physical design in timing and load balancing during oscillation. These tapping locations have phases uniformly distributed between 0° and the clock period $T$. Consider a register $R_k$ at $(x_k, y_k)$ as shown in Fig. 3, which has a phase requirement of $\psi_k$. This register can be connected to any tapping point, marked P1–P12, on the rotary ring as shown in Fig. 3.

The primary objective in connecting a register to a tapping point is to minimize the skew mismatch for the register. The phase requirement of the register must be satisfied by choosing the best tapping point while considering the added phase (e.g., delay) of the tapping wire to the tapping point. The total phase $\Theta_i(x_k, y_k)$ at register $R_k$ placed at location $(x_k, y_k)$ from each tapping point $P_i$ on the rotary ring is computed as

$$\Theta_i(x_k, y_k) = \theta_i + \phi[l_i(x_k, y_k)] \tag{6}$$

where $\theta_i$ is the phase at the tapping point $P_i$ on the custom rotary ring and $\phi[l_i(x_k, y_k)]$ is the phase of the tapping wire of length $l_i(x_k, y_k)$ from the tapping point $P_i$ to the register $R_k$ as shown in Fig. 3. In accordance to (1), the phase $\phi[l_i(x_k, y_k)]$ of the tapping wire is given by

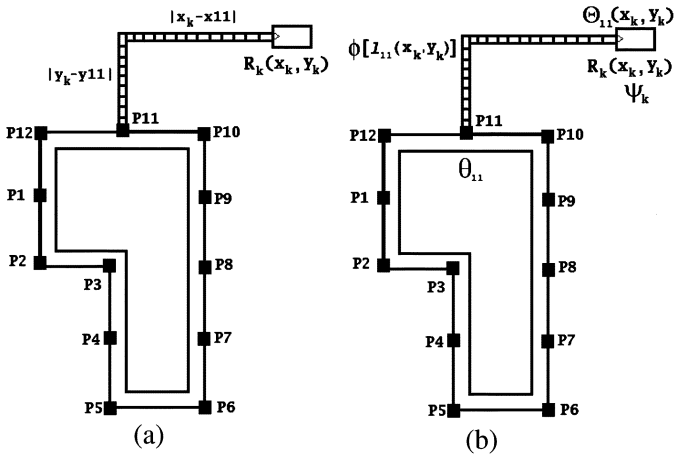


Fig. 3. "Tapping" the register $R_k$ on to the ring at the tapping point `P11`. (a) Wirelength computation. (b) Phase computation.

$$\phi[l_i(x_k, y_k)] = \left\{\frac{t[l_i(x_k, y_k)]}{T}\right\} 360^\circ \tag{7}$$

where $t[l_i(x_k, y_k)]$ is the delay of an interconnect of length $l_i$ and $T$ is the clock period. Note that, the delay function $t()$ can be of any desired accuracy for a tradeoff between the computation time and the synchronization accuracy. Using (6) and (7), the register $R_k$ is connected to the tapping point with the phase of $\theta_i$ such that $\Theta_i(x_k, y_k)$ is as close as possible to the desired phase $\psi_k$ at $R_k$. In Fig. 3, the register $R_k$ is connected to $P_{11}$. Thus, the phase at $R_k$ is $\Theta_{11}(x_k, y_k) = \theta_{11} + \phi[l_{11}(x_k, y_k)]$ such that, the phase requirement $\psi_k$ at $R_k$ is best provided by tapping on to the tapping location $P_{11}$, as opposed to any of the 11 other tapping locations

$$\min_{\forall i \in \{1,12\}} [\Theta_i(x_k, y_k) - \psi_k] = |\Theta_{11}(x_k, y_k) - \psi_k|. \tag{8}$$

This procedure is employed to connect all the registers to the best tapping locations on all possible custom rings in a given major grid. For all these rings in a major grid, the tapping wirelengths are computed. The ring that results in the minimum tapping wirelength is chosen as the best custom ring in the corresponding major grid.

### *B. Synchronization Between the Custom Rings in CROA*

Consider the CROA topology as shown in Fig. 1(b). For synchronization purposes, the rings are connected using short transmission lines as the additional design element, which form the dual-three-port network junctions. Consider the two custom rings connected together using three-port networks as shown in Fig. 4. In Fig. 4(a), the velocity mismatched pulses are shown. The on-time arriving pulse and the delayed pulse on the first three-port junction are as shown in Fig. 4(a). When the delayed pulse arrives, the delayed pulse combines with the earlier pulse. This new pulse is locked in phase and travels through the other ports synchronizing the phase of the two custom rings as shown in Fig. 4(b). Through this mechanism, the oscillating signals of both the rings are locked in phase, regardless of the direction of the delayed pulse.

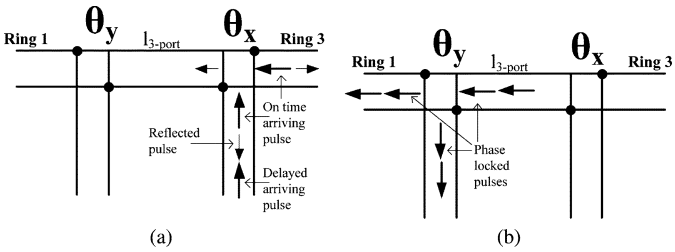


Fig. 4. Synchronization of custom rings in CROA using three-port network.

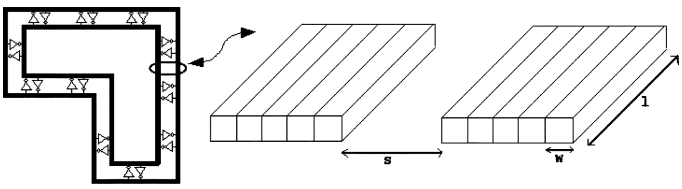


Fig. 5. Segmenting the transmission line for inductance computation.

## IV. Parasitic Analysis

The frequency of the rotary ring is estimated by (3), which depends on the circuit parasitics in (4) and (5). However, the high frequency effects and the impact of the interconnect geometries cannot be captured using (3). In the pioneering work on rotary clocking [7], the lumped *RLC* model is proposed for SPICE simulation. This model does not consider the high frequency effects and hence cannot be used for high frequency analysis. U-elements in SPICE are used to model the transmission line behavior of interconnects at high frequencies of resonant operation in [5]. As an alternative, the *partial element equivalent circuit* (PEEC) method is also used to capture the parasitic effects at high frequencies [16], [17]. As the PEEC analysis is based on the Maxwell's wave equations, it models the electromagnetic effects for an improved accuracy in analysis.

SPICE simulations including the PEEC models have been proposed for rotary clocking in [8]. In [8], the mutual inductance effects between the two transmission line elements are considered, however, the mutual inductance effects due to topological properties (such as corners and gap) are neglected. At high frequencies, parasitic effects due to the corners are significant and cannot be neglected. Especially in the CROA topology, the custom rings have a varying number of corners. Hence, the extraction of the parasitics with the additional corners is necessary in order to accurately analyze the oscillating frequency of the rotary clocking technology. A PEEC-based analysis is proposed for the parasitic extraction.

In order to perform the improved PEEC based analysis, the transmission line interconnects forming the rotary rings are partitioned into uniform segments similar to the procedure adopted in [8]. On these segments, constant current densities and charge densities are formed. Each of these segments is further divided into uniform filaments of length $l$ as shown in Fig. 5. Using the constant current and charge densities, the mutual inductance between the segments can be computed using the center filaments as explained in [18], [19]. The inductance contributed by the different segments of lengths $l$ and $a$ for the custom ring can be

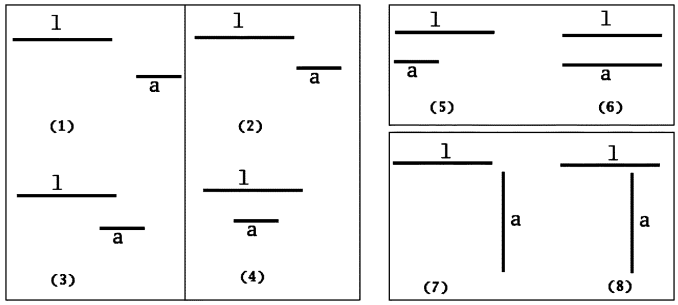


Fig. 6. Different cases in mutual inductance calculation.

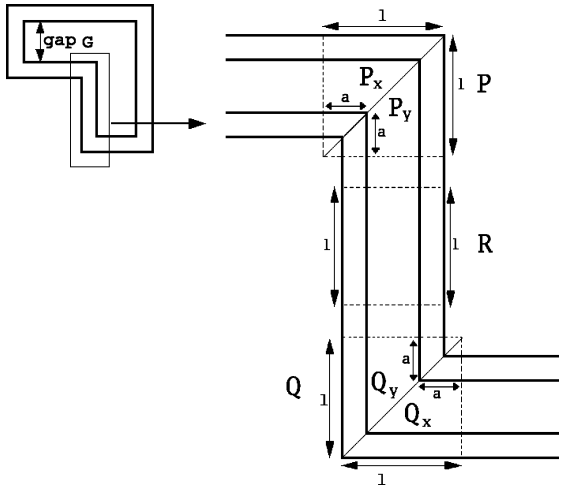


Fig. 7. Corners and gap in a custom ring.

summarized leading to eight (8) different cases for PEEC analysis as shown in Fig. 6. The PEEC analysis is performed on all the corners analytically using the formulas in [18], [19]. For any given custom ring topology, analytically computed models are synthesized to perform SPICE simulations.

The PEEC analysis results are presented in three stages in order to first establish the importance of mutual inductance analysis and then to demonstrate its overall impact. First, the mutual inductance between the components constituting a "corner" is analyzed. Second, the mutual inductance between the opposite edges of the custom topology called a "gap" is analyzed. Third, the components are merged to analyze the change in the mutual inductance for the entire custom ring with a varying number of corners.

### A. Corners

Consider a custom ring shown in Fig. 7. An enlarged version of a particular segment of a custom ring with two corners is shown. Each corner segment in a custom ring is similar to one of the corner segments marked as `P` or `Q`. Due to the cross-connected arrangement for rotary rings, each corner on the rotary ring has the outer transmission line and the inner transmission line as shown in the enlarged part of Fig. 7. The separation between the two transmission lines is $s$ and the width of each transmission line is $w$. The mutual inductance for each corner segment consists of two parts called the horizontal part ($x$ part) and the vertical part ($y$ part). For corner segments `P` and `Q`, the horizontal parts are marked as $\mathtt{P}_x$ and $\mathtt{Q}_x$, respectively, and the

vertical parts are marked as $\mathtt{P}_y$ and $\mathtt{Q}_y$, respectively. A corner segment of type P is of length $2l$, where as a corner segment of type Q is of length $2a$ on the outer transmission line.

Consider the case of the horizontal part $\mathtt{P}_x$ of the corner segment P. The outer transmission line is marked as $l$ and the inner transmission line is marked as $a$. The mutual inductance between the outer transmission line $l$ and the inner transmission line $a$ (by identifying the cases shown in Fig. 6) is computed using [18]

$$M = \left[\frac{1}{2}(L_{s+t} + L_{s-t}) - L_s\right] \cdot \left(\frac{s}{t}\right)^2 + (L_{s+t} - L_{s-t}) \cdot \left(\frac{s}{t}\right) + \frac{1}{2}(L_{s+t} + L_{s-t}) \quad (10)$$

where the subscripts to inductance L indicate the thickness of the segment, whose width is $w$ and length is $l$. The self inductances $L$ on the RHS of (10) are calculated using

$$\frac{L}{l} = \frac{\mu}{2\pi}\left[\ln\frac{2l}{0.2235 \cdot (w+t)} - 1\right] \quad (11)$$

where $s, t, l, w$ represent the separation, thickness, length, and width of the transmission line segments, respectively, and $\mu = 4\pi$ nH/cm is the permeability in free space. The vertical part $\mathtt{P}_y$ and the horizontal part $\mathtt{P}_x$ have identical mutual inductances, since the dimensions of the transmission lines, the separation and the width remain unchanged. Next, consider the case of horizontal part $\mathtt{Q}_x$ at corner Q. In this case, the lengths of the outer and inner transmission lines are $a$ and $l$, as opposed to $l$ and $a$ as in $\mathtt{P}_x$. In a similar manner, the mutual inductance between $l$ and $a$ is computed based on the cases shown in Fig. 6, using (10) and (11). The additional capacitance due to the corner is estimated using [20]

$$C_{\text{corner}} = 0.5 \times C_l \times w \quad (12)$$

where $C_l$ is the capacitance per unit length of the transmission line. The impact of corners on capacitance due to the increased wire width is included in the proposed simulation model. These improved simulation models are particularly important for the custom topology rings, where the number of corners can be high. However, the models should be used for the regular rotary rings as well, where the regular rings have the added capacitance of the four corners.

### B. Gap

The distance between the opposite edges in a rotary ring, marked on Fig. 7, is termed a "gap." In a custom ring, there are multiple edges, and every opposite edge pair contributes towards the mutual inductance. In order to investigate the level of this contribution, the mutual inductance between the opposite pairs (i.e., gap) is analyzed. The mutual inductance computation for the gap is similar to a case of two parallel segments with equal lengths [case (6)] as shown in Fig. 6. The major difference is that the separation between the transmission lines is the length of an edge of the custom ring as opposed to the separation s in Fig. 5. It is projected that due to the distance between the transmission lines, the mutual inductance contributed by the gap is controllable. Based on this projection (and the computation shown in Section V-B), a minimum gap $G$ is devised for a custom ring in CROA, either to eliminate the mutual inductance by keeping gap $G$ long enough or by analyzing for the existing mutual inductance due to the gap $G$. Note that, the improved simulation models with "gap" analysis can be applied for regular rings as well, however, the impact is minimal as "the gap $(P_r/4)$" is very large for regular rings.

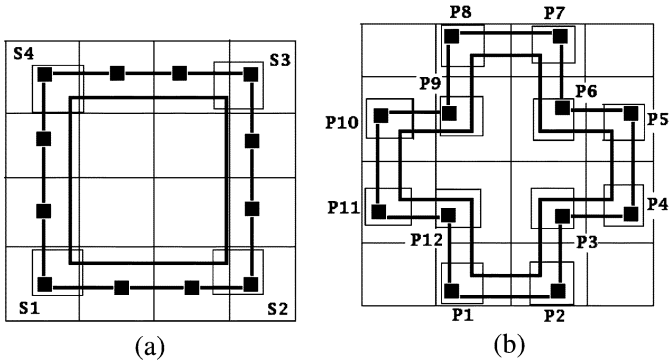


Fig. 8. Two possible custom ring topologies with $P_r = 12$ grids. (a) Minimum number of corners. (b) Maximum number of corners.

### C. Custom Ring Topologies of CROA

From a topology perspective, the parasitics of an arbitrary CROA ring depend on the gap dimensions, the number and the type of corners. In computation, the custom ring is partitioned into regular (straight) segments R, corner segments (of type P and Q) and gap segments (of type G), as shown in Fig. 7. The parasitics of each of the regular segment R, the corner segments P and Q, and the gap segment G are computed as described in Sections IV-A and IV-B, and summed over the entire length of the custom ring.

In order to simplify the parasitic analysis, the grid-based approach of the proposed CROA design methodology is leveraged. The minimum number of corners is always four in order to define a ring. Given the perimeter $P_r$ of a ring in terms of the minor grids, the maximum number of corners are identified as $P_r$ as corners are permitted once per grid. For instance, given a custom ring in a CROA partition with a perimeter $P_r$ corresponding to twelve (12) minor grids, the minimum and the maximum number of corners are 4 and 12, respectively. These cases are shown in Fig. 8. Any even number of corners between 4 and 12 is permitted for the custom ring implementation of the specification given above.

The total mutual inductance of custom rings with the minimum, maximum and any possible (an even number between minimum and maximum) number of corners are computed in experimentation. Furthermore, the frequencies for different CROA topologies are simulated with SPICE using the improved model with PEEC analysis.

## V. Experimental Results

The experimental results for the CROA design methodology described in Section III and the mutual inductance analysis

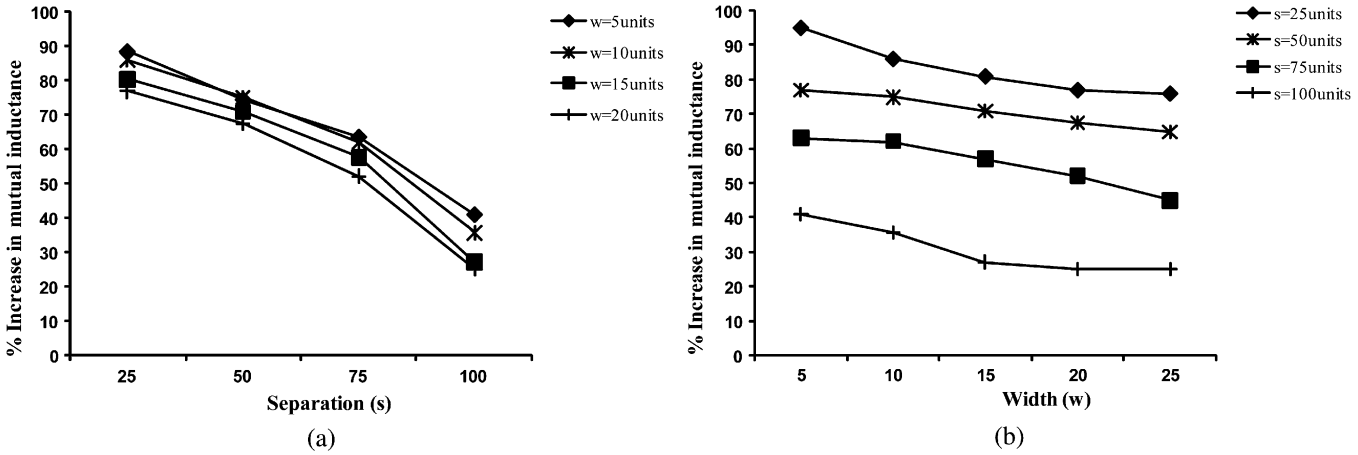


Fig. 9. Change in mutual inductance when corner segments P and Q are compared with a regular segment R.

TABLE I
TAPPING WIRELENGTH COMPARISON FOR CROA VERSUS ROA

| Benchmark | Grid size | ROA | CROA | Improvement |
|---|---|---|---|---|
| R1 | $5 \times 5$ | 2,773,150 | 1,567,220 | 43.49% |
| R2 | $6 \times 6$ | 6,552,330 | 4,059,290 | 38.05% |
| R3 | $7 \times 7$ | 8,827,920 | 5,308,910 | 39.86% |
| R4 | $9 \times 9$ | 19,962,400 | 12,281,800 | 38.58% |
| R5 | $10 \times 10$ | 33,035,200 | 21,054,800 | 36.27% |
| Average | — | — | — | 39.25% |

presented in Section IV are presented in Section V-A and Section V-B, respectively. The SPICE simulation results are presented in Section V-C.

### A. CROA Design Methodology

The proposed methodology for the CROA topology design, presented in Section III, is tested on the IBM R1–R5 benchmark circuits, which have a number of clock sinks ranging from 267 to 3101. The R1–R5 circuits include only the placement information for each synchronous component and not the phase information. The phase values—ranging from 0° to 360°—are randomly generated for the register sinks in the benchmark circuit files. The R1–R5 benchmark circuits use a generic unit of length. Thus, the same generic unit is used in this paper in order to represent the physical dimensions of wires and transmission lines.

Note that, the presented setup is for the experimentation on R1–R5 benchmark circuits only. In general, for the physical design and timing, data for any circuit can be used as an input to the proposed CROA design methodology. This includes non-zero skew circuits, where an SDF file is generated by running a clock skew scheduler on the design, which would provide required clock phases $\psi_k$ that vary significantly. A zero clock skew circuit, generated by a mainstream physical design flow would provide clock phases $\psi_k$ that are relatively similar to each other.

For each custom ring in the CROA topology, the perimeter $P_r$ is selected so as to maintain the constant frequency of oscillation $f_r$. The first-order delay model is used for delay computation purposes. The grid size of the ROA topology is determined based on the perimeter $P_r$ and placement information for each register. For example, the IBM benchmark circuit R1 is partitioned into $5 \times 5$ major ROA grids, considering the size of the circuit and the perimeter computed for a simulated frequency of $f_r = 4.7$ GHz. In order to facilitate the custom ring router, each partition is further divided into $12 \times 12$ minor grids. For the same frequency, benchmark circuit R5 is partitioned into $10 \times 10$ major ROA grids and each partition is further divided into a $12 \times 12$ minor grid structure.

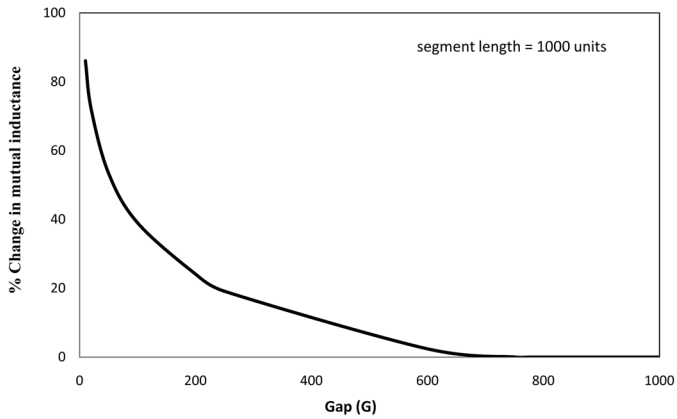


Fig. 10. Mutual inductance for varying "gap" with a segment of 1000 units.

The custom rings are drawn and the register tapping wirelengths are computed based on the algorithm presented in Section III. To compare the register tapping wirelengths obtained in CROA, regular rings are drawn at the geographical center of each partition to form the traditional ROA. The register tapping wirelength for each ring in ROA is computed. In Table I, the register tapping wirelengths for ROA and CROA are compared. With CROA, 39.25% of the tapping wirelength can be saved on average when compared to regular ROA. This wirelength saving is a direct result of the custom topology design to draw the rings closer to the high register density areas. The tapping wirelength improvement is relatively constant (36.27% to 43.49%) over different sizes of circuits.

### B. PEEC Analysis for Mutual Inductance

The mutual inductance is analyzed in three stages. First, the results for the "corner" analysis in Section IV-A are presented.

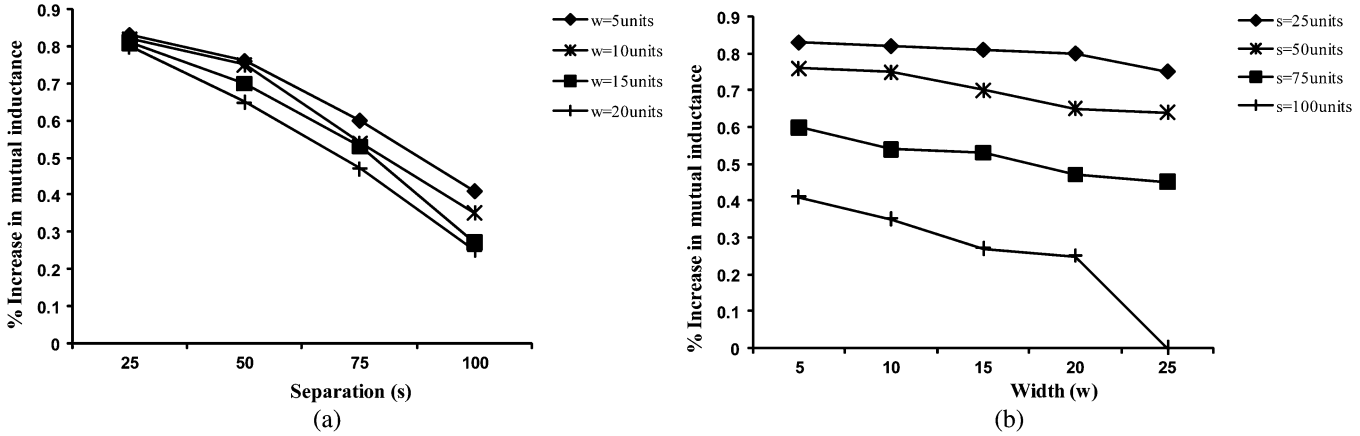


Fig. 11. Overall increase in the mutual inductance of a custom ring with an additional corner pair compared with the overall mutual inductance of a regular ring. Note that, the vertical axis is in % (e.g., $\approx$0.9% for $\mathtt{s} = 25, \mathtt{w} = 5$ units).

In this case, a regular segment of type R is compared with corner segments of types P and Q in order to observe the total increase in inductance of the transmission line of equal lengths due to the mutual inductance of the corner elements. Note that, these corners also exist in the traditional ROA topology but have been ignored in previous work in literature [8]. In Fig. 9, the variation in mutual inductance with a fixed width and a varying separation (and vice versa) is shown. It is seen that for a fixed width (separation), the increase in separation (width) causes an approximately linear decrease in the mutual inductance. This trend is reasonable as the wires are further apart, the mutual inductance is reduced. For a nominal case implementation of separation s=40 units and width $w = 20$ units of the transmission lines of the rotary rings, each corner segment (of type P or Q) leads to a 79.9% increase in the mutual inductance when compared with a regular segment (of type R).

Second, the results for the "gap" analysis in Section IV-B are presented. In this case, the opposite edges of the custom ring are divided into regular segments of type R. The opposite edges in each segment have an equal length $l$ with the gap $G$ varied to analyze the effect of mutual inductance. In Fig. 10, the plot shows the decrease in mutual inductance with an increase in the gap for the CROA methodology tested on the R1 benchmark circuit. With a grid size of 1000 *units* (corresponding to R1 circuit), it is seen that if the minimum gap is approximately 70% of the grid size, the mutual inductance is negligible $(< 0.000022\%)$. For the custom ring implementations, the gap has to be fixed as greater than 70% of the grid size to eliminate the "gap" effect. In a regular ring of conventional ROA, the gap is $P_r/4$ long. This gap is long enough so that the mutual inductance contributed by the gap can be safely neglected, which has been the norm.

Third, the results for the overall "custom ring topology" analysis in Section IV-C are presented. In Fig. 11, the plots of the overall increase in the total mutual inductance of a custom ring with six corners are shown compared to a regular ring with varying separation and width. For all practical dimensions (separation and width), the PEEC computations suggest that the change in the total mutual inductance is under 1% for the CROA ring topology. At this scale, it is seen that for a fixed width (separation), the increase in separation (width) causes the mutual inductance to decrease. Note that, although the increase in the total mutual inductance for every corner segment is very high (about 79.9%) compared to a regular segment, the overall increase in total mutual inductance for every additional corner pair of a custom ring is not very high (under 1%) compared to the overall mutual inductance of a regular ring. This trend is reasonable as the number of regular segments in a custom ring is much higher than the number of corner segments.

A series of PEEC computations are performed for the CROA implementations of nominal dimensions (separation and width) but with a varying number of corners. In order to compute the oscillation frequencies, the length units of the R1–R5 benchmark circuits are scaled to reflect the pioneering implementation in [7]. For instance a perimeter of 50 000 units for R1 corresponds to a perimeter of 3200 $\mu$m in a 180-nm technology. For the ring with the minimum number of corners [shown in Fig. 8(a)], the mutual inductance analysis results in 42 straight segments and 4 corner segments. The total mutual inductance on this structure is computed as 0.1288 nH. The frequency computed using (3) for the CROA topology with the minimum number of corners is 4.57 GHz. Similarly, for the ring with the maximum number of corners [shown in Fig. 8(b)], the analysis results in 34 straight segments and 12 corner segments. The total mutual inductance in this case is computed as 0.1485 nH and the computed frequency is 4.25 GHz. For a nominal custom ring with eight corners, the analysis results in a total mutual inductance of 0.1399 nH and the computed frequency is 4.38 GHz. The results are shown in Table II, under the third column labeled $F_{\mathrm{th}_2}$, which is the frequency computed with (3) using the mutual inductance (computed using PEEC analysis) for the corresponding number of corner segments. In Table II, the first column depicts the number of corners in the CROA topology. The second column shows $F_{\mathrm{th}_1}$, which is the frequency computed using (3) without considering the mutual inductance effect due to the corner segments. This frequency is the same across CROA topologies with different number of corners, as the additional mutual inductance due to the corner segments is neglected. The fourth column depicts the variation in the computed frequency due to the added mutual inductance. When compared with $F_{\mathrm{th}_1}$, the change in $F_{\mathrm{th}_2}$ increases from

TABLE II
COMPARISON OF $F_{\text{th}_1}$ (FREQUENCY WITHOUT CORNER MUTUAL INDUCTANCE) AND $F_{\text{th}_2}$ (FREQUENCY WITH CORNER MUTUAL INDUCTANCE COMPUTED FROM PEEC ANALYSIS), AS APPROXIMATED BY (3)

| CROA topology | $F_{th_1}$ (GHz) | $F_{th_2}$ (GHz) | Variation |
|---|---|---|---|
| Min corners (4) | 4.70 | 4.57 | 2.76% |
| Nom corners (8) | 4.70 | 4.38 | 6.81% |
| Max corners (12) | 4.70 | 4.25 | 9.57% |

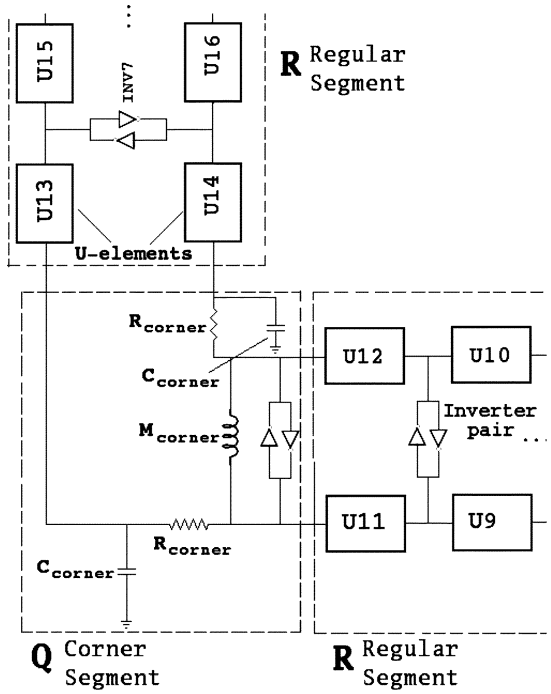


Fig. 12. Portion of the SPICE simulation schematic.

2.76% to 9.57%, for the minimum number of corners (4) to the maximum number of corners (12) of the custom ring topology, respectively.

### C. Simulation Results With SPICE

In this paper, SPICE models are created using U-element [21] models and the PEEC analysis results for mutual inductance. The U-model in HSPICE effectively captures the resistance, self inductance and self capacitance of the transmission lines. The U-model also captures the mutual inductance and mutual capacitance values between the parallel transmission line pairs. However, the mutual inductance of the transmission lines at the corners are significantly different, which are incorporated separately. Consequently, the results of the PEEC analysis are used to model the mutual inductance between the U-elements and the self capacitance and resistance of the corner elements as a part of the SPICE model. Such a model captures the expected behavior of the corner segments. Based on the perimeter of the rotary ring, 24 transmission lines segments are used and a total of 24 uniform cross coupled inverter pairs are placed at equal distances on each rotary ring [7]. A portion of the proposed simulation schematic setup for rotary clocking with the U-Elements and the parasitics (for corners) is shown in Fig. 12.

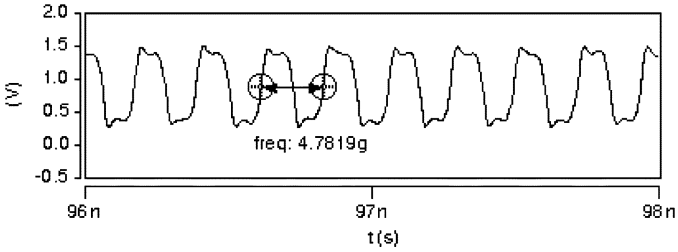


Fig. 13. Clock signal simulated for a ring with no parasitics at the corners.

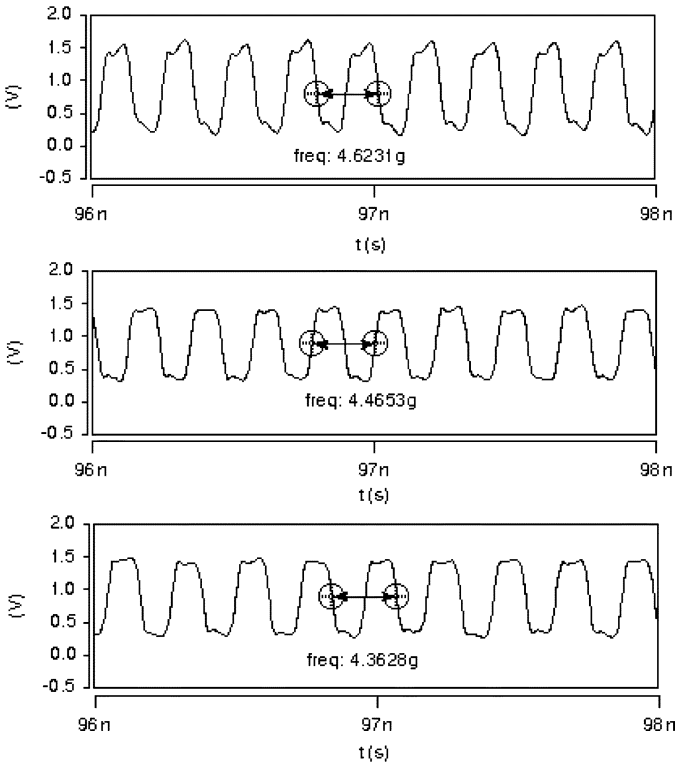


Fig. 14. Clock signals obtained for CROA topologies with a varying number of corner segments.

TABLE III
COMPARISON OF FREQUENCY $F_{\text{sim}_1}$ WITHOUT CORNER PARASITICS AND FREQUENCY $F_{\text{sim}_2}$ WITH CORNER PARASITICS (COMPUTED FROM PEEC ANALYSIS), AS SIMULATED IN HSPICE

| CROA topology | $F_{sim_1}$ (GHz) | $F_{sim_2}$ (GHz) | Accuracy imp |
|---|---|---|---|
| Min corners (4) | 4.78 | 4.62 | 3.35% |
| Nom corners (8) | 4.78 | 4.46 | 6.69% |
| Max corners (12) | 4.78 | 4.36 | 8.79% |

First, the rotary clocking circuit is set up in SPICE for the CROA topology. In this setup, the parasitics due to the corner and the gap segments are neglected (which is the state of the previous research in [5], [7], and [8]). The clock waveform obtained for this setup is shown in Fig. 13. The simulated clock frequency is 4.78 GHz.

Next, the SPICE model is modified in order to incorporate the parasitic components including the mutual inductance elements computed in the PEEC analysis. The clock waveforms obtained for the CROA topology with minimal corners (4 corners), nominal corners (8 corners), and the maximum number of

TABLE IV
COMPARISON OF SIMULATED FREQUENCY $F_{\mathrm{sim}_2}$ (CORNER PARASITICS, SPICE) WITH THE THEORETICAL FREQUENCY $F_{\mathrm{th}_2}$ (CORNER PARASITICS, PEEC) AND WITH THE THEORETICAL FREQUENCY $F_{\mathrm{th}_1}$ (PEEC IN [8])

| CROA topology | $F_{sim_2}$ (GHz) | $F_{th_2}$ (GHz) | Variation | $F_{sim_2}$ (GHz) | $F_{th_1}$ (GHz) | Variation |
|---|---|---|---|---|---|---|
| Min corners (4) | 4.62 | 4.57 | 1.08% | 4.62 | 4.70 | 1.70% |
| Nominal corners (8) | 4.46 | 4.38 | 1.79% | 4.46 | 4.70 | 5.11% |
| Max corners (12) | 4.36 | 4.25 | 2.52% | 4.36 | 4.70 | 7.80% |

corners (12 corners) are presented in Fig. 14. The frequencies for the minimal, nominal and the maximum number of corners are, 4.62, 4.46, and 4.36 GHz, respectively. It is observed that the clock frequency decreases with increasing number of corners. This decrease is expected because the mutual inductance increases with the increasing number of corners of the CROA topology.

In Table III, the SPICE simulation results with and without corner parasitics for a different number of corners are compared. The first column depicts the number of corners in the CROA topology. The second column shows the simulated frequency $F_{\mathrm{sim}_1}$, without considering the parasitics due to the corner segments. The frequency $F_{\mathrm{sim}_1}$ stays the same for different CROA topologies as parasitics due to the corners are neglected. The third column shows the simulated frequency $F_{\mathrm{sim}_2}$, using the mutual inductance (computed using PEEC analysis) for the corresponding number of corner segments. The fourth column depicts the variation in $F_{\mathrm{sim}_2}$ compared with $F_{\mathrm{sim}_1}$. The variation is the improvement in accuracy of the proposed simulated frequency due to the mutual parasitic analysis presented in this paper. When compared with $F_{\mathrm{sim}_1}$, the frequency accuracy of $F_{\mathrm{sim}_2}$ improves from 3.35% to 8.79%, for the minimum number of corners to the maximum number of corners of the CROA topology, respectively. For the regular ROA topology with four corners, the improved SPICE models increase the frequency accuracy by 3.35%. Note that, the frequency accuracy improved is computed over the frequency estimated in (3) with the formula $\mathrm{Accuracy\ Imp} = (F_{\mathrm{sim2}} - F_{\mathrm{sim1}})/(F_{\mathrm{sim1}}) \times 100$.

In order to evaluate the accuracy of the approximations in the theoretical computations in (3), the simulated frequencies (using SPICE) are compared with the theoretical frequencies computed using (3). In Table IV, the theoretical clock frequencies $F_{\mathrm{th}_2}$ [computed using (3)] and the simulated clock frequencies $F_{\mathrm{sim}_2}$ (using SPICE) are tabulated. Note that, the same mutual inductance values computed using PEEC analysis are used in computing the theoretical frequencies and in the simulations. The results of the clock frequencies from SPICE simulations are in agreement with the theoretical frequencies computed from (3) with a small variation (1.08% to 2.54% for min corners to max corners case). Thus, the theoretical approximation in (3) provides a reasonable approximation to the expected clock frequency. Further, the comparison of the simulated frequencies and the PEEC approximation in [8] without considering the mutual inductance due to corners, leads to an accuracy improvement of 1.70% to 7.80%, from minimum corners to the maximum corners of the CROA topology, respectively. Thus, the theoretical computation in (3) is not an accurate frequency estimate for CROA topologies with high number of corners, if the mutual parasitics information is not considered.

## VI. IMPACT ON THE OSCILLATION FREQUENCY

Recall from Section II that the inductance [in (4)] and the capacitance [in (5)] properties characterize the frequency of oscillation. The oscillation frequency is approximated as $f_{\mathrm{osc}} \approx (1)/(2\sqrt{L_T C_T})$. This relation can be rewritten [using (5)] as

$$f_{\mathrm{osc}} \approx \frac{1}{2\sqrt{(L_T)(\sum C_{\mathrm{reg}} + \sum C_{\mathrm{inv}} + \sum C_{\mathrm{ring}} + \sum C_{\mathrm{wire}})}} \tag{13}$$

where $L_T$ is the total inductance that does not include the mutual inductance due to the corners of the rotary ring. As analyzed in Section IV, for a more accurate analysis, the corner parasitics have to be included in the computation. When corner parasitics are included, the frequency of the regular rotary oscillatory array is estimated by

$$f_{\mathrm{roa}} \approx \frac{1}{2\sqrt{(L_{\mathrm{roa}}) \times (C_{\mathrm{roa}})}} \tag{14}$$

where the total inductance $L_{\mathrm{roa}}$ on the ROA is estimated by

$$L_{\mathrm{roa}} \approx L_T + M_{\mathrm{corner}} \times N_c. \tag{15}$$

The total capacitance $C_{\mathrm{roa}}$ is estimated by

$$C_{\mathrm{roa}} \approx \sum C_{\mathrm{reg}} + \sum C_{\mathrm{inv}} + \sum C_{\mathrm{ring}} + \sum C_{\mathrm{wire}} + C_{\mathrm{corner}} \times N_c \tag{16}$$

where $M_{\mathrm{corner}}$ and $C_{\mathrm{corner}}$ are the mutual inductance and capacitance exhibited by each corner, respectively. $N_c$ is the number of corners (four in ROA). Although the absolute frequency figures are not comparable, it is clear that due to the additional parasitics at the corners, $f_{\mathrm{roa}} < f_{\mathrm{osc}}$.

As reported in Section V-A, an average of 39.25% of the tapping wirelength can be saved in CROA. As analyzed in Section IV, however, the design of the CROA topology also causes a change in the inductance due to the varying corners. Overall, the frequency of the CROA is given by

$$f_{\mathrm{croa}} \approx \frac{1}{2\sqrt{(L_{\mathrm{croa}}) \times (C_{\mathrm{croa}})}} \tag{17}$$

where $L_{\mathrm{croa}}$ is estimated by

$$L_{\mathrm{croa}} \approx L_T + M_{\mathrm{corner}} \times N_c. \tag{18}$$

$C_{\mathrm{croa}}$ is estimated by

$$C_{\mathrm{croa}} \approx \sum C_{\mathrm{reg}} + \sum C_{\mathrm{inv}} + \sum C_{\mathrm{ring}} + (1 - 39.25\%)$$

$$\times \sum C_{\text{wire}} + C_{\text{corner}} \times N_c. \quad (19)$$

Note that, $N_c \geq 4$ for CROA, and $\text{Max}(N_c) = 12$ in the current CROA design. Depending on the granularity of the grid and the gap specifications (so that the mutual inductance due to the gap is negligible) the $\text{Max}(N_c)$ can be different for other CROA topologies. In CROA, the wirelength savings (resulting in smaller $\sum C_{\text{wire}}$) overcomes the effects of additional parasitics due to the increased corners, and $f_{\text{croa}} \geq f_{\text{osc}}$. In cases where the frequency increase is undesirable, the perimeter of the custom rings in CROA topology can be increased proportionately in order to compensate for the increase in frequency.

## VII. Conclusion

In this paper, a novel design methodology called the CROA is presented, demonstrating a tapping wirelength saving of 39.25% over the traditional ROA. Also, a methodology to analyze the parasitics resulting from the corners in the ring is presented. Simulation based analysis are performed for the clock waveforms of different CROA topologies incorporating the parasitics. When the mutual inductance exhibited by the corner segments of the rotary rings are considered, the resultant clock frequency is observed to be 8.79% less (assuming the wirelength remains the same) than the expected frequency from the *LC* circuit-based simplified formulations in [7].

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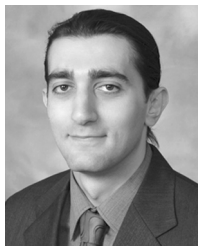

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# A Reconfigurable Clock Polarity Assignment Flow for Clock Gated Designs

Jianchao Lu, *Student Member, IEEE*, Ying Teng, *Student Member, IEEE*, and Baris Taskin, *Member, IEEE*

***Abstract*—This paper presents a novel clock polarity assignment flow which introduces post-silicon reconfigurability. The proposed methods inserts *XOR* gates at one level of the clock tree to facilitate polarity assignment instead of the conventional buffer/inverter replacement based polarity assignment in previous works. The polarity of the *XOR* gates can be reconfigured for different modes of clock gating (sleep mode, busy mode, etc.) such that a further peak current reduction is obtained for each mode. The method is integrated into an industrial design flow to study the practicality. Experimental results show that the worst case peak current on a clock tree can be reduced by 33.3% by assigning polarity to *XOR* gates at the sink level of the clock tree. An additional 12.8% reduction in the worst case peak current can be achieved by reconfiguring the polarity assignment based on the clock gating information. The proposed flow increases the area by 7.1% but reduces the total power consumption by 23.8% and reduces the global skew degradation (due to polarity assignment) from 19.3ps to 8.8ps. The insertion of *XOR* gates at non-sink nodes is also studied to further reduce the skew degradation and the area overhead. The skew degradation of 19.3ps in previous works is reduced to 1.7ps and the area increase is limited to 5.9% when the *XOR* gates are inserted at a non-sink level of the clock tree.**

***Index Terms*—Clock network synthesis, physical design, polarity assignment.**

## I. Introduction

The supply voltage levels of the modern electronic systems continue to decrease (despite not scaling at the same rate as other feature sizes) due to the prevailing applications of low power designs. However, the decreased voltage levels negatively affect the reliability of the systems due to reduced noise margins. As a result, the electronic systems are susceptible to on-chip variations such as power/ground noise [1]. The power/ground noise is harmful to both the timing and the reliability of an electronic system. A 5% drop on the supply voltage may increase the delay of the cells by 15% or even more with technology scaling according to [2]. The power/ground noise may also cause the circuit to function incorrectly. The peak current on supply rails (vdd/gnd rails) is a major source of the power/ground noise due to the inductance effect which is highly undesirable. The peak current on chip is induced by the simultaneous switching in the same direction of the cells (low to high or high to low). The clock tree is thus a significant source of peak current due to all sink buffers switching simultaneously at the clock edges. Reducing the peak current induced by the sink buffers of the clock tree is demonstrated to be an effective way of reducing the peak current on the chip [3].

There are multiple effective methods to reduce the peak current on the clock tree. In [4–7], clock skew scheduling [8] is applied to eliminating the simultaneous switching of the clock tree buffers. By applying clock skew scheduling, the clock arrival times to different registers become different so the clock buffers do not switch simultaneously at the clock edges. Clock skew scheduling, however, is not preferred in mainstream design flow due to the hardship at the verification stage. *Polarity assignment* methods are proposed for peak current reduction under zero clock skew [3, 9–14]. The basic idea of polarity assignment is to reduce the peak current introduced by clock tree by permitting some of the clock sink buffers to switch in the same direction with the clock signal while the other sink buffers switch in the opposite direction such that the current is distributed between the vdd and gnd rails at the clock edges. The polarity assignment methods typically involve replacing buffers with inverters or vice versa on an existing clock tree. Although the input to the polarity assignment problem is a zero skew clock tree, skew may be induced by the replacement of buffers with inverters and the replacement of positive edge-triggered flip-flops with negative edge-triggered flip-flops. Furthermore, cell overlapping may occur as the dimensions of the buffers and inverters are non-identical. This necessitates an incremental placement which is undesirable as the quality of the clock tree is compromised with placement change.

In this paper, a new method of performing polarity assignment is proposed, which eliminates the need to replace buffers with inverters (and positive edge-triggered *DFF*s with negative edge-triggered *DFF*s). The novel method utilizes *XOR* gates as the buffering elements on one level of a clock tree network, which are reconfigured for clock polarity. Reconfigurable polarity assignment is particularly beneficial for clock-gated trees. The clock gating [15] is a commonly used technique to reduce the power consumption on a circuit. In a clock gated system, some clock tree branches are gated such that when the registers in those branches do not change states for some cycles, the clock signal is stopped from propagating to the sink registers on those branches. It is shown for the first time in this paper that the reconfigurability of polarity assignment for clock gated circuits is essential as the peak current profiles change with each clock gating event.

The clock tree synthesis with polarity assignment method proposed in this work has the following features and novelties:

1) The proposed method eliminates the replacement of buffers and registers, and thus, the need for incremental

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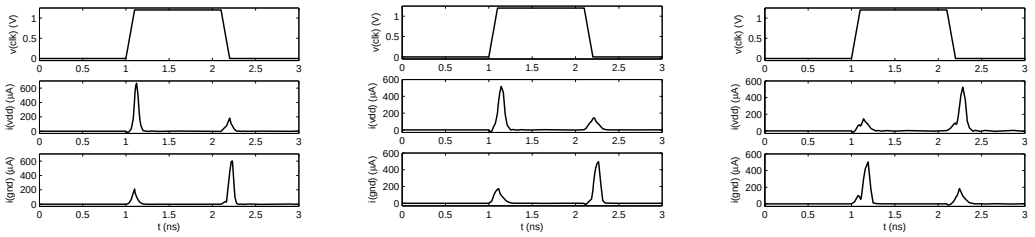



(a) Buffer *BUFX2* simulation. (b) Positive polarity *XORX2* gate simulation. (c) Negative polarity *XORX2* gate simulation.

Fig. 1. Buffer and *XOR* gate simulation in *HSPICE*.

placement. The polarity assigned tree has less clock skew degradation and power dissipation at the expense of limited area increase.

2) The proposed method has the reconfigurability feature in assigning polarity during runtime for clock gating.
3) Any clock polarity assignment method that works on the sink level buffers can be applied on the clock tree with the proposed reconfigurability feature.
4) The proposed methods can be seamlessly integrated with the current industrial design flow.

The rest of the paper is organized as follows. In Section II, the preliminaries of clock gating and proposed reconfigurability are described. In Section III, the proposed clock tree synthesis scheme with *XOR* gates insertion is proposed. In Section IV and Section V, the polarity assignment methods for *XOR* gates inserted at the sink level and non-sink level of the clock tree are proposed, respectively. In Section VI, the experimental results of the proposed method are presented. The paper is summarized in Section VII.

## II. Preliminaries

The peak current on a synchronous system often occurs at the rising edge of the clock signal when a large number of gates and registers switch simultaneously. The peak current drawn by the clock tree is critical due to all the clock buffers switching at every clock period, whereas not all the logic gates switch simultaneously or at every clock signal. An *HSPICE* simulation result on the current drawn by the vdd/gnd rails of a clock buffer is shown in Figure 1(a). In the simulation, a clock buffer *BUFX2* from a 90nm library [16] is used. The peak current on the power rails $[i(vdd)]$ occurs at the rising edge of the clock signal. The peak current on the ground rails $[i(gnd)]$ occurs at the falling edge of the clock signal. Polarity assignment intentionally permits some buffers to switch in the same direction with the clock signal and the other buffers to switch in the opposite direction with the clock signal such that the current will not accumulate on vdd or gnd rails during rising or falling edge of the source clock signal, respectively. The polarity assignment methods, as demonstrated in previous works [3, 9–13], involve replacing buffers by inverters or vice versa on the clock tree. However, such a replacement scheme not only increases the clock skew but also affects the robustness of the clock tree because of the mismatch of the clock buffers after polarity assignment. The clock skew degradation can be so dramatic that some previous polarity assignment methods have advocated clock tree re-synthesis after polarity assignment [11]. The proposed tree with an *XOR*-based level eliminates the necessity to perform incremental placement or clock tree re-synthesis (which can only be performed pre-silicon) and enables post-silicon reconfigurability.

### A. XOR Gate Insertion for Polarity Assignment

In the proposed clock tree synthesis scheme, the *XOR* gates are inserted at one level of the clock tree (sink or non-sink) to enable the reconfigurability of the polarity assignment.

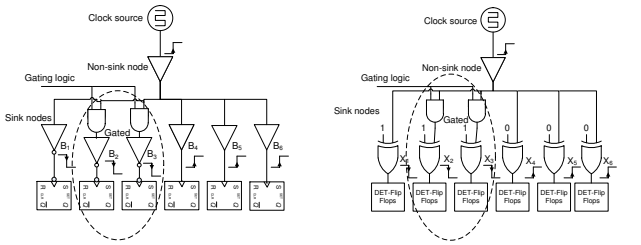
Consider a two-input *XOR* gate with inputs $A$ and $B$ and output $Q$. Let the input terminal $B$ be driven by the clock signal $clk$. If a high voltage is applied to the input terminal $A$, the negation of the input clock signal $\neg clk$ will appear on the output terminal $Q$. If a low voltage is applied to the input terminal $A$, the same phase clock signal $clk$ will appear on the output terminal $Q$. Thus, the polarity of the clock signal at the output of the *XOR* gate is reconfigurable through the control input $A$. The logic function of the *XOR* gate is shown in Table I.

TABLE I
The logic function of XOR.

| Input A | Input B | Output Q |
|---|---|---|
| 1 | clk | $\neg clk$ |
| 0 | clk | clk |

The peak current characteristics of the *XOR* gate for polarity assignment is similar to a buffer and inverter for positive and negative polarity configuration, as demonstrated in Figure 1(b) and Figure 1(c), respectively, using the *XORX2* gate from the same 90nm technology library [16].

In addition to enabling reconfigurability, the *XORX2* gate is advantageous in terms of peak current compared to the $BUFX2$ gate with similar slew rate ($7.8gV/\mu s$ vs. $8.3gV/\mu s$ driving the same capacitive load of 60 $fF$). In particular, the *XORX2* gate draws a maximum of 531 $\mu A$ while the *BUFX2* gate draws a maximum of 667 $\mu A$ during the edges of the clock signal. The trade-off of *XOR* insertion is the possible area overhead compared to the buffers. This is investigated thoroughly in experimentation to identify critical trade-offs in delay, power, area and peak current.




(a) Polarity assigned clock tree with clock gating.

(b) Reconfigurable clock tree for gated circuit.

Fig. 2. Clock tree illustration with clock gating.

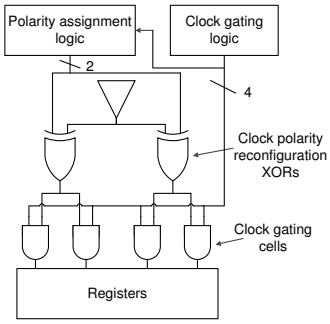
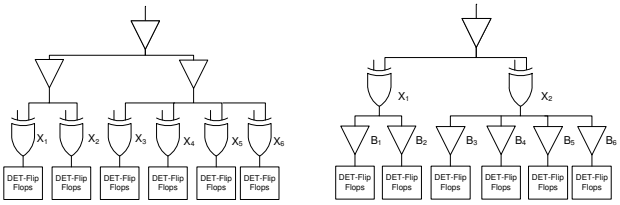



Fig. 3. The hardware for clock gating with reconfigurable polarity assignment.




(a) *XOR* gates inserted at the sink level.

(b) *XOR* gates inserted at the non-sink level.

Fig. 4. *XOR* gates insertion on clock tree.

### *B. Reconfigurable Polarity Assignment*

Clock gating [15] is a commonly used technique for reducing the power consumption on clock tree. Previous polarity assignment methods ignore clock gating, which is not optimal due to the dynamic changes in the switching activity of the clock sink buffers after gating. For instance, a polarity assigned clock tree with clock gating is shown in Figure 2(a). Let the sink buffers $B_1$–$B_3$ be assigned with negative polarity and the sink buffers $B_4$–$B_6$ be assigned with positive polarity after the polarity assignment. When clock gating occurs, the buffers $B_2$ and $B_3$ are gated and the peak current reduction effect is no longer optimal. The conventional clock polarity assignment methods do not allow the reconfigurability polarity assignment during runtime due to the following difficulties:

1) The polarity assignment is achieved through replacing buffers with inverters or vice versa at the CTS stage. This procedure can not be performed post-silicon.
2) In order to guarantee the synchronicity of the registers, the type of the registers (positive or negative edge triggered) has to be determined based on the polarity assignment at the pre-silicon stage.

By inserting the *XOR* gate at one level of the clock tree, the first difficulty is overcome because the polarity of the output signal of the *XOR* gate can be controlled by one control input signal. There is no need to replace buffers with inverters. The second difficulty is overcome by using the double edge triggered (DET) flip-flops [17, 18]. The DEF flip-flop is triggered at both the rising and the falling edges of the clock signal such that these flip-flops latch in data at both the clock rising and the falling edges. Despite having a different polarity of the clock signal at the sink level after polarity assignment, as long as the clock edges (either rising or falling edge) arrive at the same time, the synchronicity of the circuits is maintained.

In the proposed design, DET flip-flops are used as registers instead of single edge triggered registers as shown in Figure 2(b). Control inputs of the *XOR* gates are assigned to binary 0s and 1s to perform polarity assignment. After clock gating on *XOR*s $X_2$ and $X_3$, the control input to one of the positive polarity *XOR*s ($X_4$, $X_5$, $X_6$) can be assigned to 1 in order to balance the peak currents on the vdd/gnd rails.

The proposed reconfigurable polarity assignment method is proposed for clock-gated designs, which already includes the clock gating logic. Similar to the clock gating system [19], the hardware for clock gating with reconfigurable polarity assignment is shown in Figure 3. The desirable polarities corresponding to each gating logic are precomputed and stored in the polarity assignment logic. The clock gating logic triggers the corresponding polarity assignment to be applied on the control input of the *XOR* gates. The area and routing overhead for the polarity assignment logic is appended to the overheads planned for clock gating logic.

## III. Clock Tree Synthesis Scheme with *XOR* Gates Insertion

In Section III-A, the effects of *XOR* gates insertion on different levels of the clock tree are studied. In Section III-B, the peak current is investigated as a local effect on a circuit.

### *A. XOR Gate Insertion on the Clock Tree*

In the proposed clock tree synthesis scheme, *XOR* gates are inserted at one level of the clock tree to facilitate the reconfigurable polarity assignment. However, different effects are observed when the *XOR* gates are inserted at different clock tree levels as demonstrated in Figure 4. If the *XOR* gates are inserted at the sink level of the clock tree, a larger overhead possibly in terms of delay, area and power—depending on the cell library—can be observed. On the other hand, if the *XOR* gates are inserted at the non-sink level of the clock tree, the overhead is reduced but there is less granularity in polarity assignment. This is because if a non-sink *XOR* gate is assigned to one polarity, all its sink buffers have the same polarity as the driving *XOR* gate. The change in insertion delay cannot be generalized as the delay through the *XOR* gate depends on the capacitive load and input slew at the particular sink or non-sink node.

### B. Area Definition

The peak current on vdd/gnd rails is a local effect as the cells that are placed further away do not connect to the same vdd/gnd pads. Consequently, the polarity assignment for peak current optimization is typically performed per local area [11]. The areas are defined based on the connections of the cells to the vdd/gnd pads [20]. The power/ground network is synthesized at the floorplanning stage prior to clock tree synthesis, thus the local areas for polarity assignment are known.

For simplicity of the analysis and without loss of generality, the chip areas in the experiments are evenly partitioned for the vdd/gnd strips and the polarity assignment is performed on each local area individually. In Figure 5, a clock tree example on s15850 from the ISCAS'89 benchmark circuits is illustrated. The chip area in Figure 5 is evenly partitioned into four areas labeled $A_1$ through $A_4$ based on the vdd/gnd straps in physical design.

If the *XOR* gates are inserted at the sink level only, the polarity assignment can be performed separately per area. However, if the *XOR* gates are inserted on non-sink level, it is possible that one *XOR* gates may drive several sink buffers in different areas such that the polarity of one *XOR* gate may affect peak current in different areas. For instance, in Figure 5, it is observed that the highlighted non-sink *XOR* gate (shown as a black square) in area $A_1$ drives sink buffers (shown as black triangles) located in both area $A_1$ and $A_2$. Thus, assigning polarities for *XOR* gates inserted at the sink level and non-sink level of the clock tree are two different problems to be addressed in Sections IV and V, respectively.

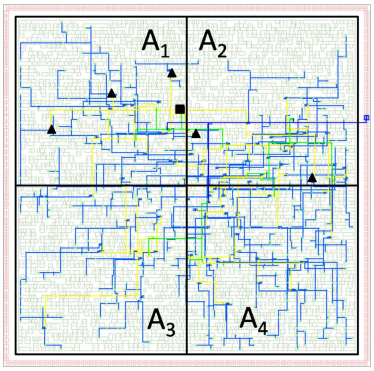



Fig. 5. A clock tree synthesized with *XOR* gates.

## IV. Polarity Assignment on Sink Level *XOR* Gates

If the *XOR* gates are inserted at the sink level of the clock tree, any polarity assignment method, including previously offered methods, can be applied. In this paper, the fast greedy algorithm proposed in [14] is adopted.

### A. Problem Formulation

The problem definition of the polarity assignment in [14] is:

*Given a synthesized clock tree with one level of XOR gates inserted, the definition of each local area $A_k$ for power/ground network connections and XOR gates locations, compute the polarity $P_i$ of each XOR gate $X_i$ such that a minimum worst case peak current is observed on vdd/gnd rails.*

The binary values 0 and 1 of the polarity variable $P_i$ represent the positive polarity and negative polarity of *XOR* gate $X_i$, respectively. Let $I^i_{v+}$ and $I^i_{g+}$ represent the peak current on vdd rails and gnd rails for *XOR* gate $X_i$ with positive polarity, respectively. Let $I^i_{v-}$ and $I^i_{g-}$ represent the peak current on vdd rails and gnd rails for *XOR* gate $X_i$ with negative polarity, respectively. The objective of the peak current reduction by applying the polarity assignment is as follows:

$$\min\Big[\max_{\forall A_k}\Big(\sum_{X_i\in A_k}(1-P_i)I^i_{v+},\ \sum_{X_i\in A_k}(1-P_i)I^i_{g+},\ \sum_{X_i\in A_k}P_iI^i_{v-},\ \sum_{X_i\in A_k}P_iI^i_{g-}\Big)\Big]. \tag{1}$$

The objective of the formulation is to reduce the worst case peak current on the vdd and gnd rails over all local areas $A_1$–$A_4$. Since the variables in each of the variables pairs $\{I^i_{v+}, I^i_{g+}\}$ and $\{I^i_{v-}, I^i_{g-}\}$ are associated with each other, optimizing the peak current on vdd rails optimizes the peak current on gnd rails as well. Moreover, optimizing the peak current on rising edges of the clock signal optimizes the peak current on falling edges of the clock signal as well. The optimization problem becomes minimizing the peak current on the worst rail (either vdd or gnd) or worst clock edge (either rising or falling edges). The objective is thus simplified as shown in Table II. The parameters $I^i_+$ and $I^i_-$ are calculated as:

$$\begin{aligned} I^i_+ &= \max(I^i_{v+},\ I^i_{g+}),\\ I^i_- &= \max(I^i_{v-},\ I^i_{g-}). \end{aligned} \tag{2}$$

The formulation is similar to the bottleneck assignment problem in [21–23]. The problem aims to minimize the worst case peak current over all the areas by assigning the polarity of *XOR* gates.

TABLE II
Polarity assignment problem formulation for *XOR* gates inserted at the sink level [14].

| Minimize peak current on power rails | |
|---|---|
| min | $\Big[\max_{\forall A_k}\Big(\sum_{X_i\in A_k}(1-P_i)I^i_+,\ \sum_{X_i\in A_k}P_iI^i_-\Big)\Big]$ |
| s.t. | $P_i\in\{0,1\},\forall\ X_i$ |

### B. A Greedy Polarity Assignment Method

In order to assign the polarity efficiently, a greedy algorithm is proposed in [14]. The algorithm is presented in Algorithm 1. The algorithm greedily assigns an unassigned *XOR* gate which has the least positive or negative polarity peak current weight with the corresponding polarity such that the worst case peak current is minimized. The peak current weight $I^i_+$ and $I^i_-$ for each *XOR* gate depends on the size of the gate and

**Algorithm 1** Greedy sink level polarity assignment [14].

**Input:** The peak current weight $I_+^i$ and $I_-^i$ of each *XOR* $X_i$
**Output:** The polarity $P_i$ of each *XOR* gate $X_i$

**for** Each area $A_k$ **do**
  Set $U_k = \{X_m | X_m \in A_k\}$. Find *XOR*s $X_i$ and $X_j$ in $U_k$ such that: $I_+^i = \min_{\forall X_l \in U_k} I_+^l$, $I_-^j = \min_{\forall X_l \in U_k, l \neq i} I_-^l$. Set $P_i = 0$, $P_j = 1$. $U_k = U_k - \{X_i\}$, $U_k = U_k - \{X_j\}$;
  **while** $U_k \neq \emptyset$ **do**
    Find *XOR* $X_i$ such that $I_+^i = \min_{\forall X_l \in U_k} I_+^l$. Find *XOR* $X_j$ such that $I_-^j = \min_{\forall X_l \in U_k} I_-^l$;
    **if** $\sum_{\forall X_l \in A_k, X_l \notin U_k} (1-P_l) I_+^l + I_+^i \geq \sum_{\forall X_l \in A_k, X_l \notin U_k} P_l I_-^l + I_-^j$ **then**
      Set $P_j = 1$, $U_k = U_k - \{X_j\}$;
    **else**
      Set $P_i = 0$, $U_k = U_k - \{X_i\}$;
    **end if**
  **end while**
**end for**

the capacitive load at the output. The algorithm returns the polarities $P_i$ of each *XOR* gate $X_i$. The algorithm obtains a feasible polarity assignment in $O(N \log N)$ time, where $N$ being the number of the *XOR* gates.

### C. Discussion on the Polarity Assignment Method

The greedy polarity assignment used in this paper is the one from [14]. A peak current improvement of 47% is reported in [14]. This level of peak current improvement is possible through polarity assignment on a modified buffered clock tree synthesis method from [24]. The *XOR* gate inserted trees in this work are synthesized using `IC Compiler`, using no clock tree re-synthesis. Thus, the level of improvement on the peak current is expected to be smaller than [14], but comparable to other polarity assignment methods without clock tree re-synthesis such as [3, 12, 13]. Other polarity assignment methods [3, 11–13], can be applied on the *XOR* based clock tree for peak current reduction without loss of generality.

## V. Polarity Assignment on Non-sink Level *XOR* Gates

The advantage of inserting *XOR* gates at the sink level is the higher granularity in polarity assignment. The disadvantage is the increased area since the *XOR* gates occupy more area in general and the relatively larger skew degradation due to the capacitive load at the sink level is often more significant. There is no polarity assignment method known in literature that directly assigns polarity for non-sink gates. To this end, a greedy method which assigns polarity on the clock tree with *XOR* gates inserted at the non-sink level is developed based on the method in Section IV.

### A. Problem Formulation

Each of the non-sink level *XOR* gates of the clock tree has several descendent sink buffers. These buffers, although sharing the same ancestor *XOR* gate, do not necessarily reside in the same local area (connect to the same vdd/gnd rail). As a result, assigning the polarity of one *XOR* gate may affect the polarity of the sink buffers in different areas. The problem is thus different from the polarity assignment on sink level *XOR* gates.

In this problem, the peak current weights $I_+^i$ and $I_-^i$ for positive and negative *XOR* gate, respectively, are represented by $M$-tuples instead of numbers, where $M$ is the number of local areas on chip. For instance, the chip area in Figure 5 is divided by four areas so the $I_+^i$ and $I_-^i$ of each *XOR* gate $X_i$ are represented by 4-tuples as shown:

$$I_+^i = \left( \sum_{B_j \in A_1 \cap S_i} I_+^j, \sum_{B_k \in A_2 \cap S_i} I_+^k, \sum_{B_m \in A_3 \cap S_i} I_+^m, \sum_{B_n \in A_4 \cap S_i} I_+^n \right), \quad (3)$$

$$I_-^i = \left( \sum_{B_j \in A_1 \cap S_i} I_-^j, \sum_{B_k \in A_2 \cap S_i} I_-^k, \sum_{B_m \in A_3 \cap S_i} I_-^m, \sum_{B_n \in A_4 \cap S_i} I_-^n \right), \quad (4)$$

where the set $S_i$ includes all the sink buffers $B_j$, which are the descendent of the *XOR* gate $X_i$. Each element $I_+^i(k)$ and $I_-^i(k)$ in the 4-tuples $I_+^i$ and $I_-^i$ represents the peak current weight in the local area $k$ of the *XOR* gate $X_i$. The peak current weight in one local area is calculated as the sum of the peak current weight of the sink buffers in that local area that are the descent of the *XOR* gate. The problem formulation for this polarity assignment problem is presented in Table III.

TABLE III
Polarity assignment problem formulation for *XOR* gates inserted at the non-sink level.

| Minimize peak current on power rails | |
|---|---|
| min | $\left[ \max_{\forall A_k} \left( I_{A_k}^+, I_{A_k}^- \right) \right]$ |
| s.t. | $I_{A_k}^+ = \sum_{\forall X_i \in E} \left[ \left( 1 - P_i \right) \sum_{B_j \in A_k \cap S_i} I_+^j \right]$, |
| | $I_{A_k}^- = \sum_{\forall X_i \in E} \left( P_i \sum_{B_j \in A_k \cap S_i} I_-^j \right)$, |
| | $P_i \in \{0,1\}, \forall X_i \in E$. |

In Table III, the parameters $I_{A_k}^+$ and $I_{A_k}^-$ represent the total positive polarity and negative polarity peak current for area $A_k$, respectively. The set $E$ is the set of all the non-sink *XOR* gates. The objective of the problem is still to minimize the worst case peak current over all the areas. However, the polarity assignment is only allowed on the non-sink *XOR* gates, which will determine the polarities of all the descendent sink buffers of the *XOR* gates.

### B. Polarity Assignment

In order to solve the polarity assignment efficiently, a greedy polarity assignment method, similar to the algorithm in [14] and discussed in Section IV-B, is proposed. The algorithm for solving the formulation in Table III is presented in Algorithm 2. The proposed polarity assignment first assigns the polarity on the *XOR* gates whose descendent sink buffers are in the same area. The algorithm then greedily assigns the polarity of the *XOR* gates which drive sink buffers in different

**Algorithm 2** Greedy non-sink level polarity assignment.

**Input:** The peak current weight $I_+^i$ and $I_-^i$ of each *XOR* $X_i$
**Output:** The polarity $P_i$ of each *XOR* gate $X_i$

Set $U = \{X_i | X_i \in E\}$
**for** Each area $A_k$ **do**
  Set $U_k = \{X_i | S_i \cap A_k = S_i\}$. Find *XOR*s $X_i$ and $X_j$ in $U_k$ such that: $I_+^i = \min_{\forall X_l \in U_k} I_+^l(k)$, $I_-^j = \min_{\forall X_l \in U_k, l \neq i} I_-^l(k)$. Set $P_i = 0$, $P_j = 1$. $U_k = U_k - \{X_i\}$, $U_k = U_k - \{X_j\}$, $U = U - \{X_i, X_j\}$, $I_{A_k}^+ = I_+^i(k)$, $I_{A_k}^- = I_-^i(k)$;
  **while** $U_k \neq \emptyset$ **do**
    Find buffer $i$ such that $I_+^i = \min_{\forall X_l \in U_k} I_+^l(k)$. Find buffer $j$ such that $I_-^j = \min_{\forall X_l \in U_k} I_-^l(k)$;
    **if** $I_{A_k}^+ + I_+^i(k) \geq I_{A_k}^- + I_-^j(k)$ **then**
      Set $P_j = 1$, $U_k = U_k - \{X_j\}$, $U = U - \{X_j\}$, $I_{A_k}^- += I_-^j(k)$;
    **else**
      Set $P_i = 0$, $U_k = U_k - \{X_i\}$, $U = U - \{X_i\}$, $I_{A_k}^+ += I_+^i(k)$;
    **end if**
  **end while**
**end for**
**for** Each $X_i \in U$ **do**
  **if** $\max_{\forall A_k}[I_{A_k}^+ + I_+^i(k)] \geq \max_{\forall A_k}[I_{A_k}^- + I_-^i(k)]$ **then**
    Set $P_i = 1$, $I_{A_k}^- += I_-^i(k), \forall\ A_k$;
  **else**
    Set $P_i = 0$, $I_{A_k}^+ += I_+^i(k), \forall\ A_k$;
  **end if**
**end for**

areas and minimize the peak current. The algorithm returns the polarities $P_i$ of each *XOR* gate $X_i$ in set $E$. The algorithm runs in $O(N \log N)$ time, where $N$ is the number of the sink buffers.

## VI. Experimental Results

The proposed clock tree synthesis scheme and the polarity assignment methods are applied on the ISCAS'89 circuits. The circuits are logically synthesized and physically synthesized using `Design Compiler` and `IC Compiler`, respectively. The operating frequency is set to 500 $MHz$ without any timing violations. The clock tree synthesis with *XOR* gates inserted on one level of the clock tree is performed by `IC Compiler`. The routed benchmark circuits are extracted using `StarRCXT`. The polarity computation methods are implemented using `C++` and the polarities are implemented using `Tcl` in `IC Compiler`. The peak current reduction effects are simulated using the `HSPICE` simulator in `Nanosim`.

In order to obtain an as fair as possible comparison between the *XOR* based polarity assignment flow and the conventional buffer/inverter based polarity assignment flow, the *XOR* gates and buffers/inverters with similar slew rate are used in clock tree synthesis. To this end, `HSPICE` simulations are performed on different sizes *XOR* gates and different sizes buffers/inverters in the selected cell library [16]. It is observed in the experiments that the buffer of size *X2* has the closest slew rate with the *XOR* of size *X2* under the same capacitive load (i.e. $8.3gV/\mu s$ vs. $7.8gV/\mu s$ driving the same capacitive load of 60 $fF$). Thus, in the experiments, the power and peak current of the circuit with the clock trees synthesized using *BUFX2* and clock trees synthesized using *BUFX2* and *XORX2* (at the sink or one non-sink level only) are compared.

### A. The Design of DET Flip-flops

The proposed method requires *XOR* gates insertion and the use of double edge triggered flip-flops. There are XOR gates of similar driving strength to buffers in the adopted cell library [16] but there are no *DET-FF*s. To this end, the *DET-FF*s of similar characteristics to the DFFs in the library are designed using custom design. The *DET-FF* adopts the same design as proposed in [18]. The layout of the *DET-FF* is designed using *Virtuoso* based on the 90 *nm* technology design rules as shown in Figure 6. The cell height of the designed *DET-FF* is restricted to be $2.88\mu m$, which is the height of the standard cells of the used library [16]. In order to gain a similar slew rate as the *DFF*s in the cell library, the inverter at the last stage of *DET-FF* is resized. Note that in the cell library [16], the design of *DFFX1* also uses a large inverter size at its last stage, thus, this is standard procedure to increase the driving strength. As a result, the designed *DET-FF* has the same driving strength (similar slew rate under the same capacitive load) as that of the *DFFX1*, which is used to synthesize all the ISCAS'89 circuits.

The characteristics of the *DFFX1* in the standard cell library and the designed *DET-FF* are compared in Table IV. All the information is obtained by driving a $60fF$ capacitive load under the same operating frequency $500MHz$. As observed in the largest benchmark circuit $s38584$, the average load of the *DFFX1* is only $16.5fF$. Thus an overly conservative capacitive load of $60fF$ is chosen to compare the characteristics of the *DFFX1* and the *DET-FF*. Although the total area of the *DET-FF* is larger than *DFFX1* in the library [16], the *DET-FF* reduces the power consumption. Moreover, the $clk-to-q$ delay of the *DET-FF* is smaller than that of *DFFX1*, which is similar to the result in [18]. The decreased delay potentially leads to an improved timing slack.

TABLE IV
The characteristics of the *DFFX1* and the designed *DET-FF* driving a capacitive load of 60 $fF$.

| Regs type | Area ($\mu m^2$) | Slew ($gV/\mu s$) | Delay (ps) | Power ($\mu W$) |
|---|---|---|---|---|
| *DFFX1* | 24.9 | 4.85 | 244 | 105.8 |
| *DET-FF* | 28.0 | 4.80 | 160 | 91.5 |

### B. Polarity Assignment with XOR Gates

The peak current reduction effects of reconfigurable polarity assignment for the clock tree with *XOR* gates inserted at the sink level are summarized in Table V. The clock tree information such as the number of sink clock tree buffers, number of *XOR* gates inserted are presented in the columns "# of ct bufs" and "# of *XOR*s", respectively. The peak current information

TABLE V
RECONFIGURABLE POLARITY ASSIGNMENT WITH *XOR* GATES INSERTED AT THE SINK LEVEL.

| Circuit information | | | Without clock gating | | | With clock gating | | | |
|---|---|---|---|---|---|---|---|---|---|
| Circuit | # of ct bufs | # of *XOR*s | Org (mA) | PA (mA) | Imp. | Gated (mA) | RePa (mA) | Incr Imp. | Total Imp. |
| *s13207* | 144 | 107 | 24.3 | 16.1 | 33.7% | 14.7 | 12.2 | 17.3% | 50.0% |
| *s15850* | 108 | 83 | 12.1 | 9.0 | 25.6% | 7.9 | 7.0 | 10.7% | 42.0% |
| *s35932* | 393 | 288 | 44.1 | 29.0 | 34.2% | 25.8 | 23.1 | 10.4% | 47.5% |
| *s38417* | 374 | 273 | 55.2 | 35.6 | 35.5% | 32.3 | 28.4 | 12.1% | 48.6% |
| *s38584* | 320 | 238 | 59.3 | 37.1 | 37.5% | 31.7 | 27.4 | 13.5% | 53.7% |
| *Average* | | | | | 33.3% | | | 12.8% | 48.4% |

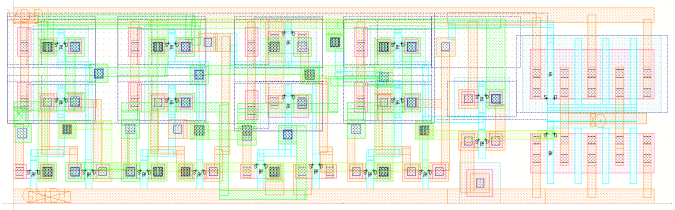


Fig. 6. The layout of a *DET-FF*.

for the clock tree before and after polarity assignment are presented in column "Org (mA)" and "PA (mA)", respectively. In Table V, the original clock tree "Org" is considered to be the clock tree with *XOR* gates inserted. Thus, the results demonstrate the efficacy of reconfigurable polarity assignment on this newly proposed tree built in `IC Compiler`. The peak current reduction is 33.3% on average which is summarized in column "Imp". The column "Gated (mA)" presents the peak current information on the polarity assigned *XOR* inserted clock trees when clock gating occurs. In this experiment, a 20% chance of clock gating is simulated. The column "RePa (mA)" presents the peak current value when polarity re-assignment is applied on the gated polarity assigned clock tree. An additional 12.8% improvement is observed by applying the reconfigurable polarity assignment, which adds up to an overall peak current reduction of 48.4%. Note that the improvement percentage may vary as the clock gating percentage changes.

To compare with the previous art, note that a polarity assignment algorithm using an optimal, dynamic programming-based method is proposed in [13]. The average level of peak current improvement reported in [13] is 35%. Thus, the level of peak current improvement (33.3%) of the adopted greedy algorithm when applied on the *XOR*-gate inserted tree is comparable to previous art when applied on the conventional buffer-based tree.

Similarly, the peak current information for the clock tree with *XOR* gates inserted at the non-sink level is presented in Table VI. In the experiments, the *XORX2* gates are inserted at the first non-sink level. The sink level buffers are chosen to be *BUFX2*. The clock gating percentage is set to 20% for consistency. By applying the proposed polarity assignment method, the peak current reduction is observed to be 33.9% on average. The reconfigurable polarity assignment permits an additional improvement of 12.9% after clock gating, totaling the improvement up to 51.1%. Note that in the experimental results, the peak current on the clock tree with *XOR* gates inserted at the sink level is less than the peak current on the clock tree with *XOR* gates inserted at the non-sink level. This is such as the peak current on *XOR* gate is less than the peak current on the clock buffers in the selected cell library ([16]).

### *C. Comparison to Conventional Polarity Assignment with Buffer/Inverter Replacement*

In Section VI-B, the efficacy of reconfigurable polarity assignment is demonstrated using the newly designed *XOR*-based tree as the comparison basis. It is shown that polarity assignment can improve the peak current from the basis design with *XOR*s by 33.3%. The impact of clock gating is also shown (12.8% additional) with the same basis for comparison.

Two other essential and enlightening comparisons are performed using the conventional buffered clock tree built in `IC Compiler` with and without clock gating as the comparison basis. Comparison against buffered clock tree without clock gating listed in Table VII demonstrates the effects of *XOR* insertion on the clock tree as it relates to polarity assignment. Comparison against buffered clock tree with clock gating listed in Table VIII demonstrates the efficacy of the proposed method when compared to the previous art. This is such as the previous art is to perform buffer/inverter replacement on a clock gated clock tree with iterative placement in the pre-silicon stage.

The peak current reduction effects without clock gating are compared in Table VII. It is observed that, despite the lack of clock gating, the peak current is reduced by a significant percentage. The peak current reduction effects for the conventional buffer/inverter replacement flow is 30.3%. The peak current value for the polarity assigned clock trees with *XOR* gates inserted at the sink level and non-sink level are reduced by 35.3% and 34.2%, respectively, compared to the peak current value on the conventional buffered clock tree without any polarity assignment. Compared to the conventional polarity assigned (buffer/inverter replaced) clock tree, the *XOR* based trees (without clock gating) has 7.4% and 5.4% less peak current after polarity assignment by inserting the *XOR* gates at the sink and non-sink level, respectively. This improvement is partially due to the low peak currents drawn by the *XOR* gates and partially due to different clock trees.

The peak current reduction effects with clock gating are summarized in Table VIII. In the conventional clock polarity assignment flow, the polarities are assigned pre-silicon. When clock gating occurs, the polarities of clock buffers are no longer optimal as discussed in Section II-B. In the *XOR* based clock polarity assignment flow, the polarities can be re-assigned when clock gating occurs. The peak current reduction

TABLE VI
RECONFIGURABLE POLARITY ASSIGNMENT WITH *XOR* GATES INSERTED AT THE NON-SINK LEVEL.

| Circuit information | | | | Without clock gating | | | With clock gating | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Circuit | # of ct bufs | # of sink bufs | # of *XOR*s | Org (mA) | PA (mA) | Imp. | Gated (mA) | RePa (mA) | Incr. Imp. | Total Imp. |
| *s13207* | 133 | 107 | 18 | 23.1 | 15.0 | 35.1% | 12.8 | 11.4 | 10.8% | 50.5% |
| *s15850* | 101 | 83 | 14 | 13.1 | 9.7 | 25.9% | 7.8 | 6.8 | 11.2% | 47.4% |
| *s35932* | 368 | 288 | 48 | 48.4 | 30.9 | 36.2% | 27.4 | 22.8 | 16.6% | 52.8% |
| *s38417* | 360 | 273 | 46 | 46.1 | 30.4 | 34.2% | 25.6 | 21.7 | 15.3% | 53.0% |
| *s38584* | 339 | 238 | 40 | 73.5 | 45.5 | 38.1% | 39.5 | 35.3 | 10.6% | 51.9% |
| *Average* | | | | | | 33.9% | | | 12.9% | 51.1% |

TABLE VII
PEAK CURRENT COMPARISON FOR CLOCK TREES WITH *XOR*S WITHOUT CLOCK GATING (WITHOUT POLARITY ASSIGNMENT).

| Circuit | Clock tree with bufs/invs | | | Clock tree with sink level *XOR* | | | Clock tree with non-sink level *XOR* | | |
|---|---|---|---|---|---|---|---|---|---|
| | Org. (mA) | PA (mA) | Impro. | Post PA (mA) | Over Org. | Over PA. | Post PA (mA) | Over Org. | Over PA. |
| *s13207* | 22.6 | 16.5 | 26.9% | 16.1 | 28.5% | 2.2% | 15.0 | 33.4% | 8.9% |
| *s15850* | 13.7 | 9.5 | 30.6% | 9.0 | 34.3% | 5.3% | 9.7 | 29.2% | -2.1% |
| *s35932* | 49.6 | 34.4 | 30.6% | 29.0 | 41.5% | 15.7% | 30.9 | 37.7% | 10.3% |
| *s38417* | 47.9 | 34.6 | 27.8% | 35.6 | 25.7% | -2.9% | 30.4 | 36.6% | 12.3% |
| *s38584* | 69.1 | 44.4 | 35.7% | 37.1 | 46.3% | 16.5% | 45.5 | 34.2% | -2.5% |
| *Average* | | | 30.3% | | 35.2% | 7.4% | | 34.2% | 5.4% |

TABLE VIII
PEAK CURRENT COMPARISON FOR CLOCK TREES WITH *XOR*S WITH CLOCK GATING.

| Circuit | Clock tree with bufs/invs | | Clock tree with sink level *XOR* | | Clock tree with non-sink level *XOR* | |
|---|---|---|---|---|---|---|
| | Org. (mA) | Gated (mA) | Gated+RePA (mA) | Over Gated | Gated+RePA (mA) | Over Gated |
| *s13207* | 22.6 | 14.6 | 12.2 | 16.4% | 11.4 | 21.4% |
| *s15850* | 13.7 | 7.8 | 7.0 | 10.2% | 6.8 | 11.8% |
| *s35932* | 49.6 | 29.9 | 23.1 | 22.8% | 22.8 | 23.8% |
| *s38417* | 47.9 | 32.2 | 28.4 | 12.0% | 21.7 | 32.7% |
| *s38584* | 69.1 | 41.5 | 27.4 | 34.0% | 35.3 | 15.0% |
| *Average* | | | | 19.1% | | 20.9% |

effects are more significant by reconfigurating the polarities. In experiments, after the reconfigurable polarity assignment at the clock gating events, the maximum peak currents are reduced by 19.1% and 20.9% with *XOR* gates inserted at the sink and non-sink level, respectively, than the clock gated buffer/inverter based polarity assigned circuit.

The skew and skew degradation of the buffer/inverter replacement based polarity assignment flow in previous works is compared against the proposed *XOR* based polarity assignment flow in Table IX. The polarity assignment degrades the clock skew for both conventional buffer/inverter trees and *XOR* gates inserted trees, despite at different rates. It is observed that unlike the conventional buffer/inverter replacement based polarity assignment, the skew degradation is very limited for the proposed *XOR* gate based clock tree synthesis scheme. The global skew of the clock tree synthesized with *BUFX2* buffers (using `IC Compiler`) is 55.0*ps*. As discussed in Section II, in the buffer/inverter based polarity assignment flow, an inverter with a similar delay while guaranteeing the slew rate and power constraints is used when performing the polarity assignment. In the *XOR* based polarity assignment flow, the *XOR* gate should have similar delay for positive and negative polarity, which is often the case in most cell libraries. Moreover, the *XOR* gates can be tuned to have the same delays for both the positive and negative polarity configurations.

The area and power information on the polarity assigned circuit using the buffer/inverter replacement based flow and the *XOR* based flow are compared in Table X. It is observed that the *XOR* based flow permits power savings compared to the buffer/inverter replacement based flow. This is such as under the same operating frequency, the frequency of the *XOR* based clock tree can be essentially halved due to the *DET-FF* triggering at both the rising and falling clock edges. Moreover, the *DET-FF* consumes less power than regular flip-flops as listed in Table IV.

## VII. CONCLUSIONS

This paper presents a novel polarity assignment flow which inserts *XOR* gates at either the sink or non-sink level of the clock tree based on the design requirement. Two polarity assignment methods are proposed to assign polarities for the clock trees with *XOR* gates inserted. The proposed clock tree synthesis scheme together with the polarity assignment methods is able to integrate the reconfigurability of polarity assignment into a design such that a further reduction in peak current is achieved when clock gating occurs. It is observed in the experimental results that the peak current on the clock tree with *XOR* gates inserted at the sink and non-sink level after the proposed polarity assignment methods are reduced by 33.3% and 33.9%, respectively. The peak current can be further reduced after polarity re-assignment when clock gating occurs by 12.8% and 12.9% on the clock tree with *XOR* gates inserted at the sink and non-sink level, respectively. The total power consumption is reduced as well by 23.8% and 25.1% with *XOR* gates inserted at the sink and non-sink level, respectively.

TABLE IX
SKEW DEGRADATION FOR DIFFERENT POLARITY ASSIGNMENT METHODS.

| Circuit | Clock tree with bufs/invs | | | Clock tree with sink level *XOR* | | | Clock tree with non-sink level *XOR* | | |
|---|---|---|---|---|---|---|---|---|---|
| | Pre PA (ps) | Post PA (ps) | Incr. (ps) | Pre PA (ps) | Post PA (ps) | Incr. (ps) | Pre PA (ps) | Post PA (ps) | Incr. (ps) |
| *s13207* | 47.3 | 68.6 | 21.3 | 56.2 | 68.7 | 12.5 | 37.5 | 41.0 | 3.5 |
| *s15850* | 43.7 | 62.0 | 18.3 | 34.8 | 36.6 | 1.8 | 32.2 | 33.4 | 1.2 |
| *s35932* | 57.5 | 74.6 | 17.1 | 48.6 | 58.6 | 10.0 | 48.2 | 48.8 | 0.6 |
| *s38417* | 55.7 | 75.7 | 20.0 | 57.2 | 67.0 | 9.8 | 38.4 | 41.4 | 3.0 |
| *s38584* | 70.6 | 90.8 | 20.2 | 61.8 | 71.5 | 9.7 | 69.0 | 69.5 | 0.5 |
| *Average* | 55.0 | 74.3 | 19.3 | 51.7 | 60.5 | 8.8 | 45.1 | 46.8 | 1.7 |

TABLE X
AREA INCREASE AND POWER SAVING INFORMATION.

| Circuit | Buf/inv | | Sink level *XOR* insertion | | | | Non-sink level *XOR* insertion | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Area ($\mu m^2$) | Power ($mW$) | Area ($\mu m^2$) | Incr. | Power ($mW$) | Savings | Area ($\mu m^2$) | Incr. | Power ($mW$) | Savings |
| *s13207* | 36660 | 16.2 | 39500 | 7.7% | 12.0 | 25.5% | 39038 | 6.5% | 11.6 | 28.0% |
| *s15850* | 39820 | 12.2 | 41936 | 5.3% | 9.3 | 23.0% | 41597 | 4.5% | 9.1 | 25.2% |
| *s35932* | 86821 | 51.6 | 94685 | 9.1% | 38.5 | 25.4% | 93517 | 7.7% | 38.4 | 25.6% |
| *s38417* | 85783 | 55.3 | 93097 | 8.5% | 42.6 | 23.0% | 91881 | 7.1% | 41.9 | 24.4% |
| *s38584* | 136496 | 55.5 | 142912 | 4.7% | 43.1 | 22.3% | 141921 | 4.0% | 43.0 | 22.4% |
| *Average* | | | | 7.1% | | 23.8% | | 5.9% | | 25.1% |

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# A Shift-Register-Based QCA Memory Architecture

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A quantum-dot cellular automata (QCA) design of an $nxm$-bit, shift-register-based memory architecture is presented. The architecture maintains data at a stable conformation, which is contrary to traditional data in-motion concept for QCA architectures. The memory architecture is based on an existing dual-phase-synchronized, line-based, one-bit QCA memory cell building block that provides size and latency improvements over other known one-bit memory cells through its novel clocking scheme. Read/write latencies up to ∼2X lower than the existing tile-based architecture with three-phase, line-based memory cells are obtained. Simulations with `QCADesigner` and `HDLQ` are performed on a sample $4x8$ bit memory architecture implementation.

Categories and Subject Descriptors: B.6.1 [**Logic Design**]: Design styles—*Cellular array and automata*

General Terms: Algorithms, Experimentation, Theory

Additional Key Words and Phrases: Quantum-dot cellular automata, clocking, memory design

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4

## 1. INTRODUCTION

Quantum-dot cellular automata (QCA) is a potentially promising technology as an alternative to complementary-metal-oxide semiconductor (CMOS) technology for nanoscale device implementations. The implementation of the QCA technology has been demonstrated with metal-dot QCA devices at very low (e.g., cryogenic) temperatures [Snider et al. 1999]. Circuit structures such as the majority gate, binary wires and fanouts have been fabricated with metal-QCA dots [Orlov et al. 1999; Amlani 1999; Kummamuru et al. 2002; Yadavalli

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et al. 2005]. Recently, research in molecular QCA implementations have been emerging through advances in DNA tiling and molecular self-assembly [Hu et al. 2005]. Molecular QCA technology is projected to operate at the room temperature with much higher functional densities [Hennessy and Lent 2001; Lent and Isaksen 2003; Amlani et al. 2003; Lent et al. 2003; Huang et al. 2005].

The manufacturing and assembly of quantum-dot devices from a physics and chemistry point of view is the pillar to the emergence of QCA technology as a viable alternative to CMOS nanoscale device implementations. While some QCA research has to be performed specific to the metallic or molecular QCA manufacturing data (such as power dissipation research), general *nanoarchitecture design* studies can be performed by modeling QCA-dots at a higher level of abstraction, relatively independent of the manufacturing technology. In the presented work, one such study is performed, which involves the *automata* design of a novel QCA-based memory architecture using the logical representation of quantum dots. Such logical representation of quantum dots is advantageous in terms of characterizing QCA nanoarchitectures independent of the manufacturing technology, which enables a systematic analysis.

Memory design in QCA logic has been a challenge[1] due to the locality of computation and constant propagation of data in cellular automata. Alternative memory cell and architecture implementations have been proposed (reviewed in Section 2), which provide different performance as well as operational characteristics. The research presented in this article is performed on the following structures:

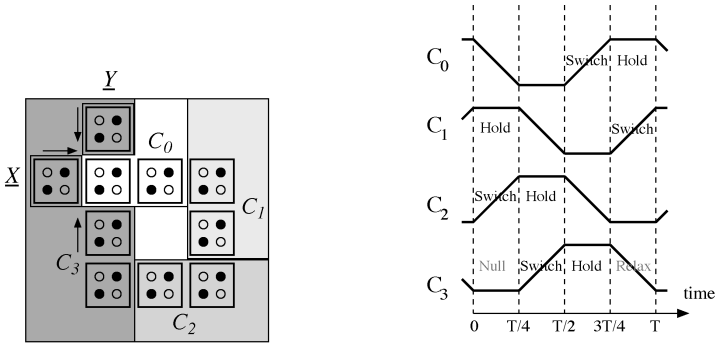
—Two types of line-topology-based memory cells: the three-phase memory cell presented in Vankamamidi et al. [2005a] and the dual-phase memory cell presented in Taskin and Hong [2006],

—Two memory architectures: the tile-based architecture presented in Vankamamidi et al. [2005b] and Ottavi et al. [2005] and the novel shift-register-based architecture presented in this article.

The two types of line-based memory cells are similar in topology and design, and differ from other memory and logic cells in promoting the use of alternative clocking schemes in addition to the four-phase clocking scheme conventionally used in QCA operation. Thanks to the alternative clocking schemes, significant performance improvements in read/write latency (in the number of clock cycles) and cell area (in the number of clocking zones) are achievable. For instance, a tile-based *nxm* bit memory architecture design is presented in Vankamamidi et al. [2005b] and Ottavi et al. [2005] that uses the three-phase line-based memory cell presented in Vankamamidi et al. [2005a] with the unconventional three phase clocking scheme. This tile-based memory architecture provides conventional memory operation with a denser bit-storage area than previously offered QCA memory architectures.

The novelty of this paper is a shift-register-based, *nxm* memory architecture that utilizes dual-phase, line-based memory cell presented in Taskin and Hong

[1]This challenge is pronounced from the suggested *automata design* point of view. Memory design is currently also a challenge from a manufacturing point of view, as is any other complex QCA system.




(a) QCA implementation where X and Y are control/data signals and the data is stored traveling around the feedback loop. Clock zones are color coded.

(b) Traditional four-phase clocking strategy.

Fig. 1. Four-phase, feedback-topology memory cell.

[2006] with the unconventional dual-phase clocking scheme. Similar to the tile-based architecture, the design density is much improved over previous QCA memory architectures. Furthermore, read/write latency of the proposed shift-register architecture is up to ∼2X lower than the previously proposed tile-based QCA memory architecture.

The rest of this article is organized as follows. In Section 2, a brief survey of previous research on QCA memory design is presented. In Section 3, the three-phase and dual-phase line based memory cells and the tile-based architecture for the three-phase memory cells are reviewed. In Section 4, the proposed shift-register based memory architecture for the dual-phase line-based memory is presented. In Section 5, simulation results using the popular QCA design simulator `QCADesigner` and the design language `HDLQ` are presented. In Section 6, performance characteristics of the presented memory architecture are analyzed. Finally, conclusions are offered in Section 7.

## 2. QCA MEMORY DESIGN OVERVIEW

Previously offered QCA memory architectures can be categorized as serial-access [Berzon and Fountain 1999; Frost et al. 2002, 2003] and parallel-access memories [Walus et al. 2003; Ottavi et al. 2005; Vankamamidi et al. 2005a]. A serial-access QCA memory has been presented as part of the SQUARES formalism in Berzon and Fountain [1999]. In Berzon and Fountain [1999], data storage is performed through a feedback topology cell, which is illustrated in Figure 1. The feedback provides the typical *unidirectional* path for propagation of the stored data value over the four consecutive clocking zones of the traditional QCA clocking strategy.

The read/write circuitry can be quite complex for serial access memories. A particular type of serial-access memory, the H-memory presented in Frost et al. [2002], incorporates thread bouncing computation method [Frost et al. 2003] in order to reduce this complexity. H-memory provides unique operation and

computation practices, within which packets of instructions and data are sent through the H-tree architecture for local computations.

The parallel access QCA memory architecture presented in Walus et al. [2003] emulates the CMOS RAM design by using the QCA feedback topology memory cell (Figure 1) for data storage. This simple design operates with the four-phase clocking scheme, not requiring any additional CMOS clock generators. However, complex clocking zones (not row or column stackable) are necessary due to the clock zone requirements of the feedback-topology memory cell. Additionally, synchronization with the traditional four-phase clocking scheme mandates a *unidirectional* data flow, limiting the exploration of performance through the *bidirectional* data flow advocated in the design of the line-based memory cells.

## 3. LINE-BASED MEMORY CELLS

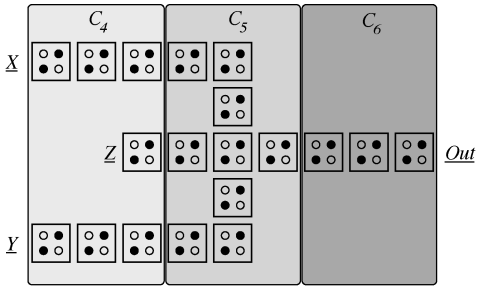
Line-based memory cells are built on the premise of bidirectional data flow. Note that, bidirectional data flow is not possible with the conventional four-phase clocking scheme. By defining additional clock phases, however, some combination (two or more) of clock zones can create flows in one direction at certain durations of their periodic clocking cycle whereas the direction can be reversed at other durations. In other words, two adjacent clock zones that are in hold and switch phases (respectively) at one time can later be observed in the switch and hold phases, respectively.

The two types of line-based memory, the three-phase and the dual-phase memory, are reviewed in Sections 3.1 and 3.2, respectively.

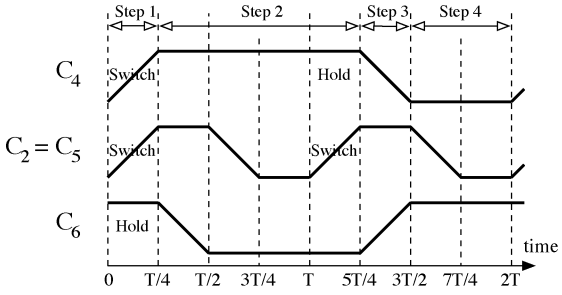
### 3.1 Three-Phase Line-Based Memory

The three-phase, line-based memory cell [Vankamamidi et al. 2005a], shown in Figure 2, is the first study to exploit non-standard clocking strategies in QCA operation. This cell consists of three clock zones $C_4$, $C_5$, $C_6$, where the four conventional clocking zones in the *rest* of the circuit are labeled $C_0$, $C_1$, $C_2$, $C_3$. Clock phase $C_5$ is identical to one of the clock phases of the four-phase clocking scheme, namely $C_2$ in Figure 1(b). Thus, unlike $C_4$ and $C_6$, the clock phase $C_5$ does not require an additional clock source. Consequently, the three-phase clocking scheme requires two additional clock generator circuits. Clock signals to zones 4, 5, and 6 (synchronized by phases $C_4$, $C_2 = C_5$, and $C_6$, respectively) all follow the hold-release-null-switch cycle. The clock phase of zone 5 is specially designed such that when either zones 4 or 6 is in the hold phase, zone 5 is in the switch phase, enabling bidirectional data flow—and storage—on the memory *line* between Z and Out. The read/write latency of the three-phase cell is equal to the period $2T$ of the synchronization scheme (where $T$ is the period of the conventional four-phase clocking scheme).

Tile-based memory architecture, shown in Figure 3, is proposed in Vankamamidi et al. [2005b] and Ottavi et al. [2005] as an architecture that employs the three-phase, line-based memory cell. This architecture is composed of one input tile (on the left), three internal tiles (in the middle), and one output tile (on the right). When tiles are placed adjacently, a major loop for data




(a) QCA implementation where X and Y are control/data signals and data is stored traveling along the line Z–Out.




(b) Three-phase clocking scheme for the line memory.

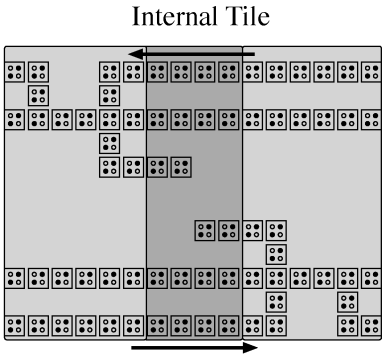
Fig. 2. Line-based memory with three-phase clocking.

propagation is constructed. Two bits of data are stored in each tile, one on the upper, one on the lower propagation path. In each internal tile, the three-phase, line-based memory cell shown in Vankamamidi et al. [2005a] is used as the bit storage mechanism.

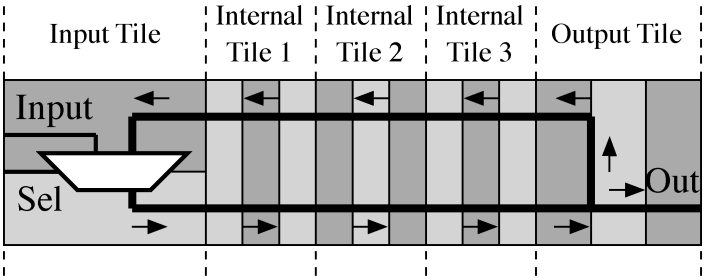
In an $m$-bit row of the tile-based architecture memory, data bits are stored circulating on a closed feedback loop as shown for $m = 3$ in Figure 3(b). Thus, when data needs to be read or written, an external counter of $log\ m$ bits is used to synchronize the writing/reading head with the requested data bit location (discussed but not implemented in Vankamamidi et al. [2005b] and Ottavi et al. [2005]). Such operation leads to variable read/write latencies, as initiating a memory access operation may take anywhere between 0 to $m-1$ cycles, followed by $m$ cycles for the read/write operation totaling up to a latency between $m$ and $2m - 1$.

### 3.2 Dual-Phase Line-Based Memory

An alternative implementation of the line-based memory with dual-phase synchronization, shown in Figure 4, is presented in Taskin and Hong [2006]. This cell consists of two clocking zones $C_6$, $C_7$ and consequently requires two clock phases (in addition to the four clock phases $C_0$, $C_1$, $C_2$, $C_3$ in the rest of the circuit). The two clock phases, $C_7$ and $C_8$, are generated by a single clock generator and a phase shifter. In operation, Zone 7 switches when zone 8 is holding (step 1)




(a) Internal tile storing two bits propagating in opposite directions




(b) Illustration of a memory with three internal tiles, an input tile and an output tile.

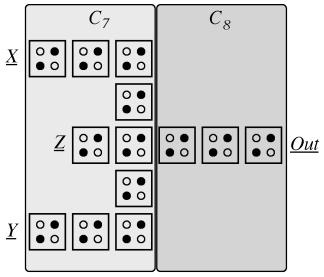
Fig. 3. Tile-based memory architecture.

and Zone 8 switches when zone 7 is holding (step 2), creating the bidirectional data flow. Consequently, data written to the cell moves back and forward on the memory *line* (between Z and Out, bidirectionally), constituting the storage mechanism. The read/write latency of the three-phase cell is equal to the period $3T/2$ of the synchronization scheme (where $T$ is the period of the conventional four-phase clocking scheme). In order to ensure proper synchronization with the surrounding circuitry (which is typically synchronized with the traditional four-phase clocking scheme with a clock period of $T$), the $3T/2$ period of two-phase memory is extended to $2T$. Under such a synchronization scheme, the write latency is extended to $2T$ (to be identical to three-phase cell), whereas the read latency is improved to $T$, leading to 2X faster read operations than the three-phase cell. The differences between the dual and three-phase line-based memory cells are categorized in Table I.

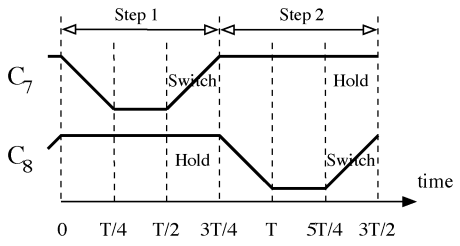
In order to observe the operational characteristics of the dual-phase line-based memory cell in a *multirow* (stacked) architecture, a shift-register-based memory architecture is proposed.

## 4. SHIFT-REGISTER-BASED MEMORY ARCHITECTURE

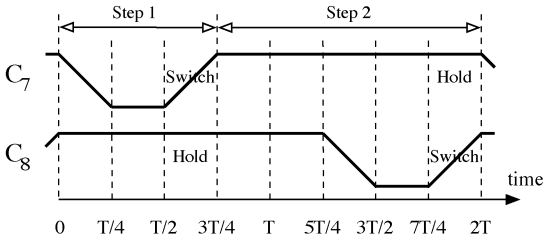
The building block of the presented shift-register-based memory architecture is shown in Figure 5. The data storage in the building block is established with




(a) QCA implementation where X and Y are control/data signals and data is stored traveling along the line Z–Out.




(b) Shortest dual-phase clocking scheme for the line memory.




(c) Proposed dual-phase clocking scheme for the line memory with $2T$ period, functionally equivalent synchronization with Fig. 4(b).

Fig. 4. Dual-phase line-based memory cell.

Table I. Design and Performance Comparison of the Three-Phase and Dual-Phase Line-Based Memory Cells

| | Three-phase | Dual-phase |
|---|---|---|
| Additional clock phases | 3 | 2 |
| CMOS clock generators | 2 | 1 |
| Clock zones per memory cell | 3 | 2 |
| Read latency | $2T$ | $T$ |
| Write latency | $2T$ | $2T$ |

the dual-phase memory cell and the read/write control is maintained through the AND and NOR gates. The memory architecture is built similar to a shift-register, where data is stored within the building blocks (e.g., register equivalents) and the blocks are replicated for a multibit storage mechanism (not shown in Figure 5).

The CMOS equivalent of building block for the shift-register-based memory architecture is shown in Figure 6. In brief, the dual-phase, line-based memory cell maintains data by applying opposite values to the two inputs ($\underline{X} \neq \underline{Y}$, also see Figure 4). In order to write data $D$ into the cell, identical values are applied to the two inputs ($\underline{X} = \underline{Y} = D$). A read/write signal $R/W$ is defined for each row that permits the read/write operations on the $m$-bit-long, shift-register structure (of an $nxm$ memory). The read/write control circuitry (AND and NOR gates) drives

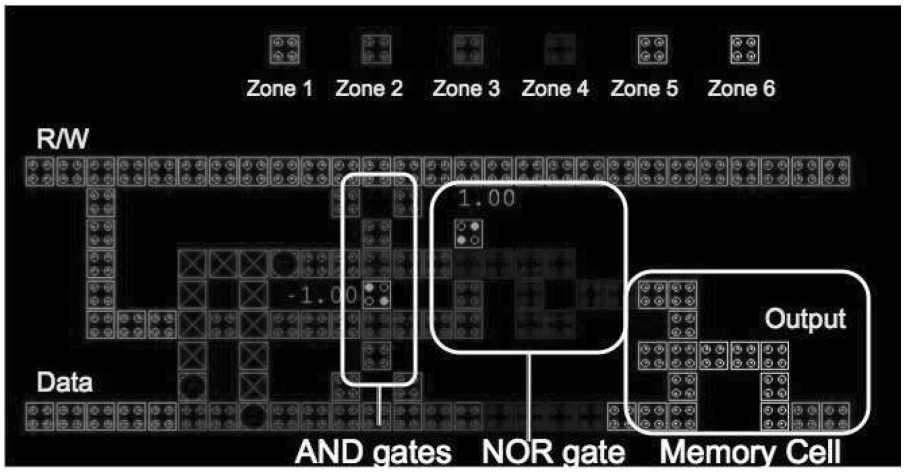



Fig. 5. Template building block for the shift-register-based memory architecture: the line-based memory cell with control circuitry.

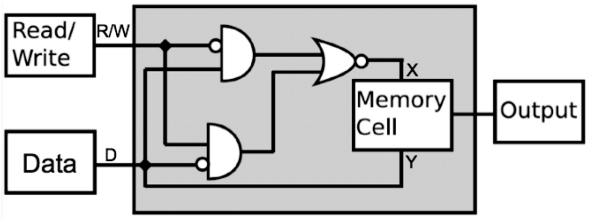



Fig. 6. CMOS equivalent of the building block.

the X and Y inputs, based on the data signal $D$ and a read/write signal $R/W$:

$$X = \overline{((\overline{R/W})D + (R/W)\overline{D})} = (R/W) \odot D, \tag{1}$$

$$Y = D. \tag{2}$$

When the Read/Write $(R/W)$ signal is asserted, new data is written in, while the previously stored data is read:

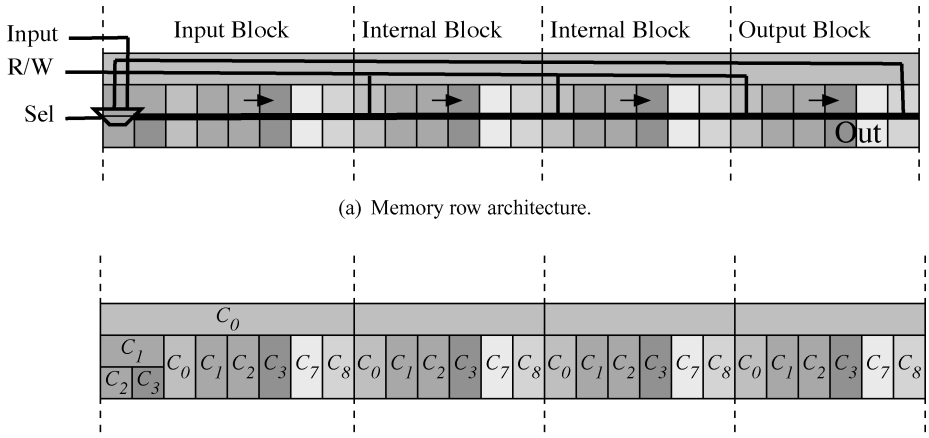
$$X = 1 \odot D = D = Y \quad \Rightarrow \quad (X = Y = D, \text{write operation}). \tag{3}$$

The rest of the time (when $R/W = 0$), the data remains stored:

$$X = 0 \odot D = \overline{D} \neq Y \quad \Rightarrow \quad (X \neq Y = D, \text{maintain operation}). \tag{4}$$

### 4.1 Architecture Design

Within the shift-register-based architecture, data is maintained in a static arrangement with serial input and output (due to the shift-register structure). Shift-registers are most suitable for first-in-first-out (FIFO) type operations but also can be used as a typical memory with a feedback wire between the serial output and the serial input. In the proposed QCA implementation, such a feedback QCA wire is used to complete the architecture design for a typical




(a) Memory row architecture.

(b) Clock zone alignments.

Fig. 7. Illustration of a shift-register-based memory with two internal tiles, an input tile and an output tile.

memory. To this end, a QCA routing line is drawn from the output of the wordline to the input of the wordline as shown in Figure 7. The template building block shown in Figure 5 is modified into input, internal and output blocks (discussed next in Section 4.2), permitting the shift-register architecture depicted in Figure 7. The data value that is stored in the shift register architecture is serially read from the `Out` terminal, while simultaneously being fed back into the multiplexer for data input to the shift register. If the shift register data needs to be stored back into the memory after a read operation, the control signal `Sel` is asserted to multiplex the feedback data signal into the shift register memory. For a destructive read or for a typical FIFO operation, the `Sel` signal is not asserted, multiplexing the external input data signal `Input` into the shift register memory.

The data feedback line is drawn along the length of the memory wordline in the same clock zone as the read/write enable signal. The area impact of this feedback line is minimal as the clock zone is shared with the read/write line. Also of importance is the area and latency impact of the three additional clock zones $C_1$, $C_2$, and $C_3$ defined on the input side of the shift-register architecture. These clock zones are stacked together, each with half the height of a typical clock zone. The multiplexer gate to select between the previously stored data and external data input is implemented within these three (additional) conventional clock zones.

As illustrated in Figure 7, the proposed shift-register QCA memory features parallel, regular layout of clock zones. The orientation and type of clock zones are clearly marked in Figure 7(b). It should be noted, that, the regularity of the clock zones can further be improved by sacrificing the latency of operation, where necessary. For instance, the multiplexer on the input side can be implemented in perfectly parallel clocking zones [Vankamamidi et al. 2006], as opposed to the relatively regular and compact clock zones used in this work.

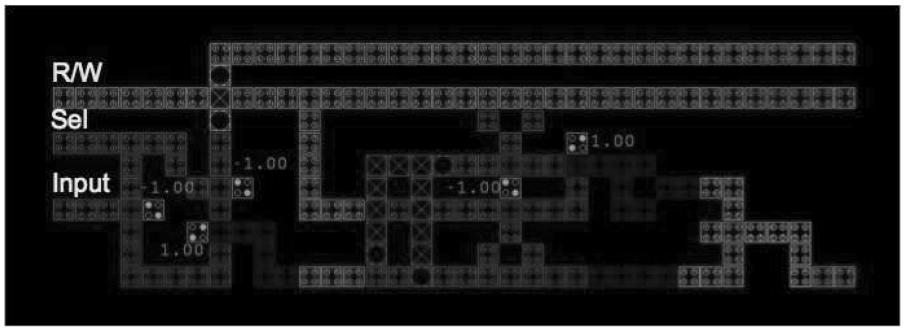



Fig. 8. Input block for the shift-register-based memory architecture.

A sample QCA layout of the proposed architecture, slightly modified to adhere to the simulation limitations of the experimental verification tool, is presented next.

### 4.2 QCA Architecture Layout

As mentioned above, the building block of the shift-register-based QCA memory shown in Figure 5 is redesigned into three specialized categories: the *input* block (Figure 8), the *internal* block (Figure 9) and the *output* block (Figure 10). This specialization is necessary to draw the feedback line connecting the `Out` terminal of the n-bit shift register to the multiplexed `Input` terminal at the input block as shown in Figure 7. The internal block is similar to the building block in Figure 5 except for the QCA line in the same zone and placed parallel to the read/write signal for output feedback. The output block has a short read/write signal and the output terminal fanouts to the feedback line propagating backwards along the direction of the shift-register architecture. The input block has the most significant changes to encapsulate the control features for the rewriting operation. In particular, the input block has three additional clock zones and three majority gates formed into a multiplexer. As illustrated in Figure 7 and visible in Figure 8, the three additional clock zones have approximately half the height of original clock zones and have comparable widths. The rewrite operation is performed with the area overheads of three clock zones for the control circuitry (e.g., for any $n$-bit shift register) and the latency overhead of one clock cycle ($T$) induced by the propagation of the feedback data.

The QCA layout of a demonstrative $4x8$ shift-register-based memory architecture (using the building blocks in Figures 8, 9, and 10) is shown in Figure 11. Note that the building blocks are stacked in a row and the clocking zones between building blocks are meshed seamlessly for uninterrupted operation and dense implementation.[2] The regularity of the clock zones in the overall architecture is visible from the color coding in Figure 11, which adheres to the

[2]Note that in Figure 11, additional spaces are inserted between building blocks as well as between the read/write signal line and the rest of the building block for better visibility; denser implementations are possible.

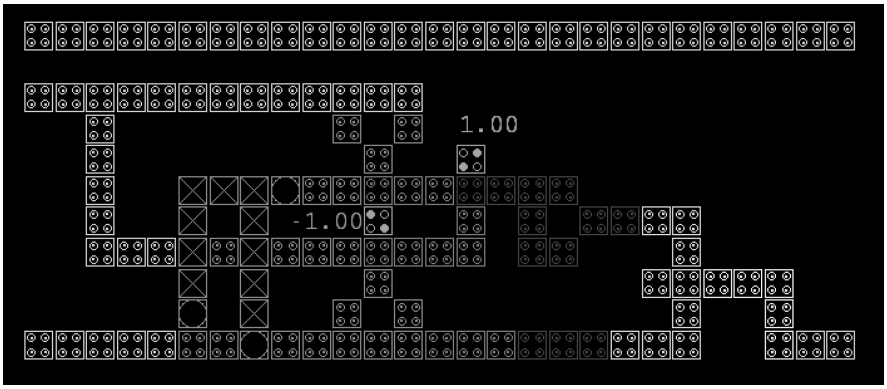



Fig. 9. Internal block for the shift-register-based memory architecture.

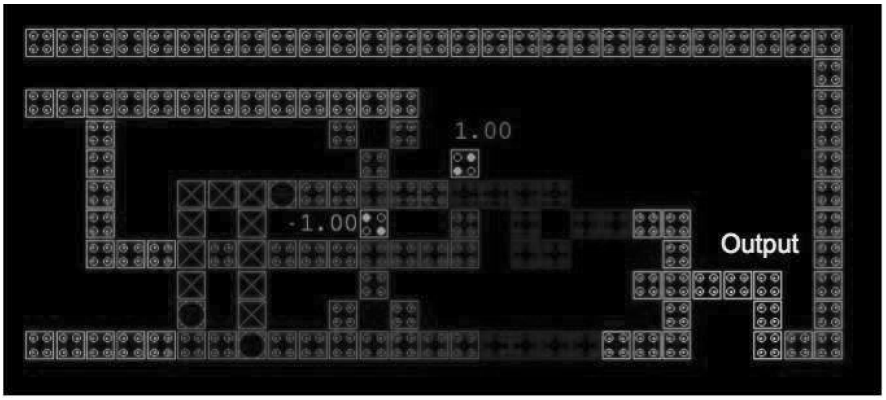



Fig. 10. Output block for the shift-register-based memory architecture.

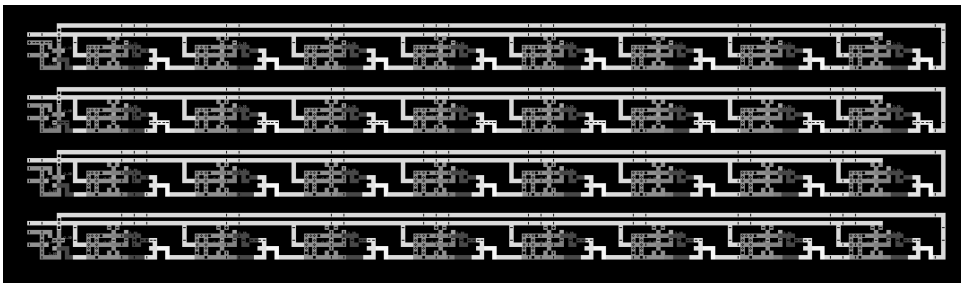


Fig. 11. QCA diagram of a sample $nxm$ memory architecture, where $n = 4$ and $m = 8$.

configuration depicted in Figure 7. Such regularity of clock zones is important for CMOS clock wiring layout within the QCA manufacturing process.

In Figure 11, the $R/W$ signal (and data feedback signal) is routed in an exclusive horizontal clocking zone for simultaneous delivery to building blocks. Thus, the number of QCA cells in a line (wire) that can be placed in a single clock zone dictates the physical limitation of operation for the displayed memory

architecture. Alternative read/write (or row select) signal delivery methods, such as those analogous to traditional CMOS methods of metal bypass, multiple drivers, and hierarchical word-line selection schemes [Rabaey et al. 2003] can easily be adopted for longer wordsize implementations using this architecture.

## 5. SIMULATIONS AND ANALYSIS

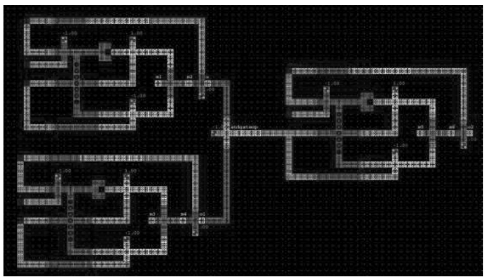
Two different simulators, QCADesigner[3] [Walus et al. 2004] and HDLQ [Ottavi et al. 2006] with Modelsim, are used to verify the functionality of the presented shift-register-based memory architecture. QCADesigner is used to simulate small, simple building blocks with higher accuracy, while HDLQ is used for the verification of the larger-scale system avoiding the slow execution speeds of QCADesigner-only simulation.

QCADesigner is an open source software which has been widely used by QCA researchers. However, QCADesigner simulator (v2.0.3) only supports the conventional four-phase clocking scheme for QCA circuits. In order to simulate QCA architectures with alternative clocking schemes, such as the three-phase, line-based memory in Vankamamidi et al. [2005a] or the dual-phase, line-based memory architectures in Taskin and Hong [2006], modifications must be performed to the design *or* to the simulator. The former method is followed in Vankamamidi et al. [2005a], where a time-to-space transformation procedure is devised. The latter method is followed in Taskin and Hong [2006], where the software is modified to accommodate advanced clocking schemes. In this article, the modified software in Taskin and Hong [2006] is used.

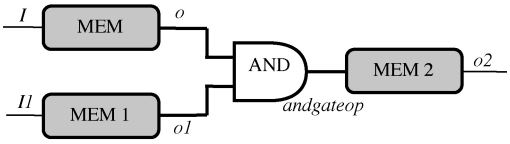
HDLQ [Ottavi et al. 2006] is a design language tool for the simulation of QCA architectures written in Verilog Hardware Description Language (HDL) style. Instead of modeling QCA at the physical level with quantum-mechanical computations, it models QCA circuits by assuming an ideal logical model of QCA operation. Such a treatment is especially valuable for fast prototyping of complex QCA circuitry. In HDLQ, a circuit is described as a series of interconnected modules, where each module is a common element of a QCA circuit. For instance, elements modeling a QCA wire, fanout, inverter, and majority voter are provided in the library. Adjacent elements of a QCA circuit have the inputs and outputs wired in Verilog representation. HDLQ also allows for bidirectionality of QCA devices, which is essential to the presented shift register design.

In the first step of design verification, the line-based memory cell is simulated using QCADesigner. For demonstrative purposes, the simple circuit shown in Figure 12 is constructed. In this circuit, data is read from two QCA memory cells (*MEM* and *MEM1*), logical AND operation is performed on this data, and the result is stored in the QCA memory cell *MEM2*. In Figure 12(a), three instances of the proposed memory cell are shown, *MEM* and *MEM1* on the left and *MEM2* on the right. The simulations results, including the simulation waveforms for the nodes labeled in Figure 12(b), are shown in Figure 13. Inputs 1110 and 1011 are applied to data input terminals $I$ and $I1$, respectively. Simulation depicts the values of internal nodes and the output node $o2$ of the AND operation on these values. For instance, the output of 1 is observed for the

[3]http://www.qcadesigner.ca.



(a) Layout view.




(b) Schematic view.

Fig. 12. Experimental circuit for the dual phase line-based memory cell.

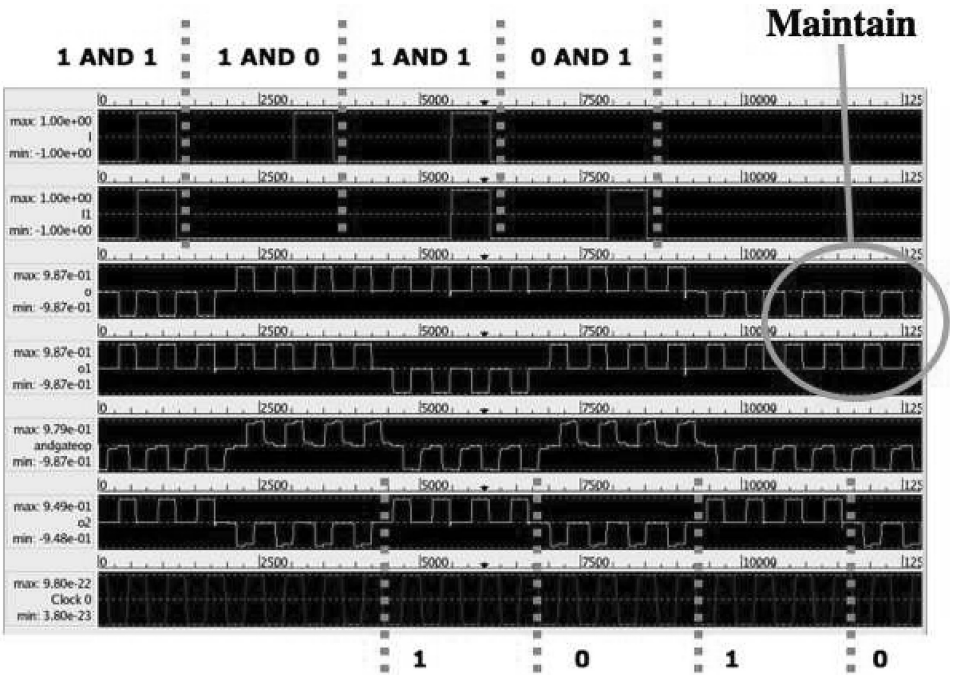



Fig. 13. Simulation waveforms obtained with `QCADesigner` (modified to accommodate advanced clocking) for the circuit shown in Figure 12.

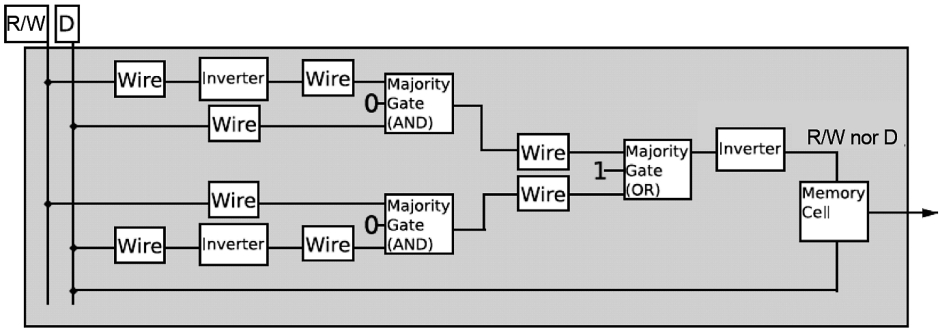



Fig. 14. HDLQ block diagram of presented memory cell shown in Figure 5.

AND operation of values 1 and 1 stored in *MEM* and *MEM1* cells, respectively ($1\ AND\ 1 = 1$). The simulations waveforms $o$ and $o1$ depict the stored values in *MEM* and *MEM1* cells, respectively. For the first set of data, $o1$ and $o2$ are 1 and 1, respectively. The $and\,gateop$ internal node depicts the computed AND value, for example, 1 for the first set of data ($1\ AND\ 1 = 1$). This value is written into *MEM3* cell and shown at the output terminal $o2$ after the write latency of that memory cell. Similar operations are observed for input sets of 1/0 ($1\ AND\ 0 = 0$), 1/1 and 0/1 ($0\ AND\ 1 = 0$). On the simulation waveform in Figure 13, read and write operations from and to memory cells *MEM*, *MEM1*, and *MEM2* are illustrated multiple times. Correct outputs are observed on all input patterns. In the simulation, maintain operation is depicted on internal outputs $o$ ($o1$) for memory cell *MEM* (*MEM1*) on input value 0 (1) during the last $T/4$ of simulation waveform. In conclusion, these QCADesigner simulations confirm the proposed operation of the dual-phase, line-based memory cells.

Next, an HDLQ module is developed for the building block, as shown in Figure 14. This model emulates the functionality of the single-bit memory cell with Verilog code in the same style as the preexisting HDLQ modules. Using this macromodel for the line-based memory cell (whose operation is proved with the QCAdesigner simulations mentioned above), experiments at the system level are performed in order to verify the functionality and characterize the performance of the proposed shift-register based memory *architecture*. The schematic for the *nxm* architecture is shown in Figure 15. Note that this HDLQ module excludes the feedback wire from the last bit to the first bit. Nonetheless, the model captures the important shifting and storage capabilities of the architecture and an extension to model the feedback wire is trivial. HDLQ simulation results, shown in Figure 16, consist of four rows of the shift-register architecture. The signals $A1$ and $A2$ serve as address signals. The testbench demonstrates the read, maintain, and write operations. Initially, the memory is reset by writing value 0 to each bit (serially). Then each of the four memory rows has a different pattern written to it. The staircase-pattern-waveforms demonstrating the shift operation are visible upon close inspection in Figure 16. Because each row is essentially a shift register, new data must be supplied as the current data is output. In experiments, zeros are written to the memory for this purpose. The memory holds its value for a time, then each row's data is output.

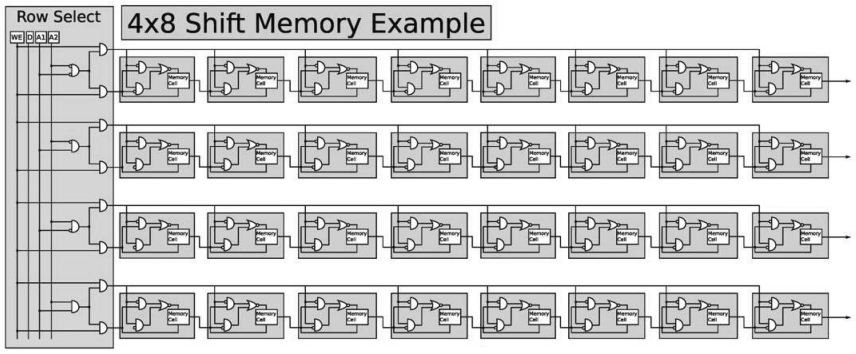



Fig. 15. Block diagram of a sample $nxm$ memory architecture, where $n = 4$ and $m = 8$.

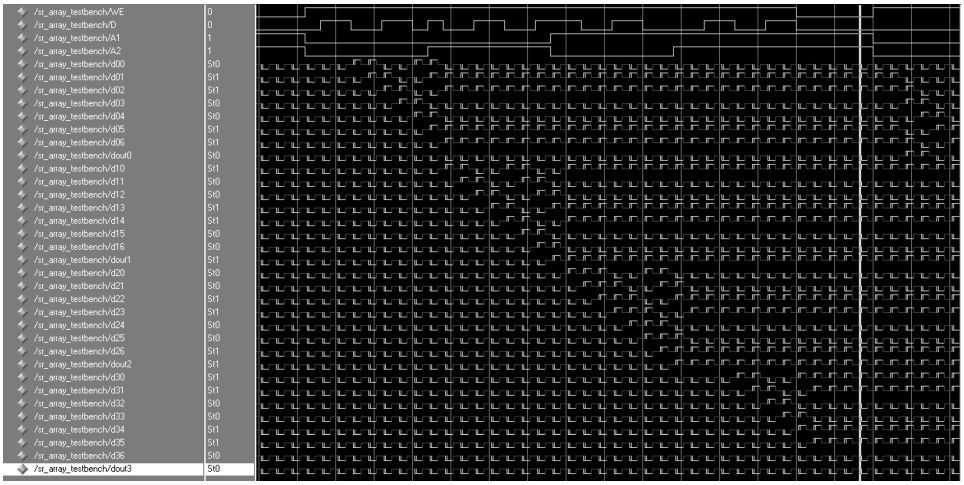



Fig. 16. `ModelSim` waveform from `HDLQ` description of the $4x8$ memory. All bits are initialized to value 0 and then overwritten.

For better visualization of the write process, memory operation on row 3 is magnified in Figure 17, onto which a data pattern 11001100 is written. In Figure 17, the top four signals are the control signals. The signal $R/W$ is the read/write signal, $D$ is the data being written, and the signals $A1$ and $A2$ are the row address bits. The rest of the signals, from $d30$ to $dout3$ show the value stored at each memory cell. The cell labeled $d30$ is the leftmost cell and the *dout3* is the rightmost cell. The staircase pattern, due to shifting, is also visible upon close inspection.

For clarity, it is important to emphasize that the simulation times shown `HDLQ` simulations do not represent the projected implementation performance of the QCA system; it is used to count the number of cycles in operation. Actual operation times will depend on QCA manufacturing technique and the clock speed.

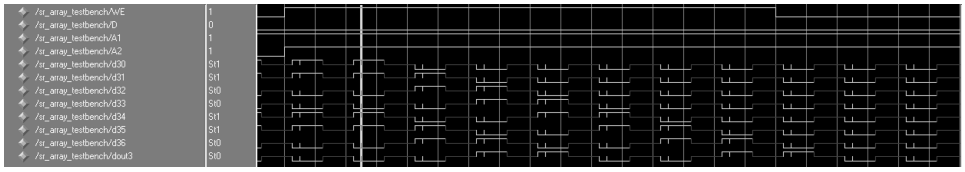



Fig. 17. Data pattern 11001100 from row 3 of the four memory rows read in parallel in consequent cycles based on shift-register operation.

## 6. COMPARISONS

The read and write latencies of the shift register architecture are $m$ cycles for an $m$-bit row, as bits are read and written serially (and sequentially). As detailed in Section 3.1, the read/write latency of the tile-based architecture is a variable between $m$ and $2m - 1$ cycles due to the circulation of data. Variable read/write latencies might cause hardship in system operation, so a constant read/write latency of $2m - 1$ cycles can be selected, which is the latency for the worst-case operation (first-bit-to-read is at the internal tile adjacent to the output tile). In comparison, the read/write latency of the QCA RAM architecture is at least proportional to wordsize (latency changes based on the address decoder implementations) and the read/write latency of H-memory is a constant dependent on the size of the binary tree (H-tree), thus cannot be directly compared.

Compared with the H-memory proposed in Frost et al. [2002] and RAM-based QCA memory proposed in Walus et al. [2003], in which conventional four-phase clocking and the feedback-topology memory cell are used, the proposed shift-register memory architecture permits denser implementations. For instance, the number of clocking zones in the H-memory depends on the wordsize and the number of words, while the number of clocking zones in line-based memories depend only on wordsize. For tile-based and shift-register-based architectures (with line-based memory cells), QCA implementations are much denser. Amongst these two architectures, the tile-based architecture is denser than the proposed shift-register-based architecture. An internal tile occupies three clocking zones and holds two bits of data, while a shift register internal block shown in Figure 9 occupies six clocking zones and holds a single bit of data. The low utilization of area in the tiles [empty space between top and bottom rows, see Figure 3(a)] slightly degrades the density advantage. Overall, considering such $\sim$2X area disadvantage and the 2X read/write latency advantage, the proposed shift-register architecture provides for a less dense but faster memory implementation compared to the tile-based memory architecture. It is important to note that the tile-based architecture requires an additional circuitry (a counter) as part of the read/write control mechanism. This external circuitry is not included in Vankamamidi et al. [2005b] and Ottavi et al. [2005], thus excluded from the comparisons presented in this paper as noted in Table II.

A categorized comparison of the two QCA memory architectures is presented in Table II. In brief, the advantages of the *dual-phase* line-based memory cells (integral part of the building blocks) presented in Table I are observed for the presented shift-register based architecture, as well, except for the area advantage. The area disadvantage is due to the inclusion of clock zones for the

Table II. Comparison of the Tile-Based Architecture and the Shift-Register-Based Architecture

| | Tile-based[Vankamamidi et al. 2005b] | Shift-register-based |
|---|---|---|
| Building blocks | Tiles | Shift register cell |
| Clock zones per cell | 3 | 6 |
| Area utilization | Low | High |
| Bits stored per cell | 2 | 1 |
| Read/write latency | $m$ to $2m-1$ | $m+1$ |
| Required external circuitry | Counter | *None* |

read/write control circuitry (AND and NOR gates), which, otherwise, does not significantly impact the nanoarchitecture performance.

## 7. CONCLUSIONS

This article presents a novel, shift-register-based QCA memory architecture. Benefits of the dual-phase, line-based memory cell are observed in the proposed shift-register-based architecture in a dense implementation with desired regularity in clock zone alignments. The read/write latency is linear in the number of bits stored per row, which records up to ∼2X improvements in read/write latency over of the tile-based memory architecture (with three-phase, line-based memory cells). Furthermore, unlike the tile-based memory architecture, shift-register-based architecture provides a constant read/write latency.

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# Simulation Based Study of On-chip Antennas for a Reconfigurable Hybrid 3D Wireless NoC

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***Abstract*—The feasibility of using on-chip antennas for a reconfigurable 3D wireless network-on-chip (3D-WiNoC) on a 3D integrated circuit (IC) is shown. The reconfigurable 3D-WiNoC is designed with on-chip antennas which are proposed to be used in conjunction with the metal interconnects making it a hybrid design. The feasibility of the on-chip antennas is shown by performing a 3-D finite element method (FEM) based full wave electro-magnetic analysis on a 3D IC model. The 3D IC is modeled according to a complimentary metal oxide semiconductor (CMOS) silicon on insulator (SoI) Benzocyclobutene (BCB) polymer adhesive bonding 3-D circuit integration technology. It is shown that it is possible to have two different frequency domains for the signal sources and the dynamic switching of the signal sinks between the two frequency domains, with minimal design and area overhead. When implemented, the proposed hybrid network architecture with two frequency channels can reduce the latency and increase the network throughput.**

## I. Introduction

The demand for high speed and high performance circuits has increased the trend of integrating large number of functional and storage cores onto a single die or system-on-chip (SoC). However, technology scaling of the devices provides new design challenges to the interconnect network that are required for communication between these functional and storage cores. Need for a global communication network between multiple cores on a SoC also increases the interconnect challenge. Technology scaling of the devices has increased the speed of the individual cores but it has also been accompanied by an increase in parasitics associated with the interconnects. The increased parasitics have caused the delay due to these interconnects to become higher than the gate delay [1]. The global interconnect networks therefore suffer from skew, jitter, power dissipation and area consumption [2], which has an increasing impact on the overall performance of the SoC [3].

The conventional design approaches introduced to mitigate the effect of the interconnect delay, such as changes to materials of the chip (e.g. use of low $\kappa$ dielectrics and high conductivity metals), can increase the scaling of the global interconnect system only by a few technology generations [1]. Hence, there is a need for alternate design solutions at the interconnect or the architecture level. Contemporary design solutions, such as the networks-on-chip (NoC), have been proposed to structure the design of the on-chip inter-core communication infrastructure [4]. In addition, 3D integrated circuits (3D ICs) can alleviate the problems of skew, jitter and delay caused by scaling of metal interconnects in planar integrated circuits (ICs). 3D ICs also provide opportunities for integration of wafers manufactured using different manufacturing processes and a true system-on-a-chip (SoC) [5]. The performance improvements in using a 3D network-on-chip (3D-NoC), over traditional NoCs is shown in [6, 7].

The 3D ICs use through silicon vias (TSVs) for communication between the tiers of the 3D IC stack. However, the TSVs suffer from a considerable utilization of the wiring footprint of the individual tiers of the 3D IC leaving less area for intra-tier routing and device placement, thereby imposing constraints on the number of TSVs per unit area [5]. Moreover, the process of fabricating TSVs for a multi-tier (more than 2 tiers) interconnection on a 3D IC is difficult for some TSV technologies and entirely prohibited for certain others [5]. Further, if two (2) laterally separated communication end-points on two (2) separate tiers are to be connected, then intra-tier routing is necessary.

The proposed alternative to address the communication challenge is to use radio frequency (RF) interconnects. In the RF interconnect based NoCs, the data is transmitted from one communication end-point to the other using electromagnetic (EM) waves. As the EM waves travel at the speed of light in the medium, a low latency and high bandwidth communication can be achieved [8]. There are two (2) types of RF IC interconnects of note: The micro-strip transmission line based interconnects operating in the RF range [9] and the wireless communication based intra-chip interconnects operating in the RF range [10]. This paper focuses on the simulation based analysis of the latter to investigate adaptability to a NoC implementation.

The proposed NoCs with wireless interconnects do not antiquate wire-based interconnects or the TSVs; the wireless RF interconnects are proposed to be used selectively for critical paths. To this end, a hybrid 3D wireless NoC is proposed that integrates the wireless RF interconnects with traditional metal wire based interconnects. The network throughput and latency improvements using the hybrid wireless NoC (WiNoC) are shown in [4, 8, 11]. In this paper, the concept of the hybrid wireless NoCs is novelly extended to 3D-NoCs making it a 3D wireless network-on-chip (3D-WiNoC). As another major contribution, two different frequency channels are provided with

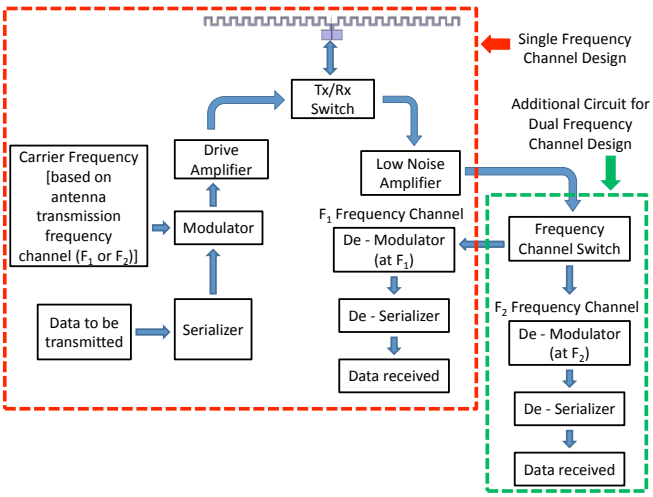



Fig. 1. Transceiver block diagram for the reconfigurable WiNoC.

inter channel communication capabilities, making the proposed 3D-WiNoC *reconfigurable*. Reconfigurability through multiple communication channels provides more flexibility to the network design and improves its latency with minimized area overhead.

This work is not a network analysis study but a feasibility study for the implementation and characterization of the proposed wireless RF interconnects. To this end, EM simulations are performed on the on-chip antennas on a 3D IC model. A network analysis study can only be performed after the feasibility and characterization of the antennas are well established. The proposed hybrid network architecture is presented in Section II. The simulation setup and the simulation results are discussed in Section III and Section IV, respectively. The key aspects of this paper are summarized in Section V.

## II. Proposed Hybrid Network Architecture

The WiNoCs proposed in [8] have a transceiver optimized to operate at the transmission frequency of the antenna—making it a single frequency design—as illustrated in Figure 1. Under such a design, if there are multiple antennas transmitting data simultaneously, there is a high possibility of corruption of data due to the collision of the two signals [11]. In order to avoid collisions, a medium access control (MAC) protocol, such as the one described in [11], can be used (similar to time division multiplexing). However, using a MAC protocol adds to the latency in the system and decreases the network throughput. In this regard, if there are multiple frequency channels, the network throughput and latency can be improved by having different antennas transmitting data simultaneously on different frequency channels (frequency division multiplexing of the channel). Having multiple antennas for different frequency channels to communicate between two identical communication end-points would require multiple transceivers, each optimized for a single frequency. Such a design will increase the area overhead tremendously making it impractical for most systems.

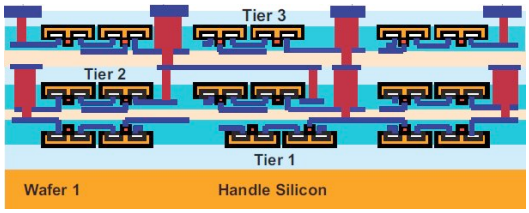



Fig. 2. 3D IC 3-tier integration structure.

In the proposed reconfigurable 3D-WiNoC design, the transceiver is designed with a receiver side operating at two receiving frequencies ($F_1$ and $F_2$) and with a transmitter side operating at a single frequency ($F_1$ or $F_2$) as illustrated in Figure 1. This design provides two different frequency channels for signal propagation with minimal increase in the circuit area overhead. The signal sources in this *reconfigurable* network design are grouped into one of the two frequency domains ($F_1$ or $F_2$). The reconfigurability in the network is due to the flexibility of the signal sinks (e.g. antennas) which can be moved dynamically into one of the two frequency domains ($F_1$ or $F_2$) with the frequency channel switch in Figure 1. Such a design is possible due to the characteristics of the antennas in the semiconductor implementation medium, as will be discussed in Section III and Section IV.

## III. Wireless Interconnect Analysis

The feasibility of on-chip antennas for intra-chip communication on planar ICs is shown in [10, 12]. High-speed operation capabilities of deep sub-micron devices have enabled circuits to operate at frequencies above 10 GHz. Since the physical dimension of an antenna is inversely proportional to its operating frequency, it is possible to have small antennas fabricated on chip using standard CMOS foundry processes. In [13–15], full wave simulation based studies are performed to study new antenna designs, the antenna characteristics in the semiconductor medium and to investigate the medium of propagation of the EM waves. However, all the previous works analyze the antenna characteristics and performance on planar ICs. In this paper, the concept of using on-chip antennas for global wireless communication is extended to 3D ICs. It is critical, for this purpose, for the simulation model to correctly incorporate the environment of operation.

In this paper, the wireless interconnects using on-chip antennas for the proposed reconfigurable 3D-WiNoC are simulated on a three tier 3D IC stack. In particular, the on-chip antennas for wireless inter-tier communication are simulated for a polymer adhesive IC tier bonding, embodied in a silicon on insulator (SoI) process [16]. The on-chip antennas can potentially be used for any of the 3D IC wafer bonding techniques. The cross-section view of the SoI 3D IC 3-tier integration is illustrated in Figure 2.

The simulations are performed in Ansoft HFSS (High Frequency Structure Simulator), a 3D finite element method (FEM) based full-wave electro-magnetic simulator [17]. Meander dipole antennas are used in the simulation

TABLE I
MATERIAL CHARACTERISTICS OF DIFFERENT SILICON REGIONS ON A DIE.

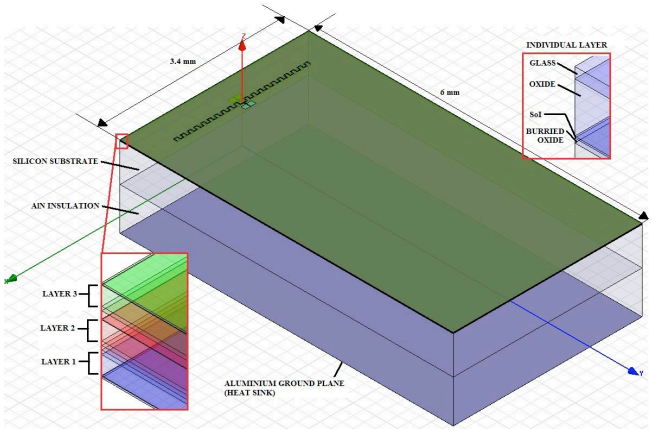
| Material | Conductivity (S/m) | Relative Permittivity |
|---|---|---|
| Silicon Dioxide | 0 | 3.7 |
| 2000 Ω-cm Silicon Substrate | 0.05 | 11.9 |
| P-type Epitaxial Silicon | 3636.36 | 11.9 |
| N-type Epitaxial Silicon | 1818.18 | 11.9 |

TABLE II
DIMENSIONAL PARAMETERS OF THE MEANDER DIPOLE ANTENNA.

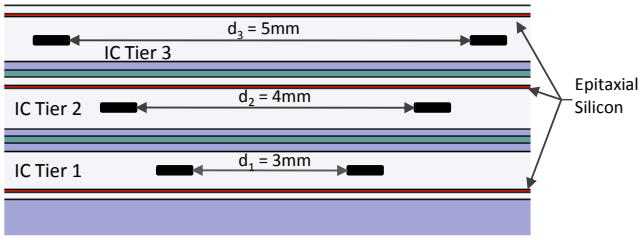
| Design Parameter | Magnitude |
|---|---|
| Arm Length (excluding bend lengths) | 1.2 mm |
| Arm Run Length (including bend lengths) | 2.4 mm |
| Bend Element Width | 10 $\mu$m |
| Bend Element Length | 60 $\mu$m |
| Antenna Thickness | 630 nm |

model as these antennas are more compatible with conventional CMOS technologies in having 90° bend angles. The antennas are designed with a total arm length (including the length of the meander segments) of 2.4 mm according to the parameters presented in [18]. Note that the parameters presented in [18] do not include a high conductivity epitaxial layer under the antennas. The presence of a high conductivity epitaxial layer can reduce the radiation frequency. Hence, to accurately model the environment of operation for the on-chip antennas, the conductivity parameters for the different materials on the die are used. These parameters are listed in Table I. The conductivity values are calculated from typical foundry parameters and doped semiconductor material resistivity data provided in [19]. The conductivity values do not change substantially from one technology generation to the other and therefore the design can easily be scaled with technology. The dimensional parameters for the meander dipole antennas are provided in Table II. The die size is 6×3.4 mm$^2$ as shown in Figure 3(a). The die size is selected arbitrarily to enable the integration of six (6) antennas of the dimensions reported in Table II. Varying the size of the dies impacts the presented simulations minimally.

The 3D-WiNoC is simulated for a six (6) antenna system. Two antennas are placed on each of the three IC tiers of the 3D IC stack with arbitrarily chosen lateral displacements of 5, 4, and 3 mm as shown in Figure 3(b) (antennas are depicted as black boxes). The antennas are identical, however placed near different epitaxial layers due to the semiconductor implementation medium. The difference in the transmitting frequency for these antennas with similar antenna structures is achieved due to the presence of high conductivity epitaxial layers under or above the antenna structures. The antennas placed on IC tiers 1 and 2 of the 3 tier IC stack are affected by two epitaxial layers with approximately equal separation for both set of antennas (antennas on tier 1 and tier 2). While the antennas placed on IC tier 3 are affected by two epitaxial layers placed closer than that for the antennas on IC tier 1 and 2 due to the 3D IC integration topology (face-to-face for IC tier 2 and face-to-back for IC tier 3 [5]).




(a) Simulated 3D IC structure.




(b) Antenna placement.

Fig. 3. Simulation setup for the reconfigurable WiNoC on a SoI 3DIC.

Hence, the transmitting frequency of the antennas on IC tiers 1 and 2 is similar while that of the antennas on IC tier 3 is different, thereby providing two different frequency channels for communication. The frequency range for the simulation is selected to be between 9 GHz to 15 GHz, based on the frequency range achievable with the antenna sizes.

## IV. RESULTS AND DISCUSSIONS

In experimentation, the scattering parameter (s-parameter) matrix $\overline{S}$ for the network is collected. The s-parameter matrix of a network characterizes the coupling between the ports of a network. An element, $S_{ij}$ of the s-parameter matrix $\overline{S}$ is the ratio of the normalized output power at port $i$ due to the normalized input power at port $j$ [20]. The s-parameter $S_{ii}$, also defined as the return loss, is used to determine the radiation frequency of the transmitting antenna. The s-parameter $S_{ij}$ characterizes the signal coupling between the receiving antenna $i$ and the transmitting antenna $j$. Hence, the s-parameter matrix is used to characterize the operation and efficiency of the reconfigurable 3D-WiNoC system.

As discussed in Section III, the presence of a thin high-conductivity epitaxial layer near the antenna structure shifts the radiation frequency. This characteristic of the 3D IC medium in having different epitaxial layers in different tiers creates two different frequency channels for communication using a single antenna design. The return loss (based on the maximum absolute value) of the antennas on different tiers is shown in Figure 4.

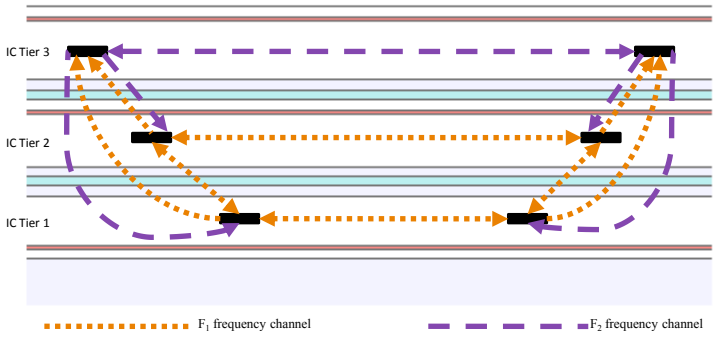



Fig. 5. The reconfigurable 3D-WiNoC with $F_1$ and $F_2$ frequency channels.

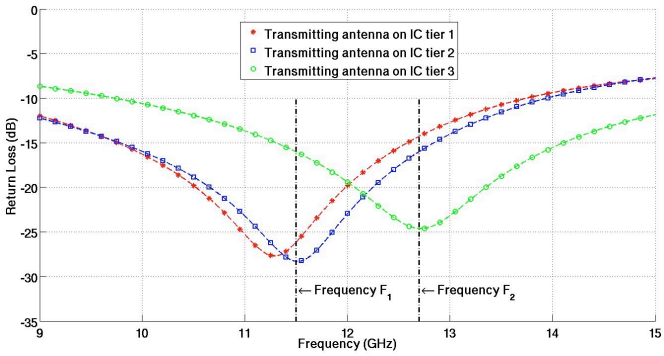



Fig. 4. Return loss $S_{11}$ at the transmitting antenna.

The lowest point of the dip indicates the frequency where the return loss is minimum; this is the frequency at which the antennas radiate energy most efficiently and therefore describes the frequency of operation of the antenna. As expected, the antennas on IC tier 1 and 2 operate at similar frequencies of $F_1 \approx 11.5\ GHz$ while the antennas on IC tier 3 operate at a different frequency of $F_2 \approx 12.7\ GHz$. These two frequencies provide the two different frequency channels for communication as depicted in Figure 5.

The figure of merit for an antenna pair is the transmission gain $G_a$ between the transmitting and receiving antenna. The transmission gain, $G_a$ of the antenna pair is computed using the following formula:

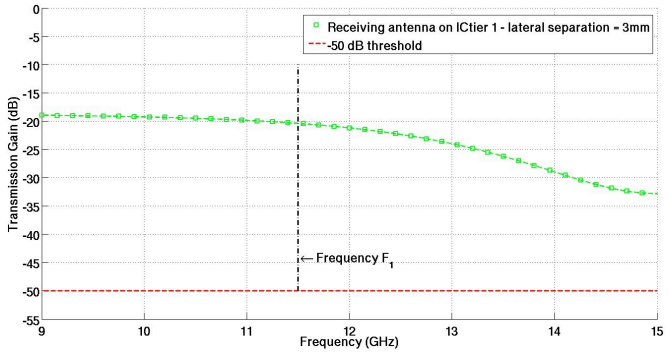
$$G_a = \frac{|S_{ij}|^2}{(1-|S_{ii}|^2)(1-|S_{jj}|^2)} = G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2 e^{-2\alpha R} \quad (1)$$

where $S_{ij}$ is the forward transmission between the receiving antenna $i$ and the transmitting antenna $j$, $S_{ii}$ is the reflection of the electric field at the receiving antenna and $S_{jj}$ is the reflection of the electric field at the transmitting antenna. $G_t$ and $G_r$ are the gains of the transmitting and receiving antennas, respectively, $\lambda$ is the wavelength of the electromagnetic waves based on the effective dielectric constant $\epsilon_r$, $\alpha$ is the attenuation constant and $R$ is the separation between the transmitting and receiving antennas.

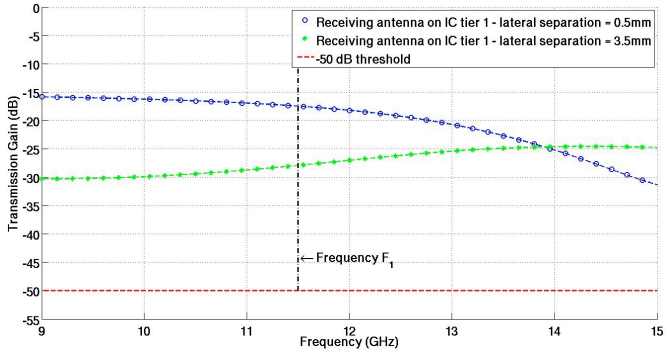
All the parameters $S_{ii}$, $S_{jj}$, and $S_{ij}$ are embodied in the s-parameter matrix $\overline{S}$ obtained from the 3D FEM analysis. A high value of the transmission gain indicates a good signal coupling. For an effective communication, it is required that the gain of the antenna pair be higher than the gain that can be provided using a low noise amplifier (LNA) at the receiving end. CMOS integrated LNAs are capable of providing gains as high as 50 dB [21], hence any transmission gain above a threshold of $-50$ dB is considered a communication channel.

Based on the return loss presented in Figure 4, the antennas on IC tier 1 transmit in the $F_1$ frequency channel in the transmitting mode. The strength of the signal coupling and the wireless channel indicated by the transmission gain between a transmitting antenna on any IC tier and a receiving antenna on IC tier 1 is shown in Figure 6. The transmission gain between a transmitting antenna on IC tier 1 and a receiving antenna on IC tier 1 communicating in the frequency channel $F_1$ is shown in Figure 6(a). The transmission gain between a transmitting antenna on IC tier 2 and a receiving antenna on IC tier 1 communicating in the frequency channel $F_1$ is shown in Figure 6(b). The transmission gain between a transmitting antenna on IC tier 3 and a receiving antenna on IC tier 1 communicating in the frequency channel $F_2$ is shown in Figure 6(c). Thus, in the receiving mode the antennas can receive signals in both the frequency channels $F_1$ and $F_2$. The transceiver can be switched from the transmitting mode to the receiving mode, or vice-versa, through the *Tx/Rx switch* shown in Figure 1. The receiver side of the transceiver can also be switched from frequency $F_1$ to $F_2$, or vice-versa, through the *frequency channel switch* as depicted in Figure 1. Similarly, the strength of the signal coupling and the wireless channel to a receiving antenna on IC tier 2 or IC tier 3 is shown in Figure 7 and Figure 8, respectively.

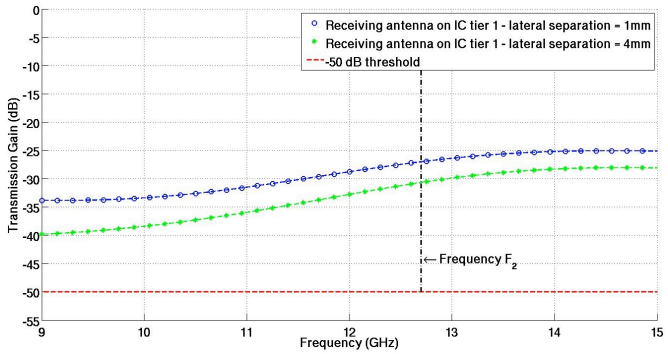
The transmission gain in all the cases is higher than the $-50$ dB threshold indicating an achievable effective communication between the transmitting and receiving antennas. The transmission distances achievable are higher than the ones assumed in [4, 8, 11], thereby providing a larger range for a single hop communication. The larger range of operation decreases the latency and increases the network throughput. The transmission gain will be lower for a larger lateral separation of antennas and higher for a smaller lateral separation of antennas as it is inversely proportional to the separation between the antennas as explained by (1).




(a) Received signal from antenna on IC tier 1 at frequency $F_1$.

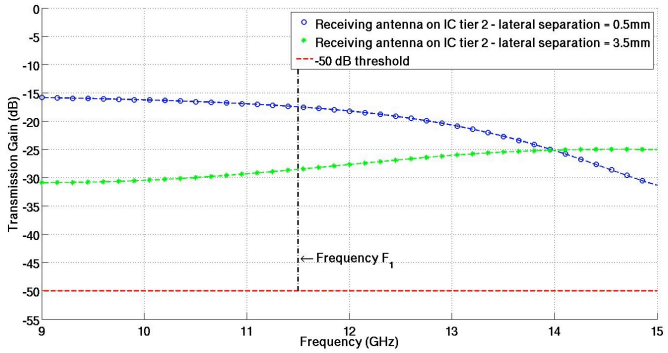



(b) Received signal from antennas on IC tier 2 at frequency $F_1$.

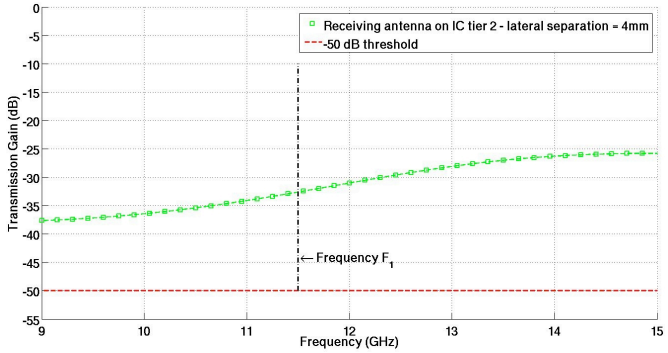



(c) Received signal from antennas on IC tier 3 at frequency $F_2$.

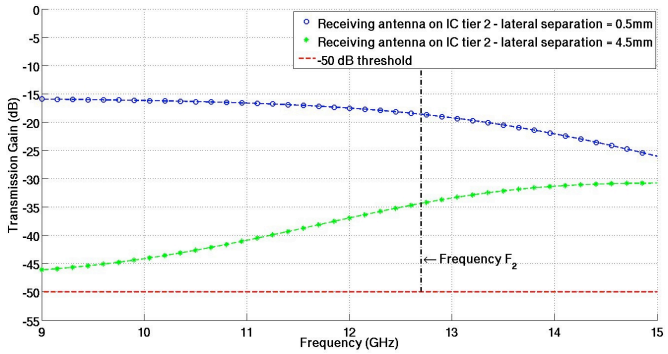
Fig. 6. Transmission gains for receiving antennas on IC tier 1.




(a) Received signal from antennas on IC tier 1 at frequency $F_1$.




(b) Received signal from antenna on IC tier 2 at frequency $F_1$.




(c) Received signal from antennas on IC tier 3 at frequency $F_2$.

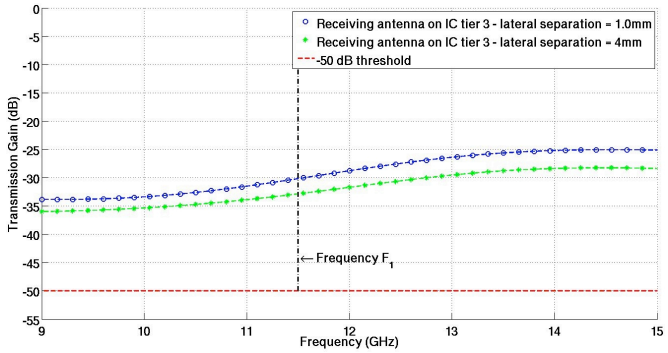
Fig. 7. Transmission gains for receiving antennas on IC tier 2.

The dynamic switching of the receiver between the two frequency domains provides the reconfigurability of the network. The reconfigurability is implementable due to the characteristics of the antennas in the semiconductor medium. The transmission gain between the antennas transmitting at frequency $F_1 \approx 11.5\ GHz$ (antennas on IC tier 1 and 2) and the receiving antennas (antennas on IC tier 3) (which transmit at frequency $F_2 \approx 12.7\ GHz$) is above the $-50$ dB threshold at frequency $F_1$, as shown in Figure 8(a) and Figure 8(b), thereby providing good signal coupling. Similarly, for the antennas transmitting at frequency $F_2$ (antennas on IC tier 3), the transmission gain between the $F_1$ and $F_2$ frequency channel antennas is above the $-50$ dB threshold at frequency $F_2$, as shown in Figure 6(c) and Figure 7(c), respectively.

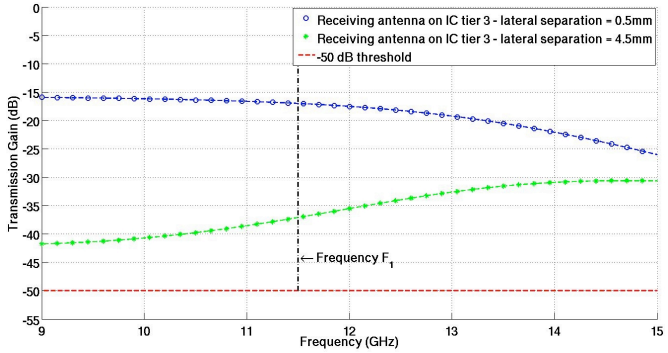
## V. Summary of Results

Based on the discussion in Section IV it is concluded that:

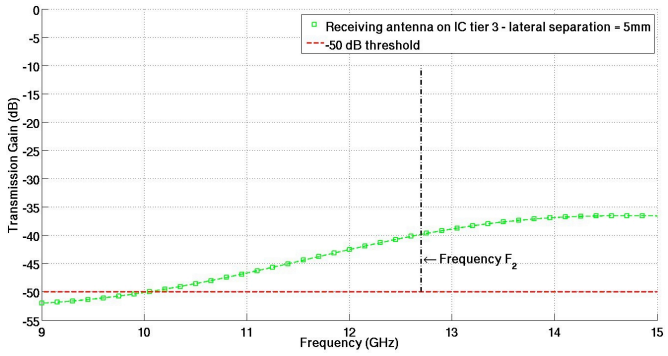
1) It is possible to have simultaneous communication between different communication end-points in two different frequency channels ($F_1 \approx 11.5\ GHz$ and $F_2 \approx 12.7\ GHz$ in the simulated environment).
2) The network has the following properties:
   a) The antennas in the transmitting mode on IC tier 1 and IC tier 2 are signal sources for the $F_1$ frequency channel and the antennas in the transmitting mode on IC tier 3 are the signal sources for the $F_2$ frequency channel.
   b) The signal sinks (antennas in the receiving mode on IC tier 1, IC tier 2 and IC tier 3) can be switched dynamically between either of the two




(a) Received signal from antennas on IC tier 1 at frequency $F_1$.




(b) Received signal from antennas on IC tier 2 at frequency $F_1$.




(c) Received signal from antenna on IC tier 3 at frequency $F_2$.

Fig. 8. Transmission gains for receiving antennas on IC tier 3.

frequency domains ($F_1$ or $F_2$) by switching the frequency channel switch depicted in Figure 1 to the appropriate channel using a control signal.

## VI. Conclusion

In this work, the feasibility of using on-chip antennas for a reconfigurable hybrid 3D wireless network-on-chip (reconfigurable 3D-WiNoC) is shown. Since the antennas and the associated circuitry are expected to occupy a considerable amount of space, they are intended to be used in conjunction (i.e. hybrid operation) with metal interconnects based 3D-NoC. This work discusses the feasibility and characterization of on-chip antennas for reconfigurable 3D-WiNoCs from a signal coupling point of view.

It is shown that it is possible not only to have a strong communication channel but also to have communication in two frequency channels. The two channels and the reconfigurable operation of the same antenna between the channels can provide improvements in the network latency and the throughput. The reconfigurability of the signal sinks in the network is achieved with a minimal area overhead.

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