Karthik Sangaiah

Ph.D. Candidate
Department of Electrical and Computer Engineering
Drexel University, Bossone 405, 3141 Chestnut Street
Philadelphia, PA 19104-2875

Phone: 919-360-9112
E-mail: ks499@drexel.edu
Url: vlsi.ece.drexel.edu

RESEARCH INTERESTS

Heterogeneous computing platforms, computer architecture design optimizations, high performance computing (HPC), communication networks on chip (NoC).

EDUCATION

- **Ph.D., Computer Engineering**, (September 2013 – current).
  Drexel University, Philadelphia, PA.
  Topic: Network-on-Chip Architectures for HPC
- **M.S., Computer Engineering**, GPA: 3.95, (June 2012).
  Drexel University, Philadelphia, PA.
  Concentration: Digital Design, Mixed-signal Embedded Systems, Computer Architecture
- **B.S., Electrical and Electronics Engineering**, GPA: 3.95 (summa cum laude), (June 2012).
  Drexel University, Philadelphia, PA.
  Concentration: Digital Design, Mixed-signal Embedded Systems, Computer Architecture

PROFESSIONAL EXPERIENCE

- **Research Assistant**, (Sept. 2013 – current)
  VLSI and Architecture Laboratory, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA, USA

  – Design of Network-on-Chip (NoC) architectures
  – Regression-based Design Space Exploration of NoC-based chip multiprocessors
  – Heterogeneous computing platforms
  – Application-aware memory and NoC co-design
  – Multi-threaded trace-based system simulation for evaluating many-core architectures and NoCs

- **Research Internship**, (June. 2015 – Dec. 2015)
  ARM Research
  Cambridge, UK

  – Extension of PhD project SynchroTrace to support ARM-based CMPs
  – Exploration of HPC platforms with SynchroTrace
  – Design of visualization tool to enable coarse-grained analysis of HPC thread behavior

- **Teaching Assistant**, (Sept. 2013 – Sept. 2014, Jan. 2017, Sept. 2017 – Mar. 2018)
  Department of Electrical and Computer Engineering & College of Engineering
  Drexel University, Philadelphia, PA, USA

  – ECEC 301, Advanced Programming for Engineers (Fall 2017)
  – ECEC 302, Digital Systems Projects (Fall 2013, Spring 2014, Fall 2017)
  – ECEC 304, Design with Microcontrollers (Winter 2014)
  – ECEC 355, Computer Architecture (Summer 2014, Winter 2017)
  – ECE 203, Programming for Engineers (Winter 2018)
  – ENGR 121, Computation Lab I (Fall 2017)

- **Combat Systems Engineer**, (July 2012 – Sept. 2013)
  Lockheed Martin MST
  Moorestown, NJ

– Designed a commercial-off-the-shelf (COTS) FPGA-based solution for replacing an internally-produced VME sensor monitor embedded computer
– Evaluated the application compatibility and performance impact of upgrading to a 64-bit Red Hawk OS
– Performed a full system capacity analysis for optimizing application performance on large-scale CMPs

◇ **R&D and Information Assurance (IA) Co-op**, (March 2011 - Sept. 2011)
Lockheed Martin MST
Moorestown, NJ

– Examined the impact of future radar parameters on Ballistic Missile Defense performance
– Performed an R&D evaluation of the Cisco Unified Computing System product line for combat ship system processing
– Executed vulnerability investigations and administered hardening of combat systems on a 60 node network

◇ **Computing and Network Infrastructure (CNI) Co-op**, (Sept. 2008 - Sept. 2010)
Lockheed Martin MST
Moorestown, NJ

– Wrote five trade studies for the customer based on research of advances in COTS hardware
– Provided network support during 12–hour and 24–hour stress and endurance tests of the Combat System Ship Qualification Testing of a 60 node network
– Evaluated a network management software for three assets and presented the findings to the customer
– Acted as the primary contact between the CNI team and three COTS vendors
– Trained two new team members in troubleshooting and designing components of the combat system

ACADEMIC HONORS, AWARDS, AND ACTIVITIES

◇ NSF Graduate Research Fellowship Program Recipient, 2014.
◇ George Hill, Jr. Fellow, Drexel University, 2014 – 2015.
◇ George Hill, Jr. Fellow, Drexel University, 2013 – 2014.
◇ Drexel IEEE Graduate Forum, President, Fall 2016 – Fall 2017.
◇ Drexel Fellowships Ambassador, Fall 2015 – Present.
◇ Graduated summa cum laude from the Department of Electrical and Computer Engineering, Drexel University, 2012.
◇ Boeing Company Scholarship, Fall 2012.
◇ Tau Beta Pi Scholar, Spring 2011.
◇ Harry E. Muchnic Scholarship, Spring 2011.
◇ Dean's List, Drexel University, 2007 – 2012.
◇ Eta Kappa Nu Vice President, Spring 2011 – Spring 2012.
◇ Tau Beta Pi Vice President, Fall 2010 – Fall 2011.

SELECTED PROJECTS

◇ **SynchroTrace**
– Architecture-agnostic, event-based network-on-chip simulation framework
– Synchronization and dependency-aware event traces of multi-threaded applications to generate real application traffic on a network-on-chip simulator
– Fast simulation of HPC-based CMP platforms
– Static and Dynamic Thread Mapping based on application communication characterization

◇ **UncoreRPD**
– Regression-based design space exploration methodology of the Memory-NoC design space
– Examining the impact of sampling methodology on overall prediction accuracy

◇ **Master's Thesis on Variable Fractional Delay (VFD) Filters on Reconfigurable Hardware**
– Based on order-scalable and modular FIR filters
– Developed hardware and software-based Lagrange coefficient computational unit
– Tested and verified on Xilinx Virtex-6 and Spartan-6 FPGAs

◇ **Evaluation of an Accelerator Architecture for Speckle Reducing Anisotropic Diffusion (SRAD)**
– Accelerator proof of concept for SRAD medical imaging algorithm
– Compared performance of in-lab developed SRAD accelerator with a massively parallel GPU and multi-threaded CPU SRAD algorithm

◇ **Statistical Power Analysis for Estimating GPU Power Consumption via Machine Learning**
– Online statistical model-learning of power utilization of GPU functional units to estimate power utilization in real-time
– Empirical data generated by GPGPU benchmarks and GPU intensive applications

SKILLS

◇ Simulation frameworks: gem5, Sniper, McPAT, CACTI
◇ Xilinx FPGAs (Spartan-3 & 6, Virtex-6), Cypress PSoC 1 & 3, Intel 8051
◇ C, C++, VHDL, Perl, Python, Basic Java
◇ Pthread, OpenMP, CUDA, CilkPlus
◇ Cadence – Virtuoso Suite, PSpice
◇ ModelSim, Xilinx ISE, EDK, & System Generator, Matlab, WireShark
◇ LaTeX, vim, Office Suites
◇ Unix, Linux, Windows, DOS

RELEVANT GRADUATE COURSEWORK

◇ Network-on-a-Chip (NoC), High Performance Computer Architecture, Parallel Computer Architecture, VLSI Design with FPGAs, Data Structures and Algorithms, Advanced Programming Techniques, Embedded Systems, Performance Analysis of Computer Networking, CMOS VLSI Circuit and Systems Design, Fundamentals of Systems I & II.

PUBLICATIONS

◇ M. Lui, K. Sangaiah, M. Hempstead, and B. Taskin, "Towards Cross-Framework Workload Analysis via Flexible Event-Driven Interfaces", IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), Belfast, Northern Ireland, April 2018.

◇ K. Sangaiah, M. Lui, R. Jagtap, S. Diestelhorst, S. Nilakantan, A. More, B. Taskin, and M. Hempstead, "SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multicore Simulation of CMP and HPC Workloads", ACM Transactions on Architecture and Code Optimization (TACO), In Print.

◇ K. Sangaiah, B. Taskin, M. Hempstead, "Fast Multicore Simulation and Performance Analysis of HPC Applications with SynchroTrace", *Boston Area Architecture Workshop (BARC 2016)*, 29 Jan. 2016.

◇ K. Sangaiah, M. Hempstead, B. Taskin, "Uncore RPD: Rapid Design Space Exploration of the Uncore via Regression Modeling", *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2015)*, 7-10 Nov. 2015.

- S. Nilakantan, K. Sangaiah, A. More, G. Salvador, B. Taskin, M. Hempstead, "SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multi-core Simulation", *Proceedings of IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2015)*, 29-31 March 2015.
- K. Sangaiah and P. Nagvajara, "Variable fractional digital delay filter on reconfigurable hardware", *Proceedings of IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS 2012)*, 5-8 August 2012, pages 430-433.
- S. Nilakantan, S. Annangi, N. Gulati, K. Sangaiah, M. Hempstead, "Evaluation of an accelerator architecture for Speckle Reducing Anisotropic Diffusion", *Proceedings of ACM International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, 9-14 Oct. 2011, pp.185-194.

REFERENCES

- **Dr. Baris Taskin**
  Associate Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  E-mail: taskin@coe.drexel.edu
- **Dr. Mark Hempstead**
  Associate Professor, Department of Electrical and Computer Engineering
  Tufts University, Medford, MA
  E-mail: mark@ece.tufts.edu
- **Dr. Prawat Nagvajara**
  Associate Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  E-mail: nagvajara@ece.drexel.edu