Robust Low Power Clock Synchronization for Multi-Die Systems

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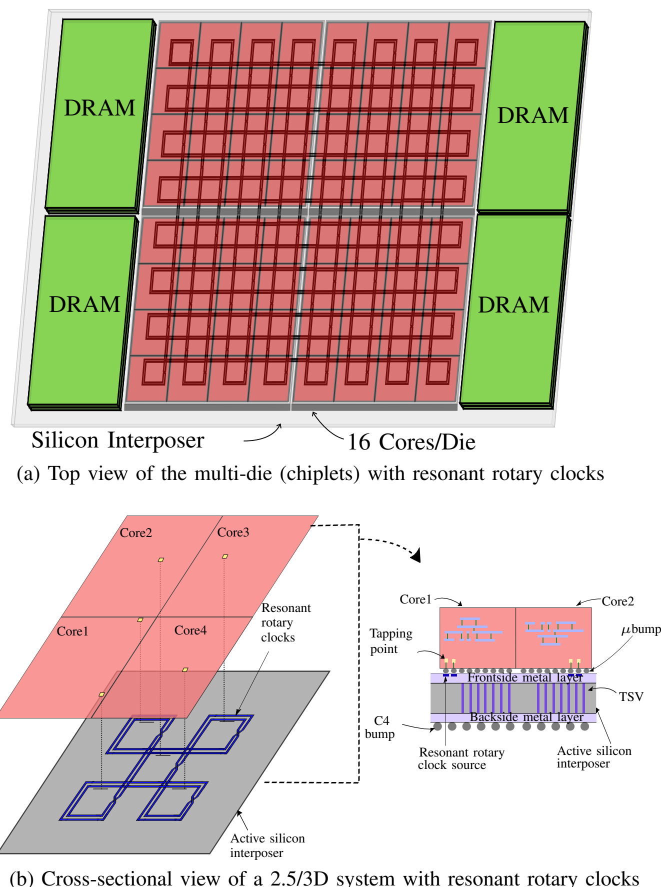
***Abstract*—A novel clock generation and distribution network is proposed for multi-die architectures connected through an active silicon interposer. The proposed clock network generates and distributes a resonant clock through the active silicon interposer between dies, with each die served through resonant local clock trees. The proposed active silicon interposer rotary oscillator array (AI-ROA) serves to establish a unitary clock domain, providing constant phase and magnitude clock sources to the multiple die (i.e. multiple chiplets) in the package. Analysis is performed with multiple ARM CORTEX M0 cores per die of a homogeneous multi-die package architecture. Each M0 core of the multi-die package belongs to the unitary clock domain, designed with AI-ROA to operate at a frequency of 1 GHz. The multiple die are designed in the 28 nm technology node and the active interposer is designed in the 65 nm technology node. `SPICE` based simulations of post-layout models provides analysis and evaluation of the proposed architecture for performance metrics under process, voltage, and temperature variations. In particular, performance metrics are reported for 1) power consumption in comparison to PLL based architectures designed and synthesized with an industrial tool, 2) robustness against process variations, and 3) clock skew across the cores throughout the multiple die.**

I. INTRODUCTION

Stacking multiple die (i.e. chiplets) on a silicon interposer within a single package allows for higher throughput per watt and dense integration of cores. Multi-die systems are actively researched and implemented in industry and academia [1–8]. More recently, server grade System-on-Chip (SoC) processors are designed with multiple die including the 32-core AMD Epyc and Threadripper processors [5].

The interposers are primarily categorized as either active, with integrated transistors, or passive, with resistive, capacitive, and/or inductive components only. Multi-die integration with passive interposers have demonstrated cost reduction and superior yield [6, 9]. In contrast, multi-die integration with active interposers have demonstrated higher interconnect performance while sacrificing yield [1–5].

In this work, the high interconnect performance of the active interposer is used to implement a single clocking domain across the multiple die. The proposed approach leverages the high quality interconnect performance offered by the 2.5D system while addressing a major challenge in SoC systems of interposer-based architectures, specifically, cross-die synchronization [6, 9]. In this work, multi-die systems are synchronized with resonant rotary traveling wave oscillators (ReRoCs) organized in an array topology on the active silicon interposer as shown in Figure 1. The proposed ReRoC



(a) Top view of the multi-die (chiplets) with resonant rotary clocks

(b) Cross-sectional view of a 2.5/3D system with resonant rotary clocks

Fig. 1: Active silicon interposer based synchronization topology for multi-die systems with resonant rotary clocks.

oscillatory array (ROA) on the active interposer, coined AI-ROA, provides a unitary clock domain for the entire multi-die system (MDS).

Designing high-speed, low-skew, low-jitter, and low-power clocks across multiple die and the interposer is challenging over a large area [4, 6, 9]. The clock network must be tolerant to within-die, die-to-die, and die-to-interposer parametric variations, as well as with potentially different fabrication technologies between the processor layers (chiplets) and the interposer. Challenges in synchronization for 3D IC systems have been described in literature. Prior work on 3D integrated circuits have analyzed clock distribution over multiple-planes with different clock distribution topologies [10] or utilized

digitally controlled delay lines for clock synchronization [11]. The proposed AI-ROA is implemented with balanced load clock trees designed for each core within the MDS. The self-tuning nature of ReRoC, in terms of jitter and phase correction through self-resonance, and phase-locking between ReRoC rings of the AI-ROA array over a large area, provide high robustness to process and environmental variations. To evaluate the efficacy of the proposed clock generation and synchronization architecture of AI-ROA, multiple instantiations of the ARM CORTEX M0 core is used to design a homogeneous MDS of multiple multi-ARM-core chiplets, with all cores operating at 1 GHz. The contributions of this work include:

1) Synchronized clock distribution across the multi-die systems, i.e., one synchronized clock domain,
2) Low-power resonant clock generation on the active silicon interposer, and
3) Robust clock distribution across the multi-die system.

The paper is organized as follows. Background material on resonant rotary clocking is reviewed in Section II. The proposed AI-ROA architecture for synchronized clock generation and distribution for active interposer based multi-die systems are presented in Section III. The experimental setup and results are presented in Section IV. Concluding remarks are provided in Section V.

II. Resonant Clocking Background

The resonant rotary clocks (ReRoCs) are designed using transmission lines. CMOS inverters are distributed uniformly along the transmission lines in anti-parallel fashion to power and amplify the signals adiabatically as shown in Figure 2. The ReRoC is modeled as an LC oscillator, with an approximate frequency given by

$$f_{osc} \approx \frac{1}{2\sqrt{L_T C_T}}. \quad (1)$$

The total inductance and total capacitance of a ReRoC ring are defined as L_T and C_T, respectively. The inductance L_T depends on the geometry of the ReRoC [12]. For large floorplans, multiple ReRoC rings are connected across corner tapping points in an array topology as shown in Figure 1(b), called a rotary oscillatory array (ROA) [12, 13].

For an ReRoC, the higher the frequency, the lower the power dissipation [14, 15]. A high frequency ReRoC master clock, divided to lower operating frequencies through the rotary frequency dividers [14] provides a power optimized solution at a target operating frequency.

Capacitive load and inductance affect the frequency of oscillations of an ReRoC as given by (1). The ReRoC rings in an ROA topology [12]) are designed with the same physical parameters including the perimeter and structure. Therefore, the inductance L_T of the rotary rings is identical. From (1), the total capacitance is estimated as

$$C_T = \Sigma\, C_{tra} + \Sigma\, C_{inv} + \Sigma\, C_{reg} + \Sigma\, C_{wire}, \quad (2)$$

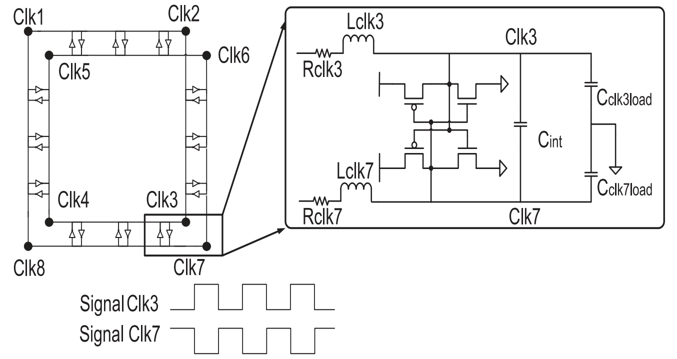


Fig. 2: Resonant rotary clock topology.

where C_{tra}, C_{inv}, C_{reg}, and C_{wire} are the capacitances contributed by the transmission line, inverter pairs, registers, and the register tapping wires, respectively. The capacitance of the transmission lines and inverter pairs are extracted from the geometries of the ROA topology. The capacitance of the registers C_{reg} and the register tapping wires C_{wire} depend on the number of registers connected to each ring and the tapping wire length of each connection. In order to maintain the self-oscillating operation of an ReRoC (and the ROA) with L_T and C_T, a balanced distribution of the parasitic components across multiple tapping points on an ROA is necessary.

III. Proposed Architecture

The quality of the synchronization of the cores in terms of clock skew in multi-die systems (MDS) with the active silicon interposer over a large area with resonant rotary clock oscillatory array (i.e. AI-ROA) requires 1) a balanced capacitance at each tapping point, 2) a bounded skew, and 3) robustness against variations. ReRoCs, through self-resonance, self-tuning, and in-phase locking across rotary rings in an ROA topology, are robust to local variations. A local variation affecting a local ReRoC ring, therefore, gets compensated across the ROA, as each local ReRoC ring is phase locked [12], and quickly recovers back to the stable resonance mode (or stabilizes at a new resonance mode with all other rings). Th ROA structure also limits jitter and skew variations. The self-resonance, on the other hand, requires algorithmic solutions that produce a balanced load across the ROA. The sensitivity of the ReRoCs to capacitive imbalance is reported in [13] as permitting no more than 25% variation in the total capacitive load at any tap, which can be achieved by applying heuristic ReRoC synthesis algorithms. First, the subtree networks for each core in the die of the MDS are designed in order to balance the loads distributed across the die and the MDS. Second, the AI-ROA is placed on the interposer to generate one-to-one matching between the subtree roots and the tapping points on the ReRoC rings of the AI-ROA. The objective of the automated one-to-one matching is to balance the delay among the subnetwork trees of the AI-ROA.

Algorithm 1: Register clustering

Input: Sink set **R**, number of subnetwork trees m and capacitance tolerance τ.

Output: Balanced cluster set $\{K_1, K_2, ..., K_m\}$

1: $[\{K_1, K_2, ..., K_m\}, \{cen_1, cen_2, ..., cen_m\}]$ = k-means(R, m).
2: **for each** i to m **do**
3: $C_{max} \leftarrow$ Largest capacitance cluster K_{i_1};
4: $C_{min} \leftarrow$ Smallest capacitance cluster K_{j_1};
5: **end for**
6: **while** $(C_{max} - C_{min})/C_{max} > \tau$ **do**
7: Find min$\{d(r_{(i_1,j)}, cen_{i_2})\}$, where $r_i \in K_{i_1}$, $i_2 = \{1, 2, ..., m, i_2 \neq i_1\}$
8: $K_{i_2} = K_{i_2} \cup r_{i_1,j}$
9: Label $r_{i_1,j}$ cannot be moved back to K_{i_1}
10: Update C_{max} and C_{min}
11: **end while**
12: Generate m unbuffered steiner trees with BST/DME.

A. Subtree Network Generation

The subtree network for each core in the MDS is designed to provide a balanced load to the AI-ROA parent ring topology in the interposer. The AI-ROA requires balanced loads to avoid an imbalance of parasitics [L_T and C_T in (1)] in the self-resonance. Each core in the MDS is modeled with m tapping points to the AI-ROA parent, where the number of subnetwork trees per core is $m = \#cores/\#ReRoC\ rings$. In order to generate a balanced load and meet skew targets (a global zero skew budget or a desired skew schedule, e.g. for concurrent clock optimization) the k-means method is applied, which is given by Algorithm 1. A user-defined balanced capacitance tolerance ratio is defined as,

$$\tau = (C_{max} - C_{min})/C_{max}. \quad (3)$$

In (3), C_{max} and C_{min} are the maximum and minimum total capacitance among all the clusters, respectively. The value of τ is set to 0.25, which constrains the range of C_{max} and C_{min}. The inputs are the register locations, number of subnetwork trees m, and the capacitance tolerance ratio τ. The outputs are the budgeted skew and the capacitively balanced clusters $K_1, K_2, ..., K_m$. The total capacitance across each cluster i is estimated by

$$C_i^{tot} = \sum_{j=1}^{n_i}(C_{i,j} + C_{i,j}^{wire}). \quad (4)$$

In (4), $C_{i,j}$ is the capacitance of the register $r_{i,j}$ in the cluster K_i, where $j = 1, ..., n_i$ and n_i is the total number of registers in the cluster K_i. $C_{i,j}^{wire}$ represents the parasitic capacitance of a wire with a Manhattan distance between the register $r_{i,j}$ and the centroid cen_i of the cluster K_i. The interconnect length between the centroid and each register is used to approximate the total wire length of the cluster. C_{tot} is the total capacitance of the registers and wires.

Algorithm 2: Generation of tapping point set

Input: Tapping point set S, subtree root set D and micro-bump locations Bu

Output: Optimized tapping point set S_{opt}, optimal matching record F_{opt}, best transformation vector t_{opt}

1: Initialize $cost = \infty$, $cost_{new} = 0$;
2: **while** $|cost - cost_{new}| > \triangle$ **do**
3: $[F, cost_{new}] = best_matching(S, D, Bu)$;
4: $\mathbf{t} = best_move(S, D, Bu, F)$;
5: $cost = cost_{new}$
6: $cost_{new} = COST(F, S, D, Bu, t)$
7: $S = S + \mathbf{t}$;
8: **end while**
9: $S_{opt} = S, F_{opt} = F, \mathbf{t}_{opt} = \mathbf{t}$;

The capacitance of all clusters is balanced heuristically. For the largest capacitance difference among all the clusters above the capacitance tolerance ratio τ, registers are moved out of the cluster with the largest total capacitance to the cluster with the smallest distance to the centroid of the cluster (line 7 in Algorithm 1). The register closest to the centroid of the candidate cluster is, therefore, selected as the target register. To avoid convergence problems, once a register is moved from a cluster, the register is not permitted to be moved again. The process is terminated when the defined τ is achieved across all the clusters.

After the clusters are generated, skew budgeted subnetwork trees are synthesized. The bounded-skew tree based on the deferred-merge and embedding (BST/DME) [16] algorithm is used to generate m unbuffered steiner trees. The local trees are unbuffered to maintain the adiabatic switching of the AI-ROA, where capacitively balanced topologies of local unbuffered trees become part of the resonating structure.

B. ReRoC Implementation

The process of generating the set of tapping points begins by determining the tapping point locations on an ReRoC distributed oscillatory array (ROA) implemented in the active silicon interposer (AI-ROA). In order to deliver the clock from the interposer to the subtree roots in the MDS, each clock source requires at least one micro-bump. The objective of the optimization process is to minimize the total delay. To ensure the total delay is optimized across the AI-ROA, a process based on the earth movers distance approach (EMD) is used [13]. The EMD is a measure of distance between discrete and finite distributions. A method based on a *modified* earth movers distance under transformations ($EMD_{\mathbf{t}}$) is used as proposed in [13]. The $EMD_{\mathbf{t}}$ is a transformation performed on one distribution to incrementally move the whole distribution towards a second distribution to minimize the EMD. The $EMD_{\mathbf{t}}$ approach is modified to account for the locations and parasitics of the micro-bump in this work. The $EMD_{\mathbf{t}}$ shifts the square shaped AI-ROA to generate a one-to-one matching between the subtree roots and the tapping points, which results

in a balanced delay among the subnetwork trees connected through the micro-bumps.

The inputs for Algorithm 2 are the AI-ROA tapping points S, the set of subtree roots D obtained after register clustering and the locations of the micro-bumps Bu. For any transformation $\mathbf{t} \in \mathbf{R}^2$, the tapping points on the ReRoC rings of the AI-ROA are shifted by the same transformation $\mathbf{t}$:

$$S + \mathbf{t} = \{s_1 + \mathbf{t}, s_2 + \mathbf{t}, ..., s_m + \mathbf{t}\}. \quad (5)$$

The $COST$ function returns a calculated delay from s_i + $\mathbf{t}$ to a single register $\mathbf{R}_{jk}$ in the subtree d_j. The problem is formulated as $F = (f_{ij}) \in \mathbf{R}^{(m \times n)}$, where f_{ij} = 1 indicates a one-to-one matching from $s_i + \mathbf{t}$ to subtree root d_j [13]. The Elmore delay model for the cost function is given by

$$t(s_i + \mathbf{t}, \mathbf{R}_{jk}) = |s_i + \mathbf{t} - d_j| \cdot r(\frac{|s_i + \mathbf{t} - d_j| \cdot c}{2} + Cap(d_j)) + r_\mu c_\mu + \sum_{e_w \in Path(d_j, \mathbf{R}_{jk})} |e_w| \cdot r(\frac{|e_w| \cdot c}{2} + Cap(w)). \quad (6)$$

In (6), r and c denote the unit length wire resistance and capacitance, respectively. The micro-bumps are modeled as a lumped resistance r_μ and a lumped capacitance c_μ. $Cap(w)$ denotes the total capacitance at the point w. In (6), $\frac{|s_i + \mathbf{t} - d_j| \cdot c}{2} \ll Cap(d_j)$, which results in the total capacitance of each subtree being approximately equal to $Cap(d_j)$. Since the registers in each subtree network are fixed before matching the tapping points to the subtree roots, the summation term of (6) is a constant given by $const_j$. (6) is, therefore, re-written as

$$t(s_i + \mathbf{t}, \mathbf{R}_{jk}) \approx |s_i + \mathbf{t} - d_j| \cdot r \cdot Cap(d_j) + r_\mu c_\mu + const_j. \quad (7)$$

The $COST$ function is, therefore, the sum of the total delay of the set of registers in tapping point set S, subtree root set D, and micro-bump location Bu with matching F and transformation $\mathbf{t}$. The total summed delay represents the delay due to the weighted total wirelength from the tapping points to the subtree roots. The skew is dependent on the total capacitance on each subtree $Cap(d_j)$.

The process outlined by Algorithm 2 includes two steps:

1) best_matching: the constraint f_{ij} = 0 or 1 is set to $0 \leq f_{ij} \leq 1$ in order to apply linear programming to find the best match, and
2) best_move: the square shaped ROA is systematically moved to minimize the cost function.

Manhattan routing is used to calculate the total minimum delay. The minimum weighted total stub wirelength and the total capacitance of each subtree are the criteria applied to balance the skew among all the subtrees. Algorithm 2 iterates until the cost function between two iterations is less than a tolerance, $\triangle$. The set of tapping points contributing to the best matching is S_{opt}, the best matching result is F_{opt}, and the optimal transformation is $\mathbf{t}_{opt}$.

C. Variation Analysis

Spatial and temporal variations affect the characteristics of the transistors, especially the transistor threshold voltage (V_t). Along with variations in V_t, the variations in the geometric properties of the AI-ROA transmission line interconnects, supply voltage, and temperature are the primary factors affecting the frequency and power consumption of the clock signals. The within die (WID), die-to-die (D2D), and die-to-interposer (DIP) variations impact the overall clock generation and delivery to the multi-die system. Random variables r, y, and x are applied for WID, D2D, and DIP, respectively, to account for the various sources of variations. The DIP variation (x_i) has two normal distributions: 1) The core variations in a 28 nm node and 2) the variations of the ReRoCs in 65 nm. The random variables are expressed as,

$$\begin{aligned} x_i &\sim N(0, \sigma^2_{DIP}), \\ y_i &\sim N(0, \sigma^2_{D2D}), \\ r_i &\sim y_i + x_i + N(0, \sigma^2_{WID}) + r^0_i. \end{aligned} \quad (8)$$

In (8), r^0_i is the nominal value of r_i. The parameters included for the analysis of the PVT variations in the die and interposer are listed in Table I, where the worst case value of each parameter is considered in this work. The geometries of the ReRoCs, the V_t of the transistors in the active silicon interposer, and the variations in the clock trees on the multiple die with the CORTEX M0 cores as loads are considered for the analysis.

IV. Experimental Analysis

The proposed architecture is implemented with multiple ARM CORTEX M0 cores per die, for two different dimensions of the MDS: 1) A 5 mm×5 mm MDS with 4 dies, each die with 4 M0 cores and 2) a 10 mm×10 mm MDS with 4 larger dies, each larger die with 16 M0 cores. An industrial 65 nm technology with 7 metal layers is used for the active silicon interposer and a 28 nm industrial node with 7 metal layers for the multiple die. The skew budget is set to 10 ps.

TABLE I: Parameters for PVT variation.

Category	Var. range (28 nm)	Var. range (65 nm)	Nom. ReRoC (65 nm)
V_{dd}	± 10%	± 10%	1.2 V
W_{tline}	–	± 10%	20 µm
Sep_{tline}	–	± 10%	25 µm
Temp.	– 40°C to 125°C	– 40°C to 125°C	25°C
σ_{V_t}	60 mV	60 mV	–

TABLE II: Design parameters for the analysis.

Category	5 mm×5 mm	10 mm×10 mm
# die	4	4
# cores/die	4	16
CORTEX M0 dimension	1 mm×1 mm	1 mm×1 mm
V_{dd}	1.2 V	1.2 V
Nom. Temp.	25°C	25°C
μ_{bump} pitch	40 µm	40 µm
μ_{bump} height/width	10 µm/5 µm	10 µm/5 µm
ReRoC W_{tline}	20 µm	20 µm
ReRoC Sep_{tline}	25 µm	25 µm

TABLE III: Power consumption of PLL clocked circuit as compared to the proposed AI-ROA distributed on an active silicon circuit operating at a frequency of 1 GHz, a V_{dd} of 1.2 V, and temperature of 25 °C.

Die dimension	#dies / #core/die	PLL clocked design				
		$PLL_{clock/die}$ power (mW)	$PLL_{core/die}$ power (mW)	$PLL_{clock/mds}$ power (mW)	$PLL_{core/mds}$ power (mW)	Skew (ps)
5 mm×5 mm	4/4	71.62	223.12	370.58	942.48	7.4
10 mm×10 mm	4/16	304.71	910.40	6295.80	14641.40	7.1

Die dimension	#dies / #core/die	`This Work`				
		`AI-ROA`$_{clock/die}$ power (mW)	`AI-ROA`$_{core/die}$ power (mW)	`AI-ROA`$_{clock/mds}$ power (mW)	`AI-ROA`$_{core/mds}$ power (mW)	Skew (ps)
5 mm×5 mm	4/4	23.13 (-67.71%)	138.48 (-37.93%)	105.24 (-71.60%)	553.92 (-41.23%)	8.7
10 mm×10 mm	4/16	86.23 (-71.70%)	562.88 (-38.17%)	1684.14 (-73.25%)	9006.08 (-38.49%)	7.9
Average this work	-	-70%	-38%	-72%	-40%	8.3

The dies and interposer are placed and routed with Cadence Innovus. The transmission lines of the ReRoCs implemented in the top two metal layers of the active silicon interposer (65 nm technology) are modeled and simulated using the high frequency structural simulator (HFSS). The micro-bumps have a pitch of 40 µm and are modeled as lumped *RC* elements [17]. To extract the parasitic impedances of the circuit after place and route, Mentor Graphics Calibre is utilized. Post-layout `SPICE` analysis is performed to more accurately characterize the AI-ROA. The design parameters for the `SPICE` analysis are listed in Table II.

An AI-ROA operating at 3 GHz is designed with a perimeter length of 1000 µm per individual ReRoC ring. Frequency dividing the ReRoC by three generates the 1 GHz clock required for the CORTEX M0 cores. The ReRoC rings are distributed as an rotary oscillator array (ROA) across the active silicon interposer area, forming the AI-ROA. The multi-die system and the active silicon interposer operate at the same voltage ($V_{dd} = 1.2$ V). The topology of the CORTEX M0 multi-die system and AI-ROA are illustrated in Figure 3,. Three sets of results are presented in this work, a) the power consumption of the multi-die system designed with ReRoCs operating at 1 GHz, b) the clock skew, and c) the variation analysis.

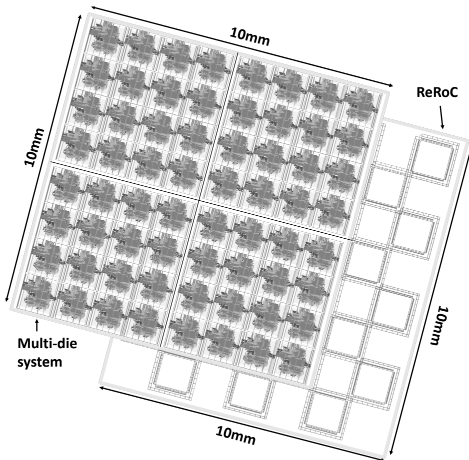


Fig. 3: Multi-die system implemented with CORTEX M0 cores and AI-ROA.

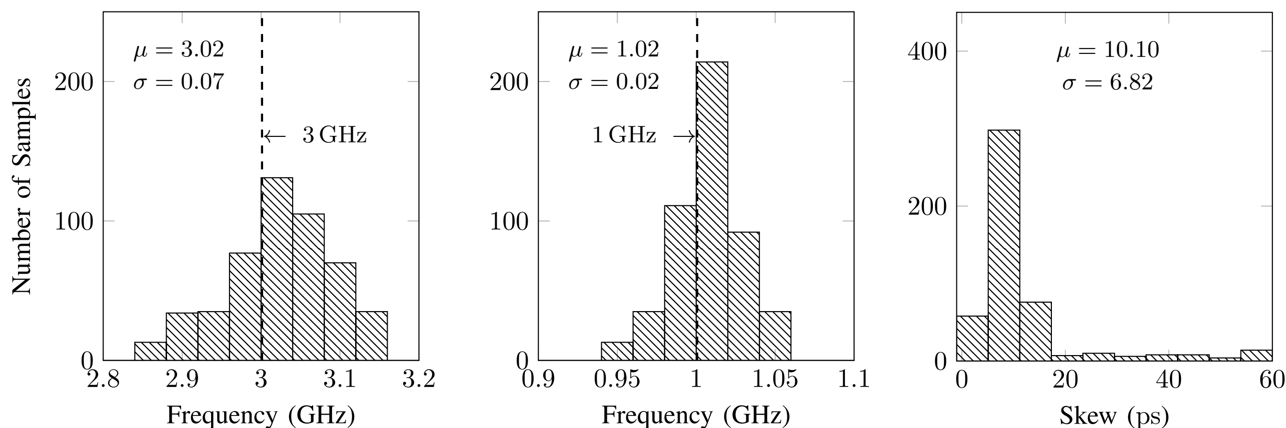
A. Power Consumption and Clock Skew

The power consumption of the ReRoC as compared to a PLL operating at 1 GHz is listed in Table III. The PLL-based design is implemented with a standard cell library from a 28 nm technology node using Cadence Innovus. Each die in the multi-die module includes one PLL to synchronize the multiple M0 cores. The power consumptions listed in Table III are 1) the power consumed only by the PLL of each die $PLL_{clock/die}$ and 2) the power consumed by the cores and clock network in each die $PLL_{core/die}$. The power consumed by the clock $PLL_{clock/mds}$ and the total power consumption $PLL_{core/mds}$ of the multi-die system are also listed in Table III.

A total power savings of approximately 40% is achieved for the multi-die system (`AI-ROA`$_{core/mds}$) when compared against a PLL clocked multi-die system ($PLL_{core/mds}$) for the 10 mm × 10 mm MDS. The clock power savings are significant for the clocks on the multi-die system: approximately 72% power savings (`AI-ROA`$_{clock/mds}$) when compared against a PLL based design ($PLL_{clock/mds}$) for the design dimension of 10 mm × 10 mm. The average clock skew for the MDS is 8.3 ps under nominal operating conditions. The ReRoCs provide a low power clock generation and distribution solution for multi-die systems in comparison to PLL based designs, providing a 40% total power savings due to the 72% reduction in the power consumption of the clock.

B. Variation Analysis

The design parameters discussed in Section III-C are varied for 500 Monte-Carlo simulations on post-layout models of the multi-die system. The σ_{V_t} is varied by 60 mV along with ±10% variations in the geometries of the ReRoCs and supply voltage. The temperature is varied from –40°C to 125°C for the analysis. The core load for the clock distribution network is modeled as *RC* elements. The frequency variation of the AI-ROA before frequency division [Fig. 4(a)], after frequency division [Fig. 4(b)], and the variation in clock skew [Fig. 4(c)] across the 10 mm×10 mm MDS are shown in Figure 4. The σ_{V_t} variation of 60 mV for the ReRoCs with geometric variations of ±10% is intentionally large to determine the robustness of the circuit implementing the AI-ROA. The interlocking of the transmission lines in the AI-



(a) Output of the 3 GHz ReRoC placed in the active interposer

(b) Output of the resonant frequency dividers with a target frequency of 1 GHz

(c) Worst case skew

Fig. 4: Frequency and skew variation for the AI-ROAs distributed over $10\,\mathrm{mm} \times 10\,\mathrm{mm}$ area in the active silicon interposer driving 4 dies each having 16 CORTEX M0 cores under variations.

ROA mitigate variations in the σ_{V_t} of the inverter pairs. The largest frequency variation observed in the AI-ROA is approximately $150\,\mathrm{MHz}$, which is a 5% variation from the target frequency of $3\,\mathrm{GHz}$. The variations in the core load within the multi-die systems have significant affect on the clock skew, approximately $60\,\mathrm{ps}$ in the worst case. This is mainly due to the PVT variation of the core load. However, note that the variation in clock skew due to PVT variation is less than 10% of the desired clock frequency. The improved clock skew is due to the unbuffered steiner clock trees in the clock distribution network, unlike traditional buffered clock trees. Under nominal operating conditions, the clock skew is within 1% of the clock frequency as listed in Table III.

V. Conclusion

In this work, a multi-die system is synchronized with resonant rotary clocks to generate one clock domain across the entire package. The proposed architecture is evaluated on two different sized dies and characterized for power consumption and robustness against variations under different conditions. The multi-die system, that includes CORTEX M0 cores, with dimensions of $10\,\mathrm{mm} \times 10\,\mathrm{mm}$ implementing the AI-ROA achieves an average reduction in the total power of 40% as compared to a PLL based system due to an average power savings of 72% on the clock network. The largest variation in frequency observed for the AI-ROA is approximately $150\,\mathrm{MHz}$, which is a 5% deviation from the target frequency of $3\,\mathrm{GHz}$.

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