

Jianchao Lu

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RESEARCH INTERESTS Electronic Design Automation (EDA) of Clock Network Synthesis including Clock Tree/Mesh Synthesis and Resonant Clocking; Static Timing Analysis; Clock Skew Scheduling; VLSI Physical Design in General including Floorplan, Placement and Routing; Parallel Computing.

- EDUCATION
- ◇ **Ph.D., Computer Engineering**, June 2011 (Expected).
Drexel University, Philadelphia, PA.
Advisor: Dr. Baris Taskin
 - ◇ **M.S., Computer Engineering**, December 2009.
Drexel University, Philadelphia, PA.
 - ◇ **B.S., Electronics and Information Engineering**, June 2007.
Zhejiang University, Hangzhou, China.

- PROFESSIONAL EXPERIENCE
- ◇ **Research Assistant**, VLSI Laboratory, Drexel University. (08/2007 – Current)
 - Clock network synthesis using mesh structure with reduced power dissipation.
 - Clock buffer polarity assignment for on chip peak current reduction.
 - Routing methodology for Rotary Oscillator Arrays (ROA).
 - Clock skew scheduling and static timing analysis.
 - ◇ **Teaching Assistant**, Drexel University. (08/2007 – Current)
 - ECEC 490/690, VLSI Design Courses Series, undergraduate/graduate levels.
 - ECEC 203, Programming for Engineers, undergraduate level.
 - ECE L301, ECE Laboratory, undergraduate level.
 - ◇ **Software Development Engineer (Intern)**, Gedae Inc., Morrestown, NJ. (06/2008 – 07/2009)
 - Multi-core, multi-processor compiler design for multiple computer architectures and operating systems.
 - Designed board support package for the multi-core processor compiler to operate on IBM Blue Gene/P super server (Parallel C programming using MPI).
 - Upgraded applications on Blue Gene/P super server using IBM Engineering Scientific Subroutine Library (ESSL) (C programming).
 - Upgraded applications on Curtiss Wright CHAMP-AV6 digital signal processor using Continuum Vector DSP Library (C programming).
 - Tested the compiler on multiple architectures including Cell BE, Blue Gene, X86 and Curtiss Wright CHAMP-AV6 (Perl programming).

PUBLICATIONS **Journals**

- [J3] J. Lu, Y. Teng and B. Taskin, “A Reconfigurable Clock Polarity Assignment Flow for Clock Gated Designs”, submitted to IEEE Transactions on Very Large Scale Integration (TVLSI) Systems (Under review).
- [J2] J. Lu and B. Taskin, “Clock Buffer Polarity Assignment with Skew Tuning”, submitted to ACM Transactions on Design Automation of Electronic Systems (TODAES) (First revision).
- [J1] J. Lu and B. Taskin, “Post-CTS Delay Insertion”, *Journal of VLSI Design*, Article 451809, vol. 2010, February 2010.

Conferences

- [C10] J. Lu, X. Mao, and B. Taskin, "Timing Slack Aware Incremental Register Placement with Non-uniform Grid Generation for Clock Mesh Synthesis", *under review*.
- [C9] J. Lu, Y. Aksehir and B. Taskin, "Register On MESH (ROME): A Novel Approach for Clock Mesh Network Synthesis", *submitted to IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2011.
- [C8] J. Lu and B. Taskin, "Reconfigurable Clock Polarity Assignment for Peak Current Reduction of Clock-gated Circuits", *submitted to IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2011.
- [C7] J. Lu, V. Honkote, X. Chen, and B. Taskin, "Steiner Tree Based Rotary Clock Routing with Bounded Skew and Capacitive Load Balancing", *to appear in the Proceedings of the Design, Automation and Test in Europe (DATE)*, March 2011.
- [C6] V. Honkote, A. More, Y. Teng, J. Lu and B. Taskin, "Interconnect Modeling, Synchronization and Power Analysis for Custom Rotary Rings", *to appear in the Proceedings of the International Conference on VLSI Design (VLSID)*, January 2011.
- [C5] J. Lu and B. Taskin, "Clock Tree Synthesis with XOR Gates for Polarity Assignment", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2010.
- [C4] J. Lu and B. Taskin, "Clock Buffer Polarity Assignment Considering Capacitive Load", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2010.
- [C3] J. Lu and B. Taskin, "Incremental Register Placement for Low Power CTS", *Proceedings of the IEEE International SoC Design Conference (ISOCC)*, November 2009.
- [C2] J. Lu and B. Taskin, "Post-CTS Clock Skew Scheduling with Limited Delay Buffering", *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2009.
- [C1] B. Taskin and J. Lu, "Post-CTS Delay Insertion to Fix Timing Violations", *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2008.

PROFESSIONAL ACTIVITIES ◇ Student coordinator for ACM Special Interest Group on Design Automation (SIGDA) University Booth at Design Automation Conference (DAC) 2009.

- ◇ Participated in SIGDA/DAC University Booth 2010 and 2009.
- ◇ Participated in ACM/SIGDA CADathlon programming contest at International Conference on Computer-Aided Design (ICCAD) 2009 and 2008.
- ◇ Reviewed papers for IEEE International Conference on VLSI Design (VLSID), 2010; IEEE Midwest Symposium on Circuits and Systems (MWSCAS), 2010.

SKILLS ◇ C++/C (Proficient), Perl (Proficient), Shell Scripting, Tcl, Java

- ◇ Cadence – Virtuoso Suite, Spectre, Calibre
- ◇ Mentor – HDL Designer, Modelsim
- ◇ Synopsys – Design Compiler, IC Compiler, Astro, StarRCXT, PrimeTime, Nanosim, HSPICE
- ◇ Xilinx – Spartan 3, Virtex 5
- ◇ VHDL, Verilog HDL
- ◇ Matlab, CPLEX, GLPK, LPSolve
- ◇ Latex, XEmacs, vi, Office Suites
- ◇ Unix, Linux, VxWorks, Mac OS, Windows, DOS

GRADUATE COURSE-
WORK ◇ EDA for VLSI circuits, Deep Sub-Micron IC Design, VLSI Design, VLSI Array Processors, Data Structure and Algorithms, Approximation Algorithms, Computer Architecture, Parallel Computer Architecture.