Ragh Kuttappa

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Education

Ph.D., Electrical Engineering, GPA: 3.95 (expected graduation 2019)
Drexel University, Philadelphia, PA.

M.S., Electrical and Computer Engineering, GPA: 3.8 August 2015
San Francisco State University, San Francisco, CA.

B.E., Electronics and Communication, GPA:3.5 July 2012
Visvesvaraya Technological University, Karnataka, India.

Professional Experience

Ph.D. Candidate, September 2015 - present
VLSI and Architecture Laboratory, Drexel University
Advisor: Dr. Baris Taskin

- Development of custom back-end automation flow for resonant rotary clocks using Cadence EDI.
- Custom methodology for frequency division of resonant clocks (MHz to GHz).
- Physical digital design and optimization of resonant and PLL-based designs.
  -Floorplan, Placement, Clock tree Synthesis and Routing of resonant-based circuits (DRC, LVS, PEX and HFSS modeling for transmission lines).
- Power distribution for resonant clocks and PLL-based designs.
- Design of transistor level and gate level low power circuits using cadence suite.
- Implementation of Verilog-A models for emerging optoelectronic components for CMOS integration.
- **Chip tapeout experience**: Resonant clocking technology for high speed frequency division in the 65nm technology node for research (1.5mm*1.5mm).

Ph.D. Intern, Samsung Austin Research Center (SARC) April 2017 - Sept. 2017
CAD Internship

- Standard cell characterization and timing correlation.
- Sign-off for latest CPU, RTL to GDSII.
- Metal stack evaluation for lower process nodes.

Masters Student, August 2013 - August 2015
Nano-electronics and Computing Research Laboratory, San Francisco State University
Advisor: Dr. Hamid Mahmoodi

- Reliability Analysis of Spin Transfer Torque (STT) based circuits.
- Low power design methodologies for reconfigurable logic using Look Up Tables (LUT).
- Developed circuit architectures for reconfigurable STT based LUTs.
- Thesis: Circuit Reliability Analysis under Variations in Nano-Scale CMOS.

Publications

- Ragh Kuttappa and Baris Taskin, "Low Frequency Rotary Traveling Wave Oscillators", in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018.

- Ragh Kuttappa, Baris Taskin, Lunal Khuon and Bahram Nabet, "Optoelectronic Capacitor Threshold Logic Gates", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)* - in review.
- Ragh Kuttappa, Leo Filippini, Scott Lerner and Baris Taskin, " Stability of Rotary Traveling Wave Oscillators under Process Variations and NBTI", in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2017.
- Ragh Kuttappa, Lunal Khuon, Bahram Nabet and Baris Taskin, "Reconfigurable Threshold Logic Gates using Optoelectronic Capacitors", in *Proceedings of the Design, Automation and Test in Europe (DATE),* March 2017.
- Ragh Kuttappa, Houman Homayoun, Hassan Salmani and Hamid Mahmoodi, "Comparative Analysis of Robustness of Spin Transfer Torque based Look Up Tables under Process Variations", in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016.
- Ragh Kuttappa, Houman Homayoun, Hassan Salmani and Hamid Mahmoodi, "Reliability Analysis of Spin Transfer Torque based Look up Tables under Process Variations and NBTI Aging", *Elsevier Microelectronics Reliability Journal*, March 2016.

Graduate Level Coursework

CMOS VLSI Design, Custom VLSI Design I/II, Advanced VLSI Design, Advanced Digital Design, Nano-Scale Circuits and Systems, Advanced Microprocessor Architecture, Parallel Computer Architecture.

Skills

- Synopsys - Custom Designer, Design Compiler, IC Compiler I/II, HSPICE, FineSim, PrimeTime; Cadence - Virtuoso Suite, Encounter, RTL Compiler, Spectre; Mentor: Calibre (DRC, LVS, PEX) ; Prog. Lang. - C, C++, Perl, TCL, SKILL, Verilog, VHDL

Teaching Assistant Coursework

- Computational Lab I/II, F'15 - W'16, F'17 - W'18 Freshman Level Class
- Analog Electronics Lab, F'15, Junior Level Class
- Micro-controller Design, W'16 - S'16, Winter 2018 Junior Level Class
- Digital Logic Design, S'16, F'16, Sophomore Level Class
- Digital Design Projects, S'16, Junior Level Class
- ASIC Design I/II, F'16 - W'17, Graduate Level Class
- Custom VLSI Design I, W'18, Graduate Level Class

References

- **Dr. Baris Taskin**
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  Drexel University, Philadelphia, PA
- **Dr. Ioannis Savidis**
  Assistant Professor, Department of Electrical and Computer Engineering
  e-mail: isavidis@coe.drexel.edu
  Drexel University, Philadelphia, PA
- **Dr. Hamid Mahmoodi**
  Professor, Department of Computer Engineering
  e-mail: mahmoodi@sfsu.edu
  San Francisco State University, San Francisco, CA