Ragh Kuttappa

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Education

Ph.D., Electrical Engineering, GPA: 3.97 (expected graduation 2020)
Drexel University, Philadelphia, PA.

M.S., Electrical and Computer Engineering, GPA: 3.8 August 2015
San Francisco State University, San Francisco, CA.

B.E., Electronics and Communication, GPA:3.5 July 2012
Visvesvaraya Technological University, Karnataka, India.

Professional Experience

Ph.D. Candidate, September 2015 - present
VLSI and Architecture Laboratory, Drexel University
Advisor: Dr. Baris Taskin

- Fast DVFS with resonant rotary clocks:
  -On-chip phase interleaved DC-DC voltage regulator design.
  -Fast switching DFS with resonant rotary clocks.
- Development of custom back-end automation flow for resonant rotary clocks operating from MHz to GHz frequency range.
- Physical digital design and optimization of resonant and PLL-based designs:
  -Power planning, Floorplan, Placement, Clock tree Synthesis and Routing of resonant-based circuits (DRC, LVS, PEX and HFSS modeling).
- Design of transistor level and gate level low power circuits using cadence suite.
- **Chip tapeout experience**: Resonant clocking technology for high speed frequency division in the 65nm technology node for research (1.5mm*1.5mm).

Ph.D. Intern, Samsung Austin Research Center (SARC) April 2017 - Sept. 2017
CAD Internship

- Standard cell characterization and timing correlation.
- Sign-off for latest CPU, RTL to GDSII.
- Metal stack evaluation for FinFET <10nm nodes.

Masters Student, August 2013 - August 2015
Nano-electronics and Computing Research Laboratory, San Francisco State University
Advisor: Dr. Hamid Mahmoodi

- Reliability Analysis of Spin Transfer Torque (STT) based circuits.
- Developed circuit architectures for reconfigurable STT based LUTs.
- Thesis: Circuit Reliability Analysis under Variations in Nano-Scale CMOS.

Selected Publications

1. Ragh Kuttappa, Adarsha Balaji, Vasil Pano, Baris Taskin, and Hamid Mahmoodi, "RotaSYN: Rotary Traveling Wave Oscillator SYNthesizer", *IEEE Transactions in Circuits and Systems I: Regular Papers* (TCAS - I), January 2019.
2. Ragh Kuttappa, Selçuk Köse, and Baris Taskin, "`FOPAC`: Flexible On-chip Power and Clock", *IEEE Transactions in Circuits and Systems I: Regular Papers* (TCAS - I) – Accepted July 2019.

3. Ragh Kuttappa, Baris Taskin, Scott Lerner, Vasil Pano, and Ioannis Savidis, "Robust Low Power Clock Synchronization for Multi-Die Systems", in *Proceedings of the IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, July 2019.
4. Vasil Pano, Ragh Kuttappa, and Baris Taskin, "3D NoCs with Active Silicon Interposer for Multi-Die Systems", in *Proceedings of the IEEE/ACM International Symposium on Networks-on-Chip (NOCs)*, October 2019.
5. Ragh Kuttappa, Scott Lerner, Leo Filipinni, and Baris Taskin, "Low–Swing and Low–Frequency Rotary Traveling Wave Oscillators", in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019.
6. Ragh Kuttappa and Baris Taskin, "FinFET-based Low Swing Rotary Traveling Wave Oscillators", *IEEE Transactions in Circuits and Systems II: Briefs* (TCAS - II) – in review.
7. Ragh Kuttappa, Longfei Wang, Selçuk Köse, and Baris Taskin, "Fast Switching Multiphase Resonant Digital Low-Dropout Regulator for On-Chip Noise Mitigation", *IEEE Transactions in Circuits and Systems I: Regular Papers* (TCAS - I) – in preparation.
8. Ragh Kuttappa and Baris Taskin, "Low Frequency Rotary Traveling Wave Oscillators", in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018.
9. Ragh Kuttappa et. al., " Stability of Rotary Traveling Wave Oscillators under Process Variations and NBTI", in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2017.
10. Ragh Kuttappa, Lunal Khuon, Bahram Nabet, and Baris Taskin, "Reconfigurable Threshold Logic Gates using Optoelectronic Capacitors", in *Proceedings of the Design, Automation and Test in Europe (DATE),* March 2017.
11. Ragh Kuttappa et. al., "Comparative Analysis of Robustness of Spin Transfer Torque based Look Up Tables under Process Variations", in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016.
12. Ragh Kuttappa et. al., "Reliability Analysis of Spin Transfer Torque based Look up Tables under Process Variations and NBTI Aging", *Elsevier Microelectronics Reliability Journal*, March 2016.

Graduate Level Coursework

CMOS VLSI Design, Custom VLSI Design I/II, Advanced VLSI Design, Advanced Digital Design, Nano-Scale Circuits and Systems, Advanced Microprocessor Architecture, Parallel Computer Architecture.

Selected Projects

Custom VLSI Design I: Design of 64x32 bit SRAM

- Design of full custom 64x32 bit SRAM schematic, layout, DRC, LVS and StarRc.
- Optimizing the design for speed, area, stability, dynamic and static power consumption.
- Optimized the circuit by smart controller logic design resulting in 1.8GHz clock frequency and 23% area reduction.

Custom VLSI Design II: On-chip two level power distribution network in IBM 180 nm technology

- Design of power distribution network while analyzing noise sources and techniques for noise reduction.

- Implementation of a two-level interdigitated grid topology and analysis of power distribution noise with switched decoupling capacitors.
- Power gating implemented and effect of noise on different local grids are studied.

ASIC Design: OpenSPARC Floating Point Unit

- Implemented a front end design flow which includes RTL Design and formal verification
- Back-end design included floor planning, maximum core utilization, effective clocking and powering schemes, fixation of violated timing using CTS model, worst and average case power estimation using Synopsys IC compiler.
- Inserted delay and global skew using STA Primetime.

Static Timing Analysis of ORCA using Synopsys Prime Time

- Analyzed a timing report from input and output ports for setup and hold and generated summary reports for the violations in ORCA.
- Debugged hold violation using SPEF parasitics.

Nano-scale Circuits and Systems: Spin Transfer Torque (STT) based Look up Tables (LUT) in Nano-scale CMOS

- Lookup table with 16nm CMOS technology using linear resistor model and characterized LUT in terms of standby power, read delay and power delay product (PDP).
- The highlights included implementing power reduction technique like Dual Vt and reducing gate level voltage.

Skills

- Synopsys - Custom Designer, Design Compiler, IC Compiler I/II, HSPICE, FineSim, PrimeTime; Cadence - Virtuoso Suite, Innovus, RTL Compiler, Spectre; Mentor: Calibre (DRC, LVS, PEX) ; Ansys - HFSS; Prog. Lang. - C, C++, Perl, TCL, SKILL, Verilog, VHDL

Teaching Assistant Coursework

- Computational Lab I/II– F'15 - W'16, F'17 - W'18 Freshman Level Class
- Analog Electronics Lab– F'15, Junior Level Class
- Micro-controller Design– W'16 - S'16, Winter 2018 Junior Level Class
- Digital Logic Design– S'16, F'16, Sophomore Level Class
- Digital Design Projects– S'16, Junior Level Class
- ASIC Design I/II– F'16 - W'17, W'19 - S'19, Graduate Level Class
- Custom VLSI Design I– W'18, Graduate Level Class

References

- **Dr. Baris Taskin**,
  Professor, ECE
  e-mail: taskin@coe.drexel.edu,
  Drexel University, Philadelphia, PA
- **Dr. Ioannis Savidis**,
  Associate Professor, ECE
  e-mail: isavidis@coe.drexel.edu,
  Drexel University, Philadelphia, PA
- **Dr. Hamid Mahmoodi**,
  Professor, EECS
  e-mail: mahmoodi@sfsu.edu,
  San Francisco State University, San Francisco, CA
- **Dr. Selçuk Köse**,
  Associate Professor, ECE
  email: selcuk.kose@rochester.edu,
  University of Rochester, Rochester, NY