

# Ragh Kuttappa

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- Education**
- Ph.D., Electrical Engineering**, GPA: 3.97 (in-progress)  
Drexel University, Philadelphia, PA.
  - M.S., Electrical and Computer Engineering**, GPA: 3.8 August 2015  
San Francisco State University, San Francisco, CA.
  - B.E., Electronics and Communication**, GPA:3.5 July 2012  
Visvesvaraya Technological University, Karnataka, India.
- Professional Experience**
- Ph.D. Candidate**, September 2015 - present  
VLSI and Architecture Laboratory, Drexel University  
Advisor: Dr. Baris Taskin
    - Physical digital design, automation, and optimization of resonant and PLL-based designs:
      - Power planning, Floorplan, Placement, Clock tree Synthesis and Routing of resonant-based circuits (DRC, LVS, PEX, STA PrimeTime, and HFSS modeling).
    - Fast switching DVFS with resonant rotary clocks and ASIC integration.
    - On-chip phase interleaved DC-DC voltage regulator design (SC, DLDO).
    - Multi-die integration for resonant clocks, voltage regulators, and high speed I/Os for 2.5/3D heterogeneous systems.
    - Power grid design, EMIR analysis, and Transmission Line modeling.
    - Design of transistor level and gate level low power circuits using cadence suite.
    - **Chip tapeout experience**: Resonant clocking technology for high speed frequency division in the 65nm technology node for research (1.5mm\*1.5mm).
  - Ph.D. Intern, Samsung Austin Research Center (SARC)** April 2017 - Sept. 2017  
CAD Internship
    - Standard cell characterization and timing correlation.
    - Sign-off for latest CPU, RTL to GDSII.
    - Metal stack evaluation for FinFET <10nm nodes.
  - Masters Student**, August 2013 - August 2015  
Nano-electronics and Computing Research Laboratory, San Francisco State University  
Advisor: Dr. Hamid Mahmoodi
    - Reliability Analysis of Spin Transfer Torque (STT) based circuits.
    - Developed circuit architectures for reconfigurable STT based LUTs.
    - Thesis: Circuit Reliability Analysis under Variations in Nano-Scale CMOS.
- Publications**
1. R. Kuttappa, B. Taskin, S. Lerner, and V. Pano, “Resonant Clock Synchronization with Active Silicon Interposer for Multi-Die Systems”, in *IEEE Transactions on Circuits and Systems I: Regular Papers* (TCAS - I) – February 2021.
  2. R. Kuttappa, A. Balaji, V. Pano, B. Taskin, and H. Mahmoodi, “RotaSYN: Rotary Traveling Wave Oscillator SYNthesizer”, *IEEE Transactions on Circuits and Systems I: Regular Papers* (TCAS - I), January 2019.

3. R. Kuttappa, S. Köse, and B. Taskin, “FOPAC: Flexible On-chip Power and Clock”, *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS - I)* – December 2019.
4. R. Kuttappa, L. Wang, S. Köse, and B. Taskin, “Multiphase Digital Low-Dropout Regulator for On-Chip Noise Mitigation”, *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS - I)* – in review.
5. R. Kuttappa and B. Taskin, “FinFET–Based Low Swing Rotary Traveling Wave Oscillators”, in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, October 2020.
6. R. Kuttappa, S. Khoa, L. Filippini, V. Pano, and B. Taskin, “Comprehensive Low Power Adiabatic Circuit Design with Resonant Power Clocking”, in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, October 2020.
7. K. Sangaiah, M. Lui, R. Kuttappa, M. Hempstead, and B. Taskin, “SnackNoc: Processing in the Communication Layer”, *Proceedings of the IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, February 2020.
8. K. Sangaiah, R. Kuttappa, V. Pano, B. Taskin, and M. Hempstead, “In-Network Processing for Multi-Die Systems”, *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, July 2021 – in review.
9. R. Kuttappa, B. Taskin, S. Lerner, V. Pano, and I. Savidis, “Robust Low Power Clock Synchronization for Multi-Die Systems”, in *Proceedings of the IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, July 2019.
10. V. Pano, R. Kuttappa, and B. Taskin, “3D NoCs with Active Silicon Interposer for Multi-Die Systems”, in *Proceedings of the IEEE/ACM International Symposium on Networks-on-Chip (NOCs)*, October 2019.
11. L. Wang, R. Kuttappa, B. Taskin, and S. Köse, “Distributed Digital Low-Dropout Regulators with Phase Interleaving for On-Chip Voltage Noise Mitigation”, in *Proceedings of the IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2019.
12. R. Kuttappa, S. Lerner, L. Filippini, and B. Taskin, “Low–Swing and Low–Frequency Rotary Traveling Wave Oscillators”, in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019.
13. R. Kuttappa and B. Taskin, “Low Frequency Rotary Traveling Wave Oscillators”, in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018.
14. R. Kuttappa, S. Lerner, L. Filippini, and B. Taskin, “Stability of Rotary Traveling Wave Oscillators under Process Variations and NBTI”, in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2017.
15. R. Kuttappa, L. Khuon, B. Nabet, and B. Taskin, “Reconfigurable Threshold Logic Gates using Optoelectronic Capacitors”, in *Proceedings of the Design, Automation and Test in Europe (DATE)*, March 2017.
16. R. Kuttappa et. al., “Comparative Analysis of Robustness of Spin Transfer Torque based Look Up Tables under Process Variations”, in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016.
17. R. Kuttappa et. al., “Reliability Analysis of Spin Transfer Torque based Look up Tables under Process Variations and NBTI Aging”, *Elsevier Microelectronics Reliability Journal*, March 2016.

**Graduate Level Coursework** CMOS VLSI Design, Custom VLSI Design I/II, Advanced VLSI Design, Advanced Digital Design, Nano-Scale Circuits and Systems, Advanced Microprocessor Architecture, Parallel Computer Architecture.

**Skills**

- Synopsys - Custom Designer, Design Compiler, IC Compiler I/II, HSPICE, FineSim, PrimeTime; Cadence - Virtuoso Suite, Innovus, RTL Compiler, Spectre; Mentor: Calibre (DRC, LVS, PEX) ; Ansys - HFSS; Prog. Lang. - C/C++, Python, Perl, TCL, SKILL, Verilog, VHDL

**References**

- **Dr. Baris Taskin**,  
Professor, ECE  
e-mail: taskin@coe.drexel.edu,  
Drexel University, Philadelphia, PA
- **Dr. Hamid Mahmoodi**,  
Professor, EECS  
e-mail: mahmoodi@sfsu.edu,  
San Francisco State University, CA
- **Dr. Ioannis Savidis**,  
Associate Professor, ECE  
e-mail: isavidis@coe.drexel.edu,  
Drexel University, Philadelphia, PA
- **Dr. Selçuk Köse**,  
Associate Professor, ECE  
email: selcuk.kose@rochester.edu,  
University of Rochester, Rochester,  
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