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Leo Filippini

Summary I am a PhD student focusing on low-power VLSI systems, with a strong background in analog IC design and layout: for the past two years I've been designing CMOS circuits in deep-submicron technologies. I have cleanroom and tapeout experience and a sound understanding of transistor level design and device physics.

Education

2010 – 2013 **Master Degree**, *University of Brescia*, Brescia (Italy), *summa cum laude*.
Electronics Engineering

2006 – 2010 **Bachelor Degree**, *University of Brescia*, Brescia (Italy), *91/110*.
Information Engineering

Experience

2013 - present **PhD candidate**, *Drexel University*, Philadelphia (PA).
My research group focuses on low-power methodologies for VLSI circuits. In particular, I am currently investigating flip-flop topologies for low-swing clock applications along with the feasibility of different adiabatic logic families.

2013 **Intern**, *Imec*, Heverlee (Belgium).
For my Master's thesis I spent six months designing an integrated transimpedance amplifier for capacitive ultrasonic transducers (CMUT).
Detailed achievements:
- Implementation of the transducer model in Cadence
- Noise analysis
- Design of a topology new to the application
- Tape-out in CMOS 180nm

2010 **Intern**, *University of Brescia – Physics Department*, Brescia (Italy).
For four months I worked on my Bachelor's thesis: *Synthesis and integration of quantum dot semiconductors in third generation excitonic solar cells.* Along with my supervisors, we chemically synthesized different types of quantum-dots and realized many cells. I, in particular, took care of the substrate deposition and characterization, of the construction of the cells, and of their optical and electrical characterization.

Computer skills

EDA Virtuoso, Custom Designer, ADS, Encounter, DC, ICC

Languages Matlab, Python, Mathematica, LaTeX, Objective-C, Bash

Languages

Italian Native

English TOEFL iBT: 107/120

Publications & Honors

2014 Can Sitik, Leo Flippini, Emre Salman, and Baris Taskin, *"High Performance Low Swing Clock Tree Synthesis with Custom D Flip-Flop Design"*, ISVLSI 2014

2011 Winner of European *Lifelong Learning Program* scholarship