3141 Chestnut St
Drexel University – ECE Dept
Philadelphia, PA 19104
☎ +1 267 439 5485
✉ leo.filippini@posteo.org
vlsi.ece.drexel.edu

Leo Filippini

Summary I am a PhD candidate focusing on charge recovery logic and novel low-power data converters, with a background in analog integrated circuits design. I have experience across the CMOS flow: design and tapeout, cleanroom, and device characterization. Moreover, I have experience in writing proposals for NSF research grants.

Education

2013 - Present **PhD candidate**, *Drexel University*, Philadelphia (PA).
Electronics Engineering

2010 - 2013 **Master Degree**, *University of Brescia*, Brescia (Italy), *summa cum laude*.
Electronics Engineering

2011 **Visiting Student**, *Koç University*, Istanbul (Turkey).
Electronics Engineering

2006 - 2010 **Bachelor Degree**, *University of Brescia*, Brescia (Italy).
Information Engineering

Research

2013 - Present **Research Assistant**, *Drexel University*, Philadelphia, PA (USA).
Charge Recovery Logic, CRL, also known as adiabatic logic, is a logic style that aims at reducing energy consumption by recycling, or recovering, part of the charge that flows through a logic gate. My current research, under the guidance of Professor Baris Taskin, is focused on i) transposing charge recovery principles to mixed-signal circuits and ii) developing a logic synthesis methodology for charge recovery logic. The prototype of a charge recovery analog to digital converter in 65 nm CMOS is currently being fabricated, and an NSF grant proposal that I co-wrote, CCF 1816857, was recently awarded $400,000 for the development of a logic synthesis tool for charge recovery logic.

2013 **Intern**, *IMEC*, Heverlee (Belgium).
As an intern at IMEC, I worked on my Master's thesis under the direction of Dr. Firat Yazicioglu. My responsibilities were the design of an integrated transimpedance amplifier for capacitive ultrasonic transducers (CMUT). In particular, I i) modeled the sensor in Cadence Virtuoso and studied its noise behavior, ii) surveyed the noise profile of several amplifier topologies, iii) designed a topology new to the application, and iv) taped-out a prototype IC in CMOS 180nm.

2010 **Intern**, *University of Brescia – Physics Department*, Brescia (Italy).
I assisted Professor Isabella Concina and Professor Alberto Vomiero to chemically synthesize different types of quantum-dots to integrate in excitonic solar cells. I, in particular, took care of the substrate deposition and characterization, of the construction of the cells, and of their optical and electrical characterization.To do so, I used the following instruments: electronic load with 4-point probe, solar simulator, monochromator, lock-in amplifier.

Teaching & Advising

2013 - Present **Teaching Assistant**, *Drexel University*, Philadelphia, PA (USA).
I have been the laboratory instructor for several undergraduate classes: Digital Electronics, Advanced Electronics I, Analog Electronics, and Electronic Devices.

2017 **Instructor**, *Drexel University*, Philadelphia, PA (USA).
I was one of two instructors for *Advanced Electronics I*, a class focusing on analog design for integrated circuits. I was the lecturer for the first half of the course, in which I developed lecture material to cover topics from operational amplifiers to the cascode configuration.

2015 & 2017 **Visiting Student Advisor**, *Drexel University*, Philadelphia, PA (USA).
I was the advisor for two visiting Master students in 2015 and in 2017, working on the layout of a charge recovery logic ASIC and on logic synthesis for charge recovery logic, respectively.

2016 - 2017 **Senior Design Project Advisor**, *Drexel University*, Philadelphia, PA (USA).
I, along with two faculty members, advised one of the senior design teams of academic year 16/17. The project, tackling implantable EEG recording in mice, focused on wirelessly powered solutions using charge recovery logic.

Publications

[1] L. Filippini and B. Taskin, "The adiabatically driven strongarm comparator," *(under review) IEEE Transactions on Circuits and Systems II*, Jun. 2018.

[2] L. Filippini and B. Taskin, "A 900 MHz charge recovery comparator with 40 fJ per conversion," in *(to appear) Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2018.

[3] L. Filippini, L. Khuon, and B. Taskin, "Charge recovery implementation of an analog comparator: Initial results," in *Proc. IEEE 60th Int. Midwest Symp. Circuits and Systems (MWSCAS)*, Aug. 2017, pp. 1505–1508. DOI: 10.1109/MWSCAS.2017.8053220.

[4] L. Filippini and B. Taskin, "A charge recovery logic system bus," in *Proc. ACM/IEEE Int. Workshop System Level Interconnect Prediction (SLIP)*, Jun. 2017, pp. 1–4. DOI: 10.1109/SLIP.2017.7974909.

[5] R. Kuttappa, L. Filippini, S. Lerner, and B. Taskin, "Stability of rotary traveling wave oscillators under process variations and NBTI," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2017, pp. 1–4. DOI: 10.1109/ISCAS.2017.8050435.

[6] L. Filippini, D. Lim, L. Khuon, and B. Taskin, "Wireless charge recovery system for implanted electroencephalography applications in mice," in *Proc. 18th Int. Symp. Quality Electronic Design (ISQED)*, Mar. 2017, pp. 342–345. DOI: 10.1109/ISQED.2017.7918339.

[7] L. Filippini and B. Taskin, "Charge recovery logic for thermal harvesting applications," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2016, pp. 542–545. DOI: 10.1109/ISCAS.2016.7527297.

[8] L. Filippini, E. Salman, and B. Taskin, "A wirelessly powered system with charge recovery logic," in *Proc. 33rd IEEE Int. Conf. Computer Design (ICCD)*, Oct. 2015, pp. 505–510. DOI: 10.1109/ICCD.2015.7357158.

[9] C. Sitik, E. Salman, L. Filippini, S. J. Yoon, and B. Taskin, "FinFET-based low-swing clocking," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, vol. 12, no. 2, p. 13, 2015.

[10] C. Sitik, L. Filippini, E. Salman, and B. Taskin, "High performance low swing clock tree synthesis with custom D flip-flop design," in *Proc. IEEE Computer Society Annual Symp. VLSI*, Jul. 2014, pp. 498–503. DOI: 10.1109/ISVLSI.2014.53.