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RESEARCH INTERESTS

Electronic Design Automation (EDA) for VLSI, High-Performance Circuits, Resonant Clocking, Clock Network Synthesis, Wireless IC Interconnects and Networks-on-Chip (NoC) for Chip Multi-Processors (CMPs).

EDUCATION

- **Ph.D, Electrical Engineering**, July 2005.
  University of Pittsburgh, Pittsburgh, PA
- **M.S., Electrical Engineering**, May 2003.
  University of Pittsburgh, Pittsburgh, PA
- **B.S., Electrical and Electronics Engineering**, June 2000.
- **Minor Program Diploma, Operations Research**, June 2000.
  Middle East Technical University, Ankara, Turkey

PROFESSIONAL EXPERIENCE

- **Associate Professor**, (09/2011 – current)
  Assistant Professor, (09/2005 – 08/2011)
  Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  – Founded Drexel VLSI Laboratory [*http://vlsi.ece.drexel.edu*], 2006.
  – Graduate level teaching/course development: EDA for VLSI Circuits I & II, Deep Sub-Micron IC Design.
  – Undergraduate/graduate level: Custom VLSI Design, ASIC Design I, ASIC Design II.
  – Graduate level: Network-on-Chip Design I, Network-on-Chip Design II.
- **Full-time Engineer**, (09/2003 – 06/2004)
  MultiGiG Inc., Scotts Valley, CA [now Analog Devices, Inc.]
  – Synchronization and timing specification of the resonant "rotary" clocking technology.
- **Teaching Fellow**, (01/2005 – 05/2005)
  Teaching/Research Assistant, (09/2000 –09/2003, 06/2004 – 01/2005)
  ECE 1192/2192 Introduction to VLSI Design, undergraduate/graduate levels,
  ECE 1193/2193 Advanced VLSI Design, undergraduate/graduate levels,
  – Received a research grant from MultiGiG Inc. for thesis work entitled *"Circuit Design and CAD Issues in the Design and Use of Synchronous Digital Circuits with Oscillatory Clock Arrays"*. Duration: 2004–2005
  Department of Electrical and Computer Engineering
  University of Pittsburgh, Pittsburgh, PA

ACADEMIC HONORS AND AWARDS

- "Young Engineer of the Year", Institute of Electrical and Electronics Engineers (IEEE) Philadelphia Section, 2013.
- Best paper nomination at ACM International Great Lakes Symposium on VLSI (GLSVLSI) 2013 held in Paris, France.
- "Distinguished Service Award", Association for Computing Machinery (ACM) Special Interest Group on Design Automation (SIGDA), 2012.

◇ "Faculty Early Career Development (CAREER)" award, National Science Foundation, 2009.

◇ "A. Richard Newton Graduate Scholarship" award for junior faculty starting new programs in EDA, ACM/IEEE Design Automation Conference (DAC) 2007.

◇ "Student Leadership Award", Student Government Board, University of Pittsburgh, 2005.

◇ "SOC Design Certificate", 2003, from Pittsburgh Digital Greenhouse, Pittsburgh, PA, for having successfully completed the program developed jointly by University of Pittsburgh, Pittsburgh, PA, Carnegie Mellon University, Pittsburgh, PA, Pennsylvania State University, University Park, PA, and Pittsburgh Digital Greenhouse, Pittsburgh, PA.

PROFESSIONAL ACTIVITIES

◇ **Editorship**

– Associate Editor, *Journal of Circuits, Systems and Computers (JCSC), 2012–current*

◇ **Organization Committee Member**

– *Finance Chair*, International Symposium on Circuits and Systems (ISCAS), 2017
– *Publicity Chair*, International Symposium on Low Power Electronic Design (ISLPED), 2014
– *Finance Chair*, International Workshop on System Level Interconnect Prediction (SLIP), 2014
– *Organizing Committee Member*, NSF CISE REU PI Meeting, 2013
– *Panel Chair*, International Workshop on System Level Interconnect Prediction (SLIP), 2013
– *Publicity Chair*, International Workshop on System Level Interconnect Prediction (SLIP), 2012
– *Finance Chair*, IFIP/IEEE International on Very Large Scale Integration (VLSI-SOC), 2012
– *Academic Coordinator*, ACM Special Interest Group on Design Automation (SIGDA) University Booth at DAC, 2008, 2009, 2010, 2011, 2012, 2013
– *Local Arrangements Chair*, ACM Great Lakes Symposium on Very Large Scale Integrated Circuits (GLSVLSI), 2006

◇ **Technical Program Committee Member**

–IEEE International Conference on Computer-Aided Design (ICCAD), 2012, 2013
–ACM Great Lakes Symposium on Very Large Scale Integrated Circuits (GLSVLSI), 2008, 2009, 2010, 2011, 2012, 2013
–ACM System Level Interconnect Prediction (SLIP), 2012, 2013
–IEEE International Conference on Computer Design (ICCD), 2010, 2012
–IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), 2009, 2010
–IEEE/ACM Asia Symposium on Quality Electronic Design (ASQED), 2010, 2011
–IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2008
–IEEE International Conference on Modeling, Simulation and Applied Optimization (ICMSAO), 2008
–EuroMicro Conference on Digital System Design (DSD), 2011, 2013
–IEEE Microelectronics Systems Education (MSE) Conference, 2011, 2013
–First International Workshop on Future Computing Technologies, 2006

◇ **Steering Committee Member**

– IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2007–current

◇ **Track Chair**

– IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), "CAD" track, 2009, 2010
– IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), "VLSI" track co-chair, 2008

◇ **Session Chair**

– *Wireless Interconnects in Network-on-Chips panel organizer and moderator*, SLIP 2013
– *Circuit Design & Optimization*, IEEE International Symposium on Circuits and Systems (ISCAS) 2011
– *Power and Thermal Analysis and Optimization*, IEEE ICCD 2010
– *Emerging Technologies*, IEEE GLSVLSI 2010
– *Clocking Strategy for Modern Low Power Multi-Core and Structured ASICs*, IEEE International Conference on Quality Electronic Design (ISQED) 2010
– IEEE NANOARCH 2009
– *CAD and Layout*, IEEE MWSCAS 2009

– *SOC Design*, IEEE MWSCAS 2008
– *VLSI Architectures*, IEEE MWSCAS 2007, 2008
– *Digital Circuits Design*, IEEE MWSCAS 2006, 2007

◇ **Reviewer**
– IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2003, 2008, 2010, 2011, 2012, 2013; IEEE Transactions on Computer-Aided Design (CAD), 2010, 2011,2012, 2013; IEEE Transactions on Nanotechnology, 2011; IEEE Journal of Emerging and Selected Topics in Circuits and Systems (JETCAS), 2011; IEEE Transactions on Education, 2007, 2012; ACM Transactions on Design and Automation of Electronic Systems (TODAES), 2007, 2008, 2011, 2012, 2013; ACM Journal of Emerging Technologies (JETC) 2008, 2009, 2010, 2012, 2013; IEEE Journal of Emerging and Selected Topics in Circuits and Systems (JETCAS), 2011; Journal of Nanomaterials and Nanotechnology, 2011; International Journal of Computers and Applications, 2011; IET Circuits, Devices & Systems 2013; IET Computers & Digital Techniques, 2011; IET Electronic Letters, 2010; ACM/IEEE International Symposium on Nanoscale Architectures (NANOARCH) 2009; Elsevier Integration, the VLSI Journal, 2010; Elsevier Microelectronics Journal, 2008, 2010; IEEE International Conference on VLSI Design (VLSID), 2008; IEEE GLSVLSI 2008, 2009; Journal of Zheijang University, 2010; Kuwait Journal of Science and Engineering, 2010; Gazi University Journal, 2006; National Science Foundation (NSF), 2006, 2008, 2010, 2011, 2012; Villanova University, 2011; IEEE International Symposium on VLSI (ISVLSI), 2007, 2009; IEEE Transactions on Nanotechnology, 2007, 2008, 2010, 2011; European Conference on Circuit Theory and Design (ECCTD), 2009, Spring Publishers, 2006; IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2006, 2010; International Journal of Computers and Their Applications (J. Comp.), 2005, 2006, 2011; IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2004; ACM/IEEE International Workshop on Timing Issues (TAU), 2004; IEEE International Symposium on Circuits and Systems (ISCAS), 2004

EDUCATIONAL INITIATIVES AND ACCOMPLISHMENTS

◇ **Academic Coordinator**, NSF-funded REU Site on "Computing for Power and Energy: The Old, The New and The Renewable", 2010–2013.

◇ **Course Development**, Network-on-Chip Design I, Network-on-Chip Design II – Graduate level courses, developed in AY 2013–2014.

◇ **Course Development**, Introduction to VLSI Design, ASIC Design I, ASIC Design II – Senior level undergraduate/graduate courses, developed in AY 2007–2008.

◇ **Course Development**, EDA for VLSI Circuits I, EDA for VLSI Circuits II, Deep Sub-Micron Integrated Circuit Design – Graduate level courses, developed in AY 2005–2006.

◇ **SIGDA University Booth at DAC** participation by senior design project group, J. DeMaio, O. Farell, M. Hazeltine and R. Ketner, 2007.

◇ **ECE Senior Design Award** as advisor to C. Weingarten and E. Fargnoli, 2010, Drexel University ECE Department.

◇ **ECE Senior Design Award** as advisor to J. DeMaio, O. Farell, M. Hazeltine and R. Ketner, 2007, Drexel University ECE Department.

UNIVERSITY AND DEPARTMENTAL SERVICE

◇ Drexel Centralized Research Facilities advisory committee, 2013–current

◇ ECE awards committee chair, 2013–current

◇ ECE awards committee, 2012–2013

◇ Computer Engineering curricular chair (interim), 2011–2012

◇ Computer Engineering faculty search committee, 2011–2013

◇ Boren Scholarship campus review committee, 2012–2013

◇ Fullbright scholarship campus review committee, 2011–2012

PUBLICATIONS

Books and Book Chapters

[B2] I. S. Kourtev, B. Taskin and E. G. Friedman, *Timing Optimization through Clock Skew Scheduling*, Springer, 2009.

[B1] B. Taskin, I. S. Kourtev and E. G. Friedman, *System Timing*, Handbook of VLSI, 2^{nd} edition, Editor: W. K. Chen, CRC Publishing, December 2006.

Journal Publications

[J15] V. Honkote and B. Taskin, "ZeROA: Zero Clock Skew Rotary Oscillatory Array", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, Vol. 20, No. 8, pp. 1528–1532, August 2012.

[J14] J. Lu, Y. Teng and B. Taskin, "A Reconfigurable Clock Polarity Assignment Flow for Clock Gated Designs", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, Vol. 20, No. 6, pp. 1002–1011, June 2012.

[J13] J. Lu, X. Mao and B. Taskin, "Integrated Clock Mesh Synthesis with Incremental Register Placement", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 31, No. 2, pp. 217–227, February 2012.

[J12] J. Lu and B. Taskin, "Clock Buffer Polarity Assignment with Skew Tuning", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 16, No. 4, Article 49, October 2011.

[J11] V. Honkote and B. Taskin, "CROA: Design and Analysis of Custom Rotary Oscillatory Array", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, Vol. 19, No. 10, pp. 1837–1847, October 2011.

[J10] S. M. Kurtas and B. Taskin, "Statistical Timing Analysis of the Clock Period Improvement through Clock Skew Scheduling", *International Journal of Circuits, Systems and Computers (JCSC)*, Vol. 20, No. 5, pp. 1–18, 2011.

[J9] K. Yencha, M. Zofchak, D. Oakum, G. Strait, B. Taskin, B. Nabet, "Design of an Addressable Internetworked Microscale Sensor", *Special Issue: Journal of Selected Areas in Microelectronics (JSAM)*, December 2010, ISSN: 1925-2676.

[J8] Y. Teng and B. Taskin, "Look-up Table Based Low Power Rotary Traelling Wave Oscillator Design Considering the Skin Effect", *Journal of Low Power Electronics (JOLPE)*, Vol. 6, No. 4, pp. 1–12, December 2010 [featured on the cover page].

[J7] J. Lu and B. Taskin, "Post-CTS Delay Insertion", *Journal of VLSI Design*, Article 451809, vol. 2010, February 2010.

[J6] B. Taskin and I. Kourtev, "Multi-Phase Synchronization of Non-Zero Clock Skew Level-Sensitive Circuit", *International Journal on Circuits, Systems and Computers (JCSC)*, Vol. 18, No. 5, pp. 899–908, July 2009.

[J5] B. Taskin, J. Demaio, O. Farell, M. Hazeltine, R. Ketner, "Custom Topology Rotary Clock Router", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 14, No. 3, Article 44, May 2009.

[J4] B. Taskin, A. Chiu, J. Salkind, D. Venutolo, "A Shift-Register Based QCA Memory Architecture", *ACM Journal on Emerging Technologies and Computation (JETC)*, Vol. 5, No. 1, Article 4, January 2009.

[J3] B. Taskin and B. Hong, "Improving Line-Based QCA Memory Cell Design Through Dual-Phase Clocking", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, Vol. 16, No. 12, pp. 1648–1656, December 2008.

[J2] B. Taskin and I. S. Kourtev, "Delay Insertion Method in Clock Skew Scheduling", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 25, No. 4, pp. 651–663, April 2006.

[J1] B. Taskin and I. S. Kourtev, "Linearization of the Timing Analysis and Optimization of Level-Sensitive Digital Synchronous Circuits", *IEEE Transactions on Very Large Scale Integration (VLSI)*

Systems (TVLSI), Vol. 12, No. 1, pp. 12–27, January 2004.

Conference Publications

[C59] Y. Teng and B. Taskin, "Resonant Frequency Divider Design Methodology for Dynamic Frequency Scaling", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2013.

[C58] C. Sitik, P. Nagvajara and B. Taskin, "A Microcontroller-Based Embedded System Design Course with PSoC3", *Proceedings of the IEEE International Conference on Microelectronic Systems Education (MSE)*, June 2013, pp. 28–31..

[C57] C. Sitik and B. Taskin, "Multi-Corner Multi-Voltage Domain Clock Mesh Design", *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, May 2013, pp. 209–214.

[C56] C. Sitik and B. Taskin, "Skew-Bounded Low Swing Clock Tree Optimization", *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, May 2013, pp. 49–54. [Best paper award nominee]

[C55] Y. Teng and B. Taskin, "Rotary Traveling Wave Oscillator Frequency Division at Nanoscale Technologies", *Proceedings of ACM Great Lakes Symposium on VLSI (GLSVLSI)*, May 2013, pp.349–350.

[C54] C. Sitik and B. Taskin, "Implementation of Domain-Specific Clock Meshes for Multi-Voltage SoCs with IC Compiler", *Proceedings of Synopsys User Group Conference Silicon Valley (SNUG)*, March 2013.

[C53] Y. Teng and B. Taskin, "Sparse-Rotary Oscillator Array (SROA) Design for Power and Skew Reduction", *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, March 2013.

[C52] J. Lu, X. Mao and B. Taskin, "Clock Mesh Synthesis with Gated Local Trees and Activity Driven Register Clustering", *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2012, pp. 691–697.

[C51] C. Sitik and B. Taskin, "Multi-Voltage Domain Clock Mesh Design", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, September 2012, pp. 201–206.

[C50] Y. Teng and B. Taskin, "Clock Mesh Synthesis Method using Earth Mover's Distance under Transformations", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, September 2012, pp. 121–126.

[C49] Y. Teng and B. Taskin, "Synchronization Scheme for Brick-Based Rotary Oscillator Arrays", *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, May 2012, pp. 117–122.

[C48] A. More and B. Taskin, "A Unified Design Methodology for a Hybrid Wireless 2-D NoC", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2012, pp. 640–643.

[C47] V. Honkote, A. More and B. Taskin, "3-D Parasitic Modeling for Rotary Interconnects", *Proceedings of the International Conference on VLSI Design (VLSID)*, January 2012, pp. 137–142.

[C46] A. More and B. Taskin, "EM and Circuit Co-simulation of a Reconfigurable Hybrid Wireless NoC on 2D ICs", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2011, pp. 19–24.

[C45] Y. Teng, J. Lu and B. Taskin, "ROA-Brick Topology for Rotary Resonant Clocks", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2011, pp. 273–278.

[C44] A. More and B. Taskin, "Simulation Based Study of On-chip Antennas for a Reconfigurable Hybrid 2D Wireless NoC", in the *Proceedings of the IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2011.

[C43] J. Lu and B Taskin, "From RTL to GDSII: An ASIC Design Course Development using Synopsys University Program", to appear in the *Proceedings of the IEEE International Conference on Microelectronic Systems Education (MSE)*, June 2011, pp. 72–75.

[C42] J. Lu, Y. Aksehir and B. Taskin, "Register On MEsh (ROME): A Novel Approach for Clock Mesh Network Synthesis", to appear in the *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2011, pp. 1219–1222.

[C41] J. Lu and B. Taskin, "Reconfigurable Clock Polarity Assignment for Peak Current Reduction of Clock-gated Circuits", to appear in the *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2011, pp. 1940–1943.

[C40] Y. Teng and B. Taskin, "Process Variation Sensitivity of the Rotary Traveling Wave Oscillator", to appear in the *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2011, pp. 236–242.

[C39] J. Lu, X. Mao and B. Taskin, "Timing Slack Aware Incremental Register Placement with Non-uniform Grid Generation for Clock Mesh Synthesis", *Proceedings of the ACM International Symposium on Physical Design (ISPD)*, March 2011, pp. 131–138.

[C38] J. Lu, V. Honkote, X. Chen and B. Taskin, "Steiner Tree Based Rotary Clock Routing with Bounded Skew and Capacitive Load Balancing", *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, March 2011, pp. 455–460.

[C37] V. Honkote, A. More, Y. Teng, J. Lu and B. Taskin, "Interconnect Modeling, Synchronization and Power Analysis for Custom Rotary Rings", *Proceedings of the International Conference on VLSI Design (VLSID)*, January 2011.

[C36] V. Honkote and B. Taskin, "Skew-Aware Capacitive Load Balancing for Low-Power Zero Clock Skew Rotary Oscillatory Array", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2010, pp. 209–214.

[C35] A. More and B. Taskin, "Simulation Based Study of On-chip Antennas for a Reconfigurable Hybrid 3D Wireless NoC", *Proceedings of the IEEE International SOC Conference (SOCC)*, September 2010, pp. 447–452.

[C34] A. More and B. Taskin, "Wireless Interconnects for Inter-tier Communication on 3-D ICs", *Proceedings of the European Microwave Integrated Circuits Conference (EuMIC)*, September 2010, pp. 105–108.

[C33] A. More and B. Taskin, "Effect of EMI between Wireless Interconnects and Metal Interconnects on CMOS Digital Circuits", *Mediterranean Microwave Sympoisum (MMS)*, August 2010.

[C32] V. Honkote and B. Taskin, "PEEC Based Parasitic Modeling for Power Analysis on Custom Rotary Rings", *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*, August 2010, pp. 111–116.

[C31] A. More and B. Taskin, "Electromagnetic Compatibility of CMOS On-chip Antennas", *Proceedings of the IEEE AP-S International Symposium on Antennas and Propagation (APS-URSI)*, July 2010.

[C30] A. More and B. Taskin, "Simulation Based Feasibility Study of Wireless RF Interconnects for 3D ICs", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2010.

[C29] J. Lu and B. Taskin, "Clock Tree Synthesis with XOR Gates for Polarity Assignment", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2010, pp. 17-22.

[C28] V. Honkote and B. Taskin, "Design Automation and Analysis of Resonant Rotary Clocking Technology", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2010, pp. 471–472.

[C27] A. More and B. Taskin, "Simulation Based Study of Wireless RF Interconnects for Practical CMOS Implementation", *the Proceedings of the System Level Interconnect Prediction (SLIP)*, June 2010, pp. 35–41.

[C26] A. More and B. Taskin, "Electromagnetic Interaction of On-Chip Antennas and CMOS Metal Layers for Wireless IC Interconnects", *Proceedings of the IEEE/ACM Great Lakes Symposium on VLSI Design (GLSVLSI)*, May 2010.

[C25] A. More and B. Taskin, "Leakage Current Analysis for Intra-Chip Wireless Interconnects", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2010, pp. 49–53.

[C24] J. Lu and B. Taskin, "Clock Buffer Polarity Assignment Considering Capacitive Load", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2010, pp. 765–770.

[C23] V. Honkote and B. Taskin, "Skew Analysis and Bounded Skew Constraint Methodology for Rotary Clocking Technology", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2010, pp. 413–417.

[C22] V. Honkote and B. Taskin, "Analysis, Design and Simulation of Capacitive Load Balanced Rotary Oscillatory Array", *Proceedings of the International Conference on VLSI Design (VLSID)*, January 2010, pp. 218–223.

[C21] J. Lu and B. Taskin, "Incremental Register Placement for Low Power CTS", *Proceedings of the IEEE International SoC Design Conference (ISOCC)*, November 2009, pp. 232–236.

[C20] V. Honkote and B. Taskin, "Skew Analysis and Design Methodologies for Improved Performance of Resonant Clocking", *Proceedings of the IEEE International SoC Design Conference (ISOCC)*, November 2009, pp. 165–168.

[C19] J. Lu and B. Taskin, "Post-CTS Clock Skew Scheduling with Limited Delay Buffering", *Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS)*, August 2009, pp. 224–227.

[C18] V. Honkote and B. Taskin, "Design Automation Scheme for Wirelength Analysis of Resonant Clocking Technologies", *Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS)*, August 2009, pp. 1147–1150.

[C17] V. Honkote and B. Taskin, "Capacitive Load Balancing for Mobius Implementation of Standing Wave Oscillator", *Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS)*, August 2009, pp. 232–235.

[C16] V. Honkote and B. Taskin, "Zero Clock Skew Synchronization with Rotary Clocking Technology", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2009, pp. 588–593.

[C15] V. Honkote and B. Taskin, "Custom Rotary Clock Router", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2008, pp. 114–119.

[C14] B. Taskin and J. Lu, "Post-CTS Delay Insertion to Fix Timing Violations", *Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS)*, August 2008, pp. 81–84.

[C13] S. Kurtas and B. Taskin, "Statistical Timing Analysis of Nonzero Clock Skew Circuits", *Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS)*, August 2008, pp. 605–608 [Best student paper award nominee].

[C12] V. Honkote and B. Taskin, "Maze Router Based Scheme for Rotary Clock Router", *Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS)*, August 2008, pp. 442–445.

[C11] B. Taskin, A. Chiu, J. Salkind, D. Venutolo, "A Shift-Register Based QCA Memory Architecture", *Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, October 2007, pp. 54–61.

[C10] P. Nagvajara and B. Taskin, "Design-for-Debug: A Vital Aspect in Education", *Proceedings of the International Conference on Microelectronic Systems Education (MSE)*, June 2007, pp. 65–66.

[C9] B. Taskin and I. S. Kourtev, "A Timing Optimization Method Based on Clock Skew Scheduling and Partitioning in a Parallel Computing Environment", *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2006, pp. 486–490.

[C8] B. Taskin, J. Wood and I. S. Kourtev, "Timing-Driven Physical Design for VLSI Circuits Using Resonant Rotary Clocking", *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2006, pp. 261–265.

[C7] B. Taskin and B. Hong, "Dual-Phase Line-Based QCA Memory Design", *Proceedings of the IEEE Conference on Nanotechnology (NANO)*, July 2006, pp. 302–305.

[C6] B. Taskin and I. S. Kourtev, "Delay Insertion in Clock Skew Scheduling", *Proceedings of the ACM International Symposium on Physical Design (ISPD)*, San Francisco, CA, Apr. 2005, pp. 47–54.

[C5] B. Taskin and I. S. Kourtev, "Performance Improvement of Edge-Triggered Sequential Circuits", *Proceedings of the IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, December 2004, pp. 607–610.

[C4] B. Taskin and I. S. Kourtev, "Advanced Timing of Level-Sensitive Sequential Circuits", *Proceedings of the IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, December 2004, pp. 603–606.

[C3] B. Taskin and I. S. Kourtev, "Time Borrowing and Clock Skew Scheduling Effects on Multi-Phase Level-Sensitive Circuits", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2004, Vol. 2, pp. II-617–620.

[C2] B. Taskin and I. S. Kourtev, "Performance Optimization of Single-Phase Level-Sensitive Circuits Using Time Borrowing and Non-Zero Clock Skew", *Proceedings of the ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, December 2002, pp. 111–117.

[C1] B. Taskin and I. S. Kourtev, "Linear Timing Analysis of SOC Synchronous Circuits with Level-Sensitive Latches", *Proceedings of the IEEE International ASIC/SOC Conference*, September 2002, pp. 358–362.

SPONSORED PROJECTS

- ◇ 9/2013-8/2016, PI, NSF CRI, $700k, *II-NEW: Testbed for High Speed Interconnects*.
- ◇ 7/2013-6/2016, Co-PI (50% with PI Salman at Stony Brook), Semiconductor Research Corporation (SRC), *Design and Automation of a Novel Low Swing Clocking Methodology with Reduced Delay Uncertainty*.
- ◇ 9/2012-8/2015, PI, NSF CCSS, $400k, *Hybrid Wireless Network-on-Chips*.
- ◇ 3/2010-2/2013, PI, NSF REU, $360k, *REU Site: Computing for Power and Energy: The Old, The New and The Renewable*.
- ◇ 9/2009-8/2014, PI, NSF CAREER, $400k, *Rotary Clock Technology Integration*.
- ◇ 9/2009-9/2010, PI, MOSIS, *Wireless Integrated Circuit Interconnect for Clocking*, $4 \times 4\text{mm}^2$ 90nm CMOS RF fabrication.
- ◇ 9/2007-8/2008, PI, A. Richard Newton Graduate Scholarship, ACM/IEEE Design Automation Conference (DAC) 2007, *Routing for Resonant Clocking Technology in Multi-GHz range*.

GRADUATE STUDENT ADVISEES

- ◇ 9/2013–current, Leo Flippini, Ph.D. student, *Topic: Low Power Circuits*
- ◇ 9/2011–current, A. Can Sitik, Ph.D. candidate, *Topic: Low Power Clock Networks*
- ◇ 9/2009–current, Ying Teng, Ph.D. candidate, *Topic: Resonant Adiabatic Clocking and Low-Power Clock Networks*
- ◇ 9/2009–5/2013, Ankit More, Ph.D., *Dissertation: Network-on-Chip (NoC) Architectures for Exascale Chip-Multi-Processor (CMPs)*
- ◇ 9/2011–6/2012, Swetha George, M.S., *Topic: Performance Analysis of NoCs with Wireless Interconnects*
- ◇ 9/2010–6/2011, Kevin Daly, B.S./M.S., *Topic: Ultra Low Power Adiabatic Logic*

- ◇ 9/2007–6/2011, Jianchao Lu, Ph.D., *Dissertation: High Performance IC Clock Networks with Mesh and Tree Topologies*
- ◇ 9/2009–6/2011, Xiaomi Mao, M.S., *Topic: IC Timing Optimization through Clocking*
- ◇ 9/2009–6/2011, Sharat C. Shekar, M.S., *Topic: IC Power Grid Simulator*
- ◇ 9/2006–6/2010, John Vargas, M.S. (part-time), *Topic: Physical Design for 3D IC and Interconnects*
- ◇ 9/2006–8/2010, Vinayak Honkote, Ph.D., *Dissertation: Design Automation and Analysis of Resonant Clocking Technologies*
- ◇ 9/2006–6/2007, Yaswanth Simhadri, M.S., *Topic: QCA Design Simulator*
- ◇ 9/2006–6/2007, Shannon M. Kurtas, B.S./M.S., *Thesis: Statistical Static Timing Analysis of Nonzero Clock Skew Circuits*

THESIS COMMITTEE MEMBERSHIP (OTHER)

- ◇ 6/2013, Ertan Gezer, Ph.D., *Species Transport Mechanisms Governing Crossover and Capacity Loss in Vanadium Redox Flow Batteries*
- ◇ 6/2013, Rui Wang, Ph.D., *Decentralized Control Architectures for Power Management in Data Centers*
- ◇ 6/2012, Karthik Ramu Sangaiah, M.S., *Variable Fractional Digital Delay Filter on Reconfigurable Hardware*
- ◇ 6/2012, Quang Tu, Ph.D., *Raman Spectroscopy Detects Cardiac Allograft Rejection with Molecular Specificity*
- ◇ 12/2011, James Anthony Shackleford, Ph.D., *High-Performance Image Registration Algorithms for Multi-Core Processors*
- ◇ 05/2011, Takashi Nakamura, Ph.D., *Quantitative X-ray Differential Interference Contrast Microscopy*
- ◇ 03/2011, Scott Haney, Ph.D., *Practical Applications and Properties of the Exponentially Modified Gaussian (EMG) Distribution*
- ◇ 11/2008, Atanu Chattopadhyay, Ph.D. (McGill University), *Dual Reference Signal, Post-Silicon Reconfigurable Clock Distribution Networks*
- ◇ 7/2008, Nakul Jain, M.S., *GPU-Accelerated Deformable Registration of Cone-beam CT Images*
- ◇ 7/2008, Shahab Ahmad, B.S./M.S., *A Parallel Controller Implementation for Dynamix Resource Allocation in Virtualized Computing Environment*
- ◇ 6/2006, Zayd Hammoudeh, B.S./M.S., *ForPowER : A Novel Architecture for Energy Efficient Implementation for Fork-Join Parallelism Using System on a Chip*
- ◇ 6/2005, Jeng Long Yang, M.S., *Implementation of Voice Over IP processor on FPGA System*