Scott P. Lerner

Department of Electrical and Computer Engineering
Drexel University, Bossone 324, 3141 Chestnut Street
Philadelphia, PA 19104-2875

Phone: 863-307-6194
E-mail: spl29@drexel.edu
Url: vlsi.ece.drexel.edu

EDUCATION

◇ **Ph.D., Electrical Engineering**, (September 2014 – expected graduation 2018).
Drexel University, Philadelphia, PA.

◇ **B.S., Electrical Engineering**, GPA: 3.5, 2014.
Drexel University, Philadelphia, PA.

◇ **B.S., Computer Engineering**, GPA: 3.5, 2014.
Drexel University, Philadelphia, PA.

PROFESSIONAL EXPERIENCE

◇ **Graduate Researcher**, (September 2014 – current)
VLSI Laboratory, Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA, USA

- Physical Design resilience through workload-awareness
- Investigated linear timing models for clock buffers
- Designed Low-power circuits using the following techniques:
  - Clock Gating
  - Low-power, high-performance
- Examined Clock Gating techniques for efficiency and power

◇ **Undergraduate Research Assistant – VLSI Laboratory**, (January 2012 – August 2014)
VLSI Laboratory, Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA, USA

- NSF Research Experience for Undergraduate (REU) grant
- Clock tree mesh optimization algorithms (500 lines C++)
- Implemented an advanced algorithm for clock buffer sizing (700 lines C++)
- Custom VLSI Design, ASIC Design I/II, Network-on-Chip, Computer Architecture courses
  - Cadence: RTL Compiler, Encounter, Virtuoso, Spectre
  - Synopsys: 1) DC for synthesis, 2) ICC for physical design floorplanning, placement, routing, CTS,
  - 3) Primetime for Static Timing Analysis 4) HSPICE for simulation
  - BookSim, HNoC for Network-on-Chip simulation
- Senior Design Project on Wireless Interconnect Design for 2D and 3D ICs
  - NoC simulation, HFSS modeling, RF and Antenna modeling

◇ **Undergraduate Research Assistant – DPAC Laboratory**, (January 2012 – August 2014)
DPAC Laboratory, Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA, USA

- Validated binary instrumentation error compared to full-system simulation
- Network-on-Chip design space exploration of resource optimization
- Automated verification testing for CPU event traces

◇ **Co-op Technical Senior**, (April 2013 – September 2013)
Lockheed Martin
Cherry Hill, NJ, USA

– Optimized software defined radios for spectrum denial capabilities
– Formulated programs to allow for large data sets to be analyzed quickly
– Obtained and maintained a **Secret level security clearance**

◇ **Software Developer**, (January 2012 – September 2012)
Software Support-PMW
Sewell, NJ, USA

– Designed five iPhone/iPad applications targeted for commercial sales
– Implemented a point-of-sale system on the iOS platform
– Maintained backend database communication to apache server

◇ **DRAM Product Engineer**, (March 2011 – September 2011)
Micron Technologies Inc.
Boise, ID, USA

– Performed functional testing and verification on packaged and bare memory die
– Diagnosed part failures for physical design and signal integrity issues
– Worked with a team to brainstorm and apply innovative fixes to new products

PUBLICATIONS

◇ S. Nilakantan, S. Lerner, M. Hempstead and B. Taskin, *Can you trust your memory trace?: A comparison of memory traces from binary instrumentation and simulation*, Presented at the IEEE International Conference on VLSI Design (VLSIDESIGN), January 2015.

◇ Can Sitik, Scott Lerner and Baris Taskin, *Timing Characterization of Clock Buffers for Clock Tree Synthesis*, Proceedings of the IEEE International Conference on Computer Design (ICCD), October 2014.

SELECTED PROJECTS

◇ **Leap Motion-Controlled Electric Wheelchair, Philly Codefest – Dean's Choice Award**
– Programmed communication circuitry to interface between XBee and DC Motors
– Designed Low Power motor control using Arduino
– Presented prototype to Venture Capitalists

◇ **Machine Learning Quadcopter, Lerner Research Labs**
– Using Machine Learning algorithms to identify surveillance targets
– Precise control of battery for extended mission flights
– Developed optimization equations related to hardware tradeoffs

◇ **Smart Light Bicycle, Lerner Research Labs**
– Added sensors to existing bicycle hardware for increased awareness
– Programmed ATMEGA328 to interpret sensor information
– Provide automatic safety to bicyclists through awareness to motorists

PRESENTATIONS

◇ C. Sitik, S. Lerner, and B. Taskin, *Timing Characterization of Clock Buffers for Clock Tree Synthesis*, Presentation given at IEEE International Conference on Computer Design (ICCD), Oct 2014.

◇ S. Lerner, V. Pano, and B. Taskin, *Wireless Network on Chip*, Poster to be presented at Mid-Atlantic ASEE, November 2014.

◇ S. Lerner, *Arduino Robotics in the Classroom*, Poster to be presented at Mid-Atlantic ASEE, November 2014.

◇ Scott Lerner, and Baris Taskin, *Low-Power Clock Network Designs*, Poster presented at IEEE Design Automation Conference, June 2014.

◇ Can Sitik, Scott Lerner, and Baris Taskin, *Low Swing Clocking Algorithm for 20nm FinFET Technology*, Poster presented at Upsilon Pi Epsilon Research Reception, February 2014.

◇ Can Sitik, Scott Lerner, and Baris Taskin, *Sub-45nm Interconnect Modeling*, Poster presented at Drexel IEEE Graduate Forum, February 2014.

- Scott Lerner, R. Welliver, B. Derveni, C. Schoenfield, I. Yilmaz , *MotionExplorer, A Leap Motion-Controlled Electric Wheelchair*, presented at Philly Codefest, February 2014.
- Can Sitik, Scott Lerner, and Baris Taskin, *Low-Power/High-Performance Clock Network Design for Microprocessors*, Poster presented at Upsilon Pi Epsilon Research Reception, February 2013.

Teaching Assistant Coursework

- Embedded Systems, Fall 2014-15, Junior Level Class
- Introduction to Computer Networks, Fall 2014-15, Junior Level Class
- Design with Microcontrollers, Summer 2013-14 Junior Level Class
- Network-on-chip I, Fall 2013-14, Graduate Level Class
- ASIC Design II, Spring 2013-14, Graduate Level Class

Professional Activities

- Technical Chair - Drexel IEEE Graduate Society 2014
- Member - Drexel IEEE Undergraduate 2013, 2014
- Student Member - Institute of Electrical and Electronics Engineers 2010-Current

Volunteer Activities

- STAR Mentor - Low-power Circuit Design, Drexel University 2013-14
- Freshman Design Mentor - Wireless HDMI, Drexel University 2013-14
- TechGirlz Workshop held in Philadelphia, PA
- SeaPerch Underwater Robotics Challenge 2014 held in Philadelphia, PA
- Biomedical Sciences and Professional Studies Graduate Orientation 2014 held in Philadelphia, PA
- City Year Park Cleanup in Philadelphia, PA

Skills

- C, C++, Python, Objective-C (10,000+ lines written)
- Pthread, OpenMP, Tcl, Assembly (MIPS), SystemC (1,000+ lines written)
- Verilog HDL, Matlab, Arduino, LaTeX (1,000+ lines written)
- Cadence – RTL Compiler, Encounter, Virtuoso Suite, Spectre, PSpice
  Synopsys – Design Compiler, IC Compiler, HSpice
- vi, Office Suites
- Unix, Linux, Windows, DOS

Academic Honors and Awards

- NSF Research Experience for Undergraduate (REU) Grant 2014
- A. Richard Newton Young Fellow Award 2014
- Dean's Choice Award at Philly Codefest for MotionExplorer 2014 held in Philadelphia, PA.
- NextFab Innovation Award at Philly Codefest for MotionExplorer 2014 held in Philadelphia, PA.
- Doctor Thomas Moore Endowed Grant 2014
- Dean's List, 2009, 2010, 2011, 2012, 2013, 2014.

References

- **Dr. Baris Taskin**
  Associate Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  E-mail: taskin@coe.drexel.edu
- **Dr. Mark Hempstead**
  Assistant Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  E-mail: mhempstead@coe.drexel.edu