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RESEARCH INTERESTS

Hardware and software design with expertise in electronic design automation (EDA) for VLSI, clock network synthesis and resonant clocking, circuit timing and retiming, low-power circuits and systems (CAS), charge-recovering circuits, networks-on-chip (NoC) for chip multi-processors (CMPs), hardware/software design space exploration for exascale computing systems.

EDUCATION

- **Ph.D, Electrical Engineering**, July 2005.
  University of Pittsburgh, Pittsburgh, PA
- **M.S., Electrical Engineering**, May 2003.
  University of Pittsburgh, Pittsburgh, PA
- **B.S., Electrical and Electronics Engineering**, June 2000.
- **Minor Program Diploma, Operations Research**, June 2000.
  Middle East Technical University, Ankara, Turkey

PROFESSIONAL EXPERIENCE

- **Professor**, (09/2016 – current)
  Associate Professor, (09/2011 – 08/2016)
  Assistant Professor, (09/2005 – 08/2011)
  Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  – Drexel VLSI and Architecture Laboratory (VANDAL)

- **Ph.D. Intern Engineer**, (09/2003 – 06/2004)
  MultiGiG Inc., Scotts Valley, CA [now Analog Devices, Inc.]

ACADEMIC HONORS AND AWARDS

- "Keynote speaker", IEEE International Workshop on Network on Chip Architectures 2019 (NOCARC'19), Columbus, OH.
- "Outstanding Research", Drexel ECE Department, 2015.
- "Young Engineer of the Year", Institute of Electrical and Electronics Engineers (IEEE) Philadelphia Section, 2013.
- "Distinguished Service Award", Association for Computing Machinery (ACM) Special Interest Group on Design Automation (SIGDA), 2012.
- "Faculty Early Career Development (CAREER)" award, National Science Foundation (NSF), 2009.
- "A. Richard Newton Graduate Scholarship" award for junior faculty starting new programs in EDA, ACM/IEEE Design Automation Conference (DAC) 2007.
- "Student Leadership Award", Student Government Board, University of Pittsburgh, 2005.

PROFESSIONAL ACTIVITIES

- **Editorship**
  – Associate Editor, *Microelectronics Journal, Elsevier, 2015–current*
  – Associate Editor, *Journal of Circuits, Systems and Computers (JCSC), World Scientific, 2012–current*

◇ **Professional Society and Government Service**

– *Chair*, IEEE Circuits and Systems Society (CASS) VLSI Systems and Applications Technical Committee (VSA-TC), 2018–2020

– *Chair*, IEEE Council on EDA (CEDA) Pennsylvania Local Chapter, 2016–current

– *Treasurer*, IEEE Council on EDA (CEDA) Pennsylvania Local Chapter, 2015–2016

– *Co-founder [with Xin Li (CMU), Helen Li (Pitt)]*, IEEE Council on EDA (CEDA) Pennsylvania Local Chapter, 2015

– *Academic Coordinator*, ACM Special Interest Group on Design Automation (SIGDA) University Booth at DAC, 2008, 2009, 2010, 2011, 2012, 2013

– *Organizing Committee Member*, NSF CISE REU PI Meeting, 2013

◇ **Organization Committee Member (General Chair, TPC Chair, Finance Chair, etc.)**

– *TPC Co-Chair*, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2020

– *General Co-Chair*, ACM Great Lakes Symposium on Very Large Scale Integrated Circuits (GLSVLSI), 2019

– *TPC Co-Chair*, ACM Great Lakes Symposium on Very Large Scale Integrated Circuits (GLSVLSI), 2018

– *Finance Chair*, International Symposium on Circuits and Systems (ISCAS), 2017

– *General Chair*, ACM/IEEE System Level Interconnect Prediction (SLIP), 2016

– *Publications Chair*, IEEE Computer Society International Symposium on VLSI (ISVLSI), 2016

– *TPC Chair*, ACM/IEEE System Level Interconnect Prediction (SLIP), 2015

– *Publicity Chair*, International Symposium on Low Power Electronic Design (ISLPED), 2014, 2015

– *Finance Chair*, ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP), 2014

– *Panel Chair*, ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP), 2013

– *Publicity Chair*, ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP), 2012

– *Finance Chair*, IFIP/IEEE International on Very Large Scale Integration (VLSI-SOC), 2012

– *Local Arrangements Chair*, ACM Great Lakes Symposium on Very Large Scale Integrated Circuits (GLSVLSI), 2006

◇ **Technical Program Committee Member**

–IEEE International Conference on Computer-Aided Design (ICCAD), 2012, 2013, 2014

–ACM Great Lakes Symposium on Very Large Scale Integrated Circuits (GLSVLSI), 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015

–ACM/IEEE System Level Interconnect Prediction (SLIP), 2012, 2013, 2014

–IEEE International Conference on Computer Design (ICCD), 2010, 2012, 2014, 2015, 2020

–IEEE International Green and Sustainable Computing Conference (IGSC), 2018

–IEEE/ACM International Symposium on System-on-a-Chip (ISOCC), 2015

–IEEE International Symposium on Nanoelectronic and Information Systems (INIS), 2015, 2016, 2017

–IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), 2009, 2010

–IEEE/ACM Asia Symposium on Quality Electronic Design (ASQED), 2010, 2011

–IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2008, 2020

–IEEE International Conference on Modeling, Simulation and Applied Optimization (ICMSAO), 2008

–EuroMicro Conference on Digital System Design (DSD), 2011, 2013

–IEEE Microelectronics Systems Education (MSE) Conference, 2011, 2013, 2015

–ASEE Mid-Atlantic Conference, 2015

–First International Workshop on Future Computing Technologies, 2006

◇ **Steering Committee Member**

– ACM Great Lakes Symposium on Very Large Scale Integrated Circuits (GLSVLSI), 2019–current

– ACM/IEEE System Level Interconnect Prediction (SLIP), 2017–current

– IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2007–2013

◇ **Track Chair**

– IEEE International Symposium on Circuits and Systems (ISCAS), "Digital Integrated Circuits and Systems" track co-chair, 2019, 2020

– IEEE International System-on-Chip Conference (ISOCC), "Power and Energy Circuits", 2016

– ACM Great Lakes Symposium on VLSI (GLSVLSI), "Low Power and Power Aware Design", 2014, 2015, 2016

– IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), "CAD" track, 2009, 2010
– IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), "VLSI" track co-chair, 2008

EDUCATIONAL INITIATIVES AND ACCOMPLISHMENTS

- ◇ **Drexel VIP Team advisor to IoT Processor project (2017–curent)** Started 1 of the 3 first Vertically Integrated Projects (VIP) teams at Drexel University in 2017.
- ◇ **Undergraduate Research Advisor to NSF GRFP recipients**, Michael Miller (from Computer Science, Goshen College, IN, 2013 to CMU in 2015), Scott Lerner (from ECE, Drexel University, 2012–4, to Drexel University in 2015), Giordano Salvador (from Computer Science, University of Pennsylvania, 2013–4, to UIUC in 2015)
- ◇ **Course Development**, Computation Lab I and II – Freshmen level course, developed in AY 2014–2015.
- ◇ **Academic Coordinator and PI**, NSF-funded REU Site on "Computing for Power and Energy: The Old, The New and The Renewable", 2010–2014.
- ◇ **Course Development**, Network-on-Chip Design – Graduate level course, developed in AY 2013–2014.
- ◇ **Course Development**, Introduction to VLSI Design, ASIC Design I, ASIC Design II – Senior level undergraduate/graduate courses, developed in AY 2007–2008.
- ◇ **Course Development**, EDA for VLSI Circuits I, EDA for VLSI Circuits II, Deep Sub-Micron Integrated Circuit Design – Graduate level courses, developed in AY 2005–2006.
- ◇ **SIGDA University Booth at DAC** participation by senior design project group, J. DeMaio, O. Farell, M. Hazeltine and R. Ketner, 2007.
- ◇ **ECE Senior Design Award** as advisor to C. Weingarten and E. Fargnoli, 2010, Drexel University ECE Department.
- ◇ **ECE Senior Design Award** as advisor to J. DeMaio, O. Farell, M. Hazeltine and R. Ketner, 2007, Drexel University ECE Department.

UNIVERSITY AND DEPARTMENTALSERVICE

- ◇ ECE Planning and Development Committee member, 2018–current
- ◇ ECE Faculty Promotion and Recognition Committee member, 2018–2020
- ◇ ECE Faculty Promotion and Recognition Committee chair, 2017–2018
- ◇ ECE Faculty Recruitment Committee chair, 2016–current
- ◇ Computer Engineering Curricular Group chair, 2014–2018
- ◇ Drexel College of Engineering Research Committee - ECE representative, 2014–2016
- ◇ Drexel Centralized Research Facilities advisory committee, 2013–2016
- ◇ ECE Awards committee Member/Chair/Past Chair, 2012–2013 / 2013–2014 / 2014–2017
- ◇ College of Engineering Awards committee member, 2014–2015
- ◇ Computer Engineering curricular group chair (interim), 2011–2012
- ◇ Computer Engineering faculty search committee, 2011–2013
- ◇ Boren Scholarship campus review committee, 2012–2014
- ◇ Fullbright scholarship campus review committee, 2011–2012

PUBLICATIONS

Conference Publications

[C102] R. Kuttappa, S. Khoa, L. Filippini, V. Pano, and B. Taskin, "Comprehensive Low Power Adiabatic Circuit Design with Resonant Power Clocking", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2020.

[C101] R. Kuttappa and B. Taskin, "FinFET – Based Low Swing Rotary Traveling Wave Oscillators", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2020.

[C100] K. Sangaiah, M. Lui, R. Kuttappa, B. Taskin, and M. Hempstead, "SnackNoc: Processing in the Communication Layer", *Proceedings of the IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, February 2020.

[C99] V. Pano, R. Kuttappa, and B. Taskin, "3D NoCs with Active Interposer for Multi-Die Systems", *Proceedings of the IEEE/ACM International Symposium on Networks-on-Chip (NOCS)*, October 2019.

[C98] R. Kuttappa, B. Taskin, S. Lerner, V. Pano, and I. Savidis, "Robust Low Power Clock Synchronization for Multi-Die Systems", *Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, July 2019.

[C97] L. Wang, R. Kuttappa, B. Taskin, and S. Kose, "Distributed Digital Low-Dropout Regulators with Phase Interleaving for On-Chip Voltage Noise Mitigation", *Proceedings of the IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2019.

[C96] C. Sitik, W. Liu, B. Taskin and E. Salman, "Low Voltage Clock Tree Synthesis with Local Gate Clusters", *Proceedings of the ACM Great Lakes Symposium on Very Large Scale Integration (GLSVLSI)*, May 2019.

[C95] V. Pano, I. Tekin, Y. Liu, K. R. Dandekar, and B. Taskin, "In-Package Wireless Communication with TSV-based Antenna", *IEEE International Symposium on Circuits and Systems Late Breaking News (ISCAS-LBN)*, May 2019.

[C94] R. Kuttappa, S. Lerner, L. Filippini, and B. Taskin, "Low Swing – Low Frequency Rotary Traveling Wave Oscillators", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019.

[C93] S. Lerner and B. Taskin, "Towards Design Decisions for Genetic Algorithms in Clock Tree Synthesis", *Proceedings of the IEEE International Green and Sustainable Computing Conference (IGSC)*, October 2018.

[C92] O. Bshara, Y. Liu, I. Tekin, B. Taskin, K. R. Dandekar, "mmWave Antenna Gain Switching to Mitigate Indoor Blockage", *Proceedings of the IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (APS-URSI)*, July 2018.

[C91] V. Pano, S. Lerner, I. Yilmaz, M. Lui, and B. Taskin, "Workload-Aware Routing (WAR) for Network-on-Chip Lifetime Improvement," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018.

[C90] S. Lerner, V. Pano, and B. Taskin, "NoC Router Lifetime Improvement using Per-Port Router Utilization," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018.

[C89] R. Kuttappa and B. Taskin, "Low Frequency Rotary Traveling Wave Oscillators", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018.

[C88] L. Filippini and B. Taskin, "A 900 MHz Charge Recovery Comparator with 40 fJ Per Conversion", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018.

[C87] M. Lui, K. Sangaiah, M. Hempstead, and B. Taskin, "Towards Cross-Framework Workload Analysis via Flexible Event-Driven Interfaces", *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 2018, pp. 169–178.

[C86] L. Filippini, L. Khuon, and B. Taskin, "Charge Recovery Implementation of an Analog Comparator: Initial Results", *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2017, pp. 1505–1508.

[C85] V. Pano, Y. Liu, I. Yilmaz, A. More, B. Taskin and K. Dandekar, "Wireless NoCs using Directional and Substrate Propagation Antennas", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2017, pp. 188–193.

[C84] S. Lerner and B. Taskin, "WT-CTS: Incremental Delay Balancing Using Parallel Wiring Type For CTS", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2017, pp. 465–470.

[C83] L. Filippini and B. Taskin, "A Charge Recovery Logic System Bus", *Proceedings of the IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2017.

[C82] S. Lerner, E. Leggett and B. Taskin, "Slew-Down: Analysis of Slew Relaxation for Low-Impact Clock Buffers", *Proceedings of the IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2017.

[C81] R. Kuttappa, L. Filippini, S. Lerner and B. Taskin, "Stability of Rotary Traveling Wave Oscillators Under Process Variations and NBTI", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2017.

[C80] R. Kuttappa, L. Khuon, B. Nabet and B. Taskin, "Reconfigurable Threshold Logic Gates using Optoelectronic Capacitors", *Proceedings of the Design, Automation and Test in Europe (DATE)*, March 2017, pp. 614–617.

[C79] S. Lerner and B. Taskin, "Workload-Aware ASIC Flow for Lifetime Improvement of Multi-core IoT Processors", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2017, pp. 379–384.

[C78] L. Filippini, D. Lim, L. Khuon and B. Taskin, "Wireless Charge Recovery System for Implanted Electroencephalography Applications in Mice", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2017, pp. 342–345.

[C77] V. Pano, I. Yilmaz, A. More and B. Taskin, "Energy Aware Routing of Multi-Level Network-on-Chip Traffic," *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2016, pp. 480–486.

[C76] V. Pano, I. Yilmaz, Y. Liu, B. Taskin and K. Dandekar, "Wireless Network-on-Chip Analysis of Propagation Technique for On-chip Communication," *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2016, pp. 400-403.

[C75] L. Filippini and B. Taskin, "Charge Recovery Logic for Thermal Harvesting Applications," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 542–545.

[C74] W. Liu, E. Salman, C. Sitik and B. Taskin, "Exploiting Useful Skew in Gated Low Voltage Clock Trees for High Performance," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 259–2598.

[C73] K. Sangaiah, M. Hempstead and B. Taskin, "Uncore RPD: Rapid Design Space Exploration of the Uncore via Regression Modeling", *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2015, pp. 365–372.

[C72] L. Filippini, E. Salman, B. Taskin, "A Wirelessly Powered System with Charge Recovery Logic", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2015, pp. 505–510.

[C71] M. Rathore, E. Salman, C. Sitik and B. Taskin, "A Novel Static D Flip-Flop Topology for Low Swing Clocking", *Proceedings of ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, May 2015, pp. 301–306.

[C70] W. Liu, E. Salman, C. Sitik and B. Taskin, "Clock Skew Scheduling in the Presence of Heavily Gated Clock Networks", *Proceedings of ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, May 2015, pp. 283-288.

[C69] W. Liu, E. Salman, C. Sitik and B. Taskin, "Enhanced Level Shifter for Multi-Voltage Operation," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 1442–1445.

[C68] Y. Liu, V. Pano, D. Patron, K. Dandekar and B. Taskin, "Innovative Propagation Mechanism for Inter-chip and Intra-chip Communication," *Proceedings of the IEEE Wireless and Microwave Technology Conference (WAMICON)*, April 2015, pp. 1–6.

[C67] S. Nilakantan, K. Sangaiah, A. More, G. Salvador, B. Taskin, M. Hempstead, "SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multi-core Simulation", *Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2015)*, March 2015, pp. 278–287.

[C66] G. Salvador, S. Nilakantan, B. Taskin, M. Hempstead and A. More, "Effects of Nondeterminism in Hardware and Software Simulation with Thread Mapping", *Proceedings of the IEEE/ACM International Conference on VLSI Design (VLSID)*, January 2015, pp. 129–134.

[C65] S. Nilakantan, S. Lerner, M. Hempstead and B. Taskin, "Can you trust your memory trace?: A comparison of memory traces from binary instrumentation and simulation", *IEEE/ACM International Conference on VLSI Design (VLSID)*, January 2015, pp. 135–140.

[C64] Y. Teng and B. Taskin, "Frequency-Centric Resonant Rotary Clock Distribution Network Design", *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2014, pp. 742–749.

[C63] C. Sitik, S. Lerner and B. Taskin, "Timing Characterization of Clock Buffers for Clock Tree Synthesis", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2014, pp. 230–236.

[C62] G. Salvador, S. Nilakantan, A. More, B. Taskin and M. Hempstead, "Static Thread Mapping for NoC CMPs via Binary Instrumentation Traces", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2014, pp. 517–520.

[C61] C. Sitik, L. Filippini, E. Salman and B. Taskin, "High Performance Low Swing Clock Tree Synthesis with Custom D Flip-Flop Design", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2014, pp. 498–503.

[C60] J. Kemmerer and B. Taskin, "Range-based Dynamic Routing of Hierarchical On Chip Network Traffic", *Proceedings of the IEEE International Workshop on System Level Interconnect Prediction (SLIP)*", June 2014, pp. 1-9.

[C59] Y. Teng and B. Taskin, "Resonant Frequency Divider Design Methodology for Dynamic Frequency Scaling", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2013, pp. 479–482.

[C58] C. Sitik, P. Nagvajara and B. Taskin, "A Microcontroller-Based Embedded System Design Course with PSoC3", *Proceedings of the IEEE International Conference on Microelectronic Systems Education (MSE)*, June 2013, pp. 28–31.

[C57] C. Sitik and B. Taskin, "Multi-Corner Multi-Voltage Domain Clock Mesh Design", *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, May 2013, pp. 209–214.

[C56] C. Sitik and B. Taskin, "Skew-Bounded Low Swing Clock Tree Optimization", *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, May 2013, pp. 49–54. [Best paper award nominee]

[C55] Y. Teng and B. Taskin, "Rotary Traveling Wave Oscillator Frequency Division at Nanoscale Technologies", *Proceedings of ACM Great Lakes Symposium on VLSI (GLSVLSI)*, May 2013, pp.349–350.

[C54] C. Sitik and B. Taskin, "Implementation of Domain-Specific Clock Meshes for Multi-Voltage SoCs with IC Compiler", *Proceedings of Synopsys User Group Conference Silicon Valley (SNUG)*, March 2013.

[C53] Y. Teng and B. Taskin, "Sparse-Rotary Oscillator Array (SROA) Design for Power and Skew Reduction", *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, March 2013, pp. 1229–1234.

[C53] J. Lu, X. Mao and B. Taskin, "Clock Mesh Synthesis with Gated Local Trees and Activity Driven Register Clustering", *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2012, pp. 691–697.

[C51] M. Guthaus and B. Taskin, "High-Performance, Low-Power Resonant Clocking: Embedded tutorial", *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2012, pp. 742–745.

[C50] C. Sitik and B. Taskin, "Multi-Voltage Domain Clock Mesh Design", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, September 2012, pp. 201–206.

[C49] Y. Teng and B. Taskin, "Clock Mesh Synthesis Method using Earth Mover's Distance under Transformations", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, September 2012, pp. 121–126.

[C48] Y. Teng and B. Taskin, "Synchronization Scheme for Brick-Based Rotary Oscillator Arrays", *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, May 2012, pp. 117–122.

[C47] A. More and B. Taskin, "A Unified Design Methodology for a Hybrid Wireless 2-D NoC", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2012, pp. 640–643.

[C46] V. Honkote, A. More and B. Taskin, "3-D Parasitic Modeling for Rotary Interconnects", *Proceedings of the International Conference on VLSI Design (VLSID)*, January 2012, pp. 137–142.

[C45] A. More and B. Taskin, "EM and Circuit Co-simulation of a Reconfigurable Hybrid Wireless NoC on 2D ICs", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2011, pp. 19–24.

[C44] Y. Teng, J. Lu and B. Taskin, "ROA-Brick Topology for Rotary Resonant Clocks", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2011, pp. 273–278.

[C43] A. More and B. Taskin, "Simulation Based Study of On-chip Antennas for a Reconfigurable Hybrid 2D Wireless NoC", in the *Proceedings of the IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2011.

[C42] J. Lu and B Taskin, "From RTL to GDSII: An ASIC Design Course Development using Synopsys University Program", *Proceedings of the IEEE International Conference on Microelectronic Systems Education (MSE)*, June 2011, pp. 72–75.

[C41] J. Lu, Y. Aksehir and B. Taskin, "Register On MEsh (ROME): A Novel Approach for Clock Mesh Network Synthesis", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2011, pp. 1219–1222.

[C40] J. Lu and B. Taskin, "Reconfigurable Clock Polarity Assignment for Peak Current Reduction of Clock-gated Circuits", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2011, pp. 1940–1943.

[C39] Y. Teng and B. Taskin, "Process Variation Sensitivity of the Rotary Traveling Wave Oscillator", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2011, pp. 236–242.

[C38] J. Lu, X. Mao and B. Taskin, "Timing Slack Aware Incremental Register Placement with Non-uniform Grid Generation for Clock Mesh Synthesis", *Proceedings of the ACM International Symposium on Physical Design (ISPD)*, March 2011, pp. 131–138.

[C37] J. Lu, V. Honkote, X. Chen and B. Taskin, "Steiner Tree Based Rotary Clock Routing with Bounded Skew and Capacitive Load Balancing", *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, March 2011, pp. 455–460.

[C36] V. Honkote and B. Taskin, "Skew-Aware Capacitive Load Balancing for Low-Power Zero Clock Skew Rotary Oscillatory Array", *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2010, pp. 209–214.

[C35] A. More and B. Taskin, "Simulation Based Study of On-chip Antennas for a Reconfigurable Hybrid 3D Wireless NoC", *Proceedings of the IEEE International SOC Conference (SOCC)*, September 2010, pp. 447–452.

[C34] A. More and B. Taskin, "Wireless Interconnects for Inter-tier Communication on 3-D ICs", *Proceedings of the European Microwave Integrated Circuits Conference (EuMIC)*, September 2010, pp. 105–108.

[C33] A. More and B. Taskin, "Effect of EMI between Wireless Interconnects and Metal Interconnects on CMOS Digital Circuits", *Mediterranean Microwave Sympoisum (MMS)*, August 2010.

[C32] V. Honkote and B. Taskin, "PEEC Based Parasitic Modeling for Power Analysis on Custom Rotary Rings", *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*, August 2010, pp. 111–116.

[C31] A. More and B. Taskin, "Electromagnetic Compatibility of CMOS On-chip Antennas", *Proceedings of the IEEE AP-S International Symposium on Antennas and Propagation (APS-URSI)*, July 2010.

[C30] A. More and B. Taskin, "Simulation Based Feasibility Study of Wireless RF Interconnects for 3D ICs", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2010, pp. 228–231.

[C29] J. Lu and B. Taskin, "Clock Tree Synthesis with XOR Gates for Polarity Assignment", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2010, pp. 17-22.

[C28] V. Honkote and B. Taskin, "Design Automation and Analysis of Resonant Rotary Clocking Technology", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2010, pp. 471–472.

[C27] A. More and B. Taskin, "Simulation Based Study of Wireless RF Interconnects for Practical CMOS Implementation", *the Proceedings of the System Level Interconnect Prediction (SLIP)*, June 2010, pp. 35–41.

[C26] A. More and B. Taskin, "Electromagnetic Interaction of On-Chip Antennas and CMOS Metal Layers for Wireless IC Interconnects", *Proceedings of the IEEE/ACM Great Lakes Symposium on VLSI Design (GLSVLSI)*, May 2010, pp. 413-416.

[C25] A. More and B. Taskin, "Leakage Current Analysis for Intra-Chip Wireless Interconnects", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2010, pp. 49–53.

[C24] J. Lu and B. Taskin, "Clock Buffer Polarity Assignment Considering Capacitive Load", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2010, pp. 765–770.

[C23] V. Honkote and B. Taskin, "Skew Analysis and Bounded Skew Constraint Methodology for Rotary Clocking Technology", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2010, pp. 413–417.

[C22] V. Honkote and B. Taskin, "Analysis, Design and Simulation of Capacitive Load Balanced Rotary Oscillatory Array", *Proceedings of the International Conference on VLSI Design (VLSID)*, January 2010, pp. 218–223.

[C21] J. Lu and B. Taskin, "Incremental Register Placement for Low Power CTS", *Proceedings of the IEEE International SoC Design Conference (ISOCC)*, November 2009, pp. 232–236.

[C20] V. Honkote and B. Taskin, "Skew Analysis and Design Methodologies for Improved Performance of Resonant Clocking", *Proceedings of the IEEE International SoC Design Conference (ISOCC)*, November 2009, pp. 165–168.

[C19] J. Lu and B. Taskin, "Post-CTS Clock Skew Scheduling with Limited Delay Buffering", *Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS)*, August 2009, pp. 224–227.

[C18] V. Honkote and B. Taskin, "Design Automation Scheme for Wirelength Analysis of Resonant Clocking Technologies", *Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS)*, August 2009, pp. 1147–1150.

[C17] V. Honkote and B. Taskin, "Capacitive Load Balancing for Mobius Implementation of Standing Wave Oscillator", *Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS)*, August 2009, pp. 232–235.

[C16] V. Honkote and B. Taskin, "Zero Clock Skew Synchronization with Rotary Clocking Technology", *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2009, pp. 588–593.

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[C12] V. Honkote and B. Taskin, "Maze Router Based Scheme for Rotary Clock Router", *Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS)*, August 2008, pp. 442–445.

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Journal Publications

[J31] V. Pano, I. Tekin, I. Yilmaz, Y. Liu, K. R. Dandekar, and B. Taskin, "TSV Antennas for Multi-Band Wireless Communication", *IEEE Journal on Emerging Topics in Circuits and Systems (JETCAS)*, March 2020.

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[J29] R. Kuttappa, S. Kose, and B. Taskin, "FOPAC: Flexible On-Chip Power and Clock", *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I), Vol. 66, No. 12, pp. 4628–4636, December 2019.*

[J28] Y. Liu, O. Bshara, I. Tekin, C. Israel, A. Hoorfar, B. Taskin, K. Dandekar, "Design and Fabrication of a Two-Port Three-Beam Switched Beam Antenna Array for 60 GHz Communication", *IET Microwaves, Antennas & Propagation, Vol. 13, No. 9, pp. 1438–1442, July 2019.*

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[J26] R. Kuttappa, A. Balaji, V. Pano, B. Taskin, and H. Mahmoodi, "RotaSYN: Rotary Traveling Wave Oscillator SYNthesizer", *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I), Vol. 66, No. 7, pp. 2685–2698, July 2019*.

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[J23] S. Lerner and B. Taskin, "Slew Merging Region Propagation for Bounded Slew and Skew Clock Tree Synthesis," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI), Vol. 27, No. 1, pp 1–11, January 2019.*

[J22] A. More, V. Pano, and B. Taskin, "Vertical Arbitration-free 3D NoCs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Vol. 37, No. 9, pp. 1853–1866, September 2018*.

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[J18] Y. Teng and B. Taskin, "ROA-Brick Topology for Low-Skew Rotary Resonant Clock Network Design", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 23, No. 11, pp. 2519–2530, November 2015.

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[J16] C. Sitik and B. Taskin, "Iterative Skew Minimization for Low Swing Clocks", *Elsevier Integration, the VLSI Journal*, Vol. 47, No. 3, pp. 356–364, June 2014.

[J15] V. Honkote and B. Taskin, "ZeROA: Zero Clock Skew Rotary Oscillatory Array", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, Vol. 20, No. 8, pp. 1528–1532, August 2012.

[J14] J. Lu, Y. Teng and B. Taskin, "A Reconfigurable Clock Polarity Assignment Flow for Clock Gated Designs", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, Vol. 20, No. 6, pp. 1002–1011, June 2012.

[J13] J. Lu, X. Mao and B. Taskin, "Integrated Clock Mesh Synthesis with Incremental Register Placement", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 31, No. 2, pp. 217–227, February 2012.

[J12] J. Lu and B. Taskin, "Clock Buffer Polarity Assignment with Skew Tuning", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 16, No. 4, Article 49, October 2011.

[J11] V. Honkote and B. Taskin, "CROA: Design and Analysis of Custom Rotary Oscillatory Array", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, Vol. 19, No. 10, pp. 1837–1847, October 2011.

[J10] S. M. Kurtas and B. Taskin, "Statistical Timing Analysis of the Clock Period Improvement through Clock Skew Scheduling", *International Journal of Circuits, Systems and Computers (JCSC)*, Vol. 20, No. 5, pp. 1–18, 2011.

[J9] K. Yencha, M. Zofchak, D. Oakum, G. Strait, B. Taskin, B. Nabet, "Design of an Addressable Internetworked Microscale Sensor", *Special Issue: Journal of Selected Areas in Microelectronics (JSAM)*, December 2010, ISSN: 1925-2676.

[J8] Y. Teng and B. Taskin, "Look-up Table Based Low Power Rotary Traelling Wave Oscillator Design Considering the Skin Effect", *Journal of Low Power Electronics (JOLPE)*, Vol. 6, No. 4, pp. 1–12, December 2010 [featured on the cover page].

[J7] J. Lu and B. Taskin, "Post-CTS Delay Insertion", *Journal of VLSI Design*, Article 451809, vol. 2010, February 2010.

[J6] B. Taskin and I. Kourtev, "Multi-Phase Synchronization of Non-Zero Clock Skew Level-Sensitive Circuit", *International Journal on Circuits, Systems and Computers (JCSC)*, Vol. 18, No. 5, pp. 899–908, July 2009.

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[J4] B. Taskin, A. Chiu, J. Salkind, D. Venutolo, "A Shift-Register Based QCA Memory Architecture", *ACM Journal on Emerging Technologies and Computation (JETC)*, Vol. 5, No. 1, Article 4, January 2009.

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[J2] B. Taskin and I. S. Kourtev, "Delay Insertion Method in Clock Skew Scheduling", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 25, No. 4, pp. 651–663, April 2006.

[J1] B. Taskin and I. S. Kourtev, "Linearization of the Timing Analysis and Optimization of Level-Sensitive Digital Synchronous Circuits", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, Vol. 12, No. 1, pp. 12–27, January 2004.

Books and Book Chapters

[B2] I. S. Kourtev, B. Taskin and E. G. Friedman, *Timing Optimization through Clock Skew Scheduling*, Springer, 2009.

[B1] B. Taskin, I. S. Kourtev and E. G. Friedman, *System Timing*, Handbook of VLSI, 2^{nd} edition, Editor: W. K. Chen, CRC Publishing, December 2006.

Patents

[P5] United States Patent No. 10,338,633, "Slew-Driven Clock Tree Synthesis", Inventors: Liu, Salman, Sitik, Taskin, 2019

[P4] United States Patent No. 9,484,896, "Resonant Frequency Divider Design Methodology for Dynamic Frequency Scaling", Inventors: Taskin and Teng, 2018

[P3] United States Patent No. 9,773,079, "Methods and computer-readable media for synthesizing a multi-corner mesh-based clock distribution network for multi-voltage domain and clock meshes and integrated circuits", Inventors: Taskin and Sitik, 2017

[P2] United States Patent No. 9,059,264, "Tunable Hot-Electron Transfer Within a Nanostructure", Inventors: Spanier, et al., 2015

[P1] United States Patent No. 8,704,577, "Clock Mesh Synthesis with Gated Local Tree Activity Driven Register Clustering", Inventors: Taskin and Lu, April 22, 2014.

SPONSORED PROJECTS

- ◇ 10/2020-9/2023, PI (with Co-PI Dandekar), NSF CNS, $465k, *CNS Core: Small: Wireless Interconnect Networks for Multi-Die systems*.
- ◇ 9/2018-8/2021, PI, NSF CCF, $390k, *SHF: Small: Circuits and Systems with Charge Recovery*.
- ◇ 7/2017–6/2020, Co-PI (with PI Dandekar), NSF CRI, $850,000, *II-NEW: Scalable Software Defined Radio Network Testbed for Hybrid Measurement and Emulation*.
- ◇ 5/2015-4/2016, Samsung Research, PI (50% with Co-PI Hempstead), *Fast and Efficient Hardware Design Exploration through Memory-NoC Analysis for Multi-Core SoCs*.
- ◇ 9/2013-8/2016, PI, NSF CRI, $700k, *II-NEW: Testbed for High Speed Interconnects*.
- ◇ 7/2013-6/2016, Co-PI (50% with PI Salman at Stony Brook), Semiconductor Research Corporation (SRC), *Design and Automation of a Novel Low Swing Clocking Methodology with Reduced Delay Uncertainty*.
- ◇ 9/2012-8/2015, PI, NSF CCSS, $400k (+$16k REU supplement), *Hybrid Wireless Network-on-Chips*.
- ◇ 3/2010-2/2013, PI, NSF REU, $360k, *REU Site: Computing for Power and Energy: The Old, The New and The Renewable*.
- ◇ 9/2009-8/2014, PI, NSF CAREER, $400k, *Rotary Clock Technology Integration*.
- ◇ 9/2009-9/2010, PI, MOSIS, *Wireless Integrated Circuit Interconnect for Clocking*, $4 \times 4\text{mm}^2$ 90nm CMOS RF fabrication.
- ◇ 9/2007-8/2008, PI, A. Richard Newton Graduate Scholarship, ACM/IEEE Design Automation Conference (DAC) 2007, *Routing for Resonant Clocking Technology in Multi-GHz range*.

CURRENT GRADUATE STUDENT ADVISEES

- ◇ 9/2013–current, Karthik "Paco" R. Sangaiah, Ph.D. candidate, *Topic: Exascale CMP Co-Design*, NSF GRFP (2014–2017), ARM internship (2015)
- ◇ 9/2014–current, Scott Lerner, Ph.D. candidate, *Topic: Low Power Cross-Layer Architecture and Physical Design*, NSF GRFP (2015–2018), AMD internship (2015), Intel Internship (2019)
- ◇ 9/2014–current, Michael Lui, Ph.D. candidate, *Topic: Hardware-Software Co-Design*, Facebook internship (2019-2020)
- ◇ 9/2015–current, Ragh Kuttappa, Ph.D. candidate, *Topic: Low Power Clocking*, Samsung internship (2017)
- ◇ 9/2018–current Dongen "Brad" Zhou, Ph.D. student, *Topic: TBD*

PAST GRADUATE STUDENT ADVISEES

- ◇ 9/2019–6/2020 Steven Khoa, M.S., *MS Thesis: Adiabatic Step-Charging Power-Clock Generator* [Lockheed-Martin, NJ]
- ◇ 9/2014–8/2019, Vasil Pano, Ph.D., *Dissertation: Wireless Network on Chip for Multi-Die Systems* [Post-Doc at Drexel University]
- ◇ 9/2013–6/2019, Leo Filippini, Ph.D., *Dissertation: Charge Recovery Circuits* [Voxtel, OR]
- ◇ 2014–2018, Isikcan Yilmaz, MS, BS, *Topic: Computer Architecture* [Apple, CA]
- ◇ 2017–2018, Adarsha Balaji, MS [Ph.D. at Drexel University]
- ◇ 6/2017–8/2017, Milene Douarche, visiting MS student from Grenoble Institute of Technology, France, *Topic: Layout Automation*
- ◇ 9/2016–4/2017, Rizwana Begum, Ph.D., *Dissertation: Energy Management of Multi-Component Computing Platforms Under Energy Constraints* [graduating advisor after M. Hempstead moved to Tufts University] [Intel, OR]
- ◇ 9/2011–12/2015, A. Can Sitik, Ph.D., *Dissertation: Design and Automation of Voltage-Scaled Networks* [Intel, OR]
- ◇ 6/2015–8/2015, Sophie Germain, visiting MS student from Grenoble Institute of Technology, France, *Topic: Low Power Circuit Design*
- ◇ 6/2012–6/2014, Steve DeLuca, MS (part-time), *Topic: Rotary Ring Design Automation* [Intel, PA]
- ◇ 10/2013–6/2014, Julian Kemerrer, BS/MS student, *Topic: Hierarchical NoC Design* [Susquehanna International Group (SIG), PA]
- ◇ 9/2009–6/2014, Ying Teng, Ph.D., *Dissertation: Low Power Resonant Rotary Global Clock Distribution Network Design* [Apple, CA]
- ◇ 9/2009–5/2013, Ankit More, Ph.D., *Dissertation: Network-on-Chip (NoC) Architectures for Exascale Chip-Multi-Processor (CMPs)* [Intel, OR]
- ◇ 9/2011–6/2012, Swetha George, MS, *Topic: Performance Analysis of NoCs with Wireless Interconnects* [Ph.D. program in University of Rochester]
- ◇ 9/2010–6/2011, Kevin Daly, BS/MS, *Topic: Ultra Low Power Adiabatic Logic*
- ◇ 9/2007–6/2011, Jianchao Lu, Ph.D., *Dissertation: High Performance IC Clock Networks with Mesh and Tree Topologies* [Synopsys, CA; Linkedin, CA]
- ◇ 9/2009–6/2011, Xiaomi Mao, MS, *Topic: IC Timing Optimization through Clocking* [Oracle, CA]
- ◇ 9/2009–6/2011, Sharat C. Shekar, MS, *Topic: IC Power Grid Simulator* [Samsung, TX; Apple, TX]
- ◇ 9/2006–6/2010, John Vargas, MS (part-time), *Topic: Physical Design for 3D IC and Interconnects* [Mentor Graphics, PA]
- ◇ 9/2006–8/2010, Vinayak Honkote, Ph.D., *Dissertation: Design Automation and Analysis of Resonant Clocking Technologies* [Intel, India; Intel, OR]
- ◇ 9/2006–6/2007, Yaswanth Simhadri, MS, *Topic: QCA Design Simulator*
- ◇ 9/2006–6/2007, Shannon M. Kurtas, BS/MS, *Thesis: Statistical Static Timing Analysis of Nonzero Clock Skew Circuits* [Intel, OR; CMU Finance, NY; Deutsche Bank, UK]

CURRENT AND PAST UNDERGRADUATE STUDENT ADVISEES

- ◇ Malachi Moody (2020) [Delaware State University- NSF REU]
- ◇ Eric Zane (2020) [Rowan University - NSF REU]
- ◇ Angela Wei (2019-2020) [Drexel]
- ◇ Steven Khoa (2019) [Drexel]
- ◇ Albert Emanuel Milani (2019) [Drexel]
- ◇ Neil Eelman (2018-2019) [Drexel, Fullbright alternate 2020]

- ◇ Kathrina Waugh (2018) [Drexel STARS scholar]
- ◇ Rhea Dutta (2018) [Drexel STARS scholar]
- ◇ Irmak Gezginer (2017) [Middle East Technical University (METU), graduate school at ETH]
- ◇ Daniel Heuckeroth (2016) [Drexel STARS scholar]
- ◇ Albert Emanuel Milani (2016) [Drexel STARS scholar]
- ◇ Nazzareno Farnesi (2016) [Drexel, Drexel STARS scholar]
- ◇ Brian Hosler (2015-2016) [Drexel], graduate school at Drexel
- ◇ Eric Leggett, Jr (2015-2016) [Drexel]
- ◇ Gabrielle Madden (2015) [Drexel STARS scholar]
- ◇ Isikcan Yilmaz (2015) [Drexel]
- ◇ Eronides Da Silva Neto (2015) [Temple]
- ◇ George Slavin (2015) [Drexel]
- ◇ Habeeb Olawin (2014) [Drexel STARS scholar]
- ◇ Fernando Ellis (2013) [RIT - NSF REU]
- ◇ Daniel Schoepflin (2013) [Drexel STARS scholar]
- ◇ Giordano Salvador (2013-2014) [Penn - NSF REU, NSF GRFP recipient in 2015]
- ◇ Vasil Pano (2013-2014) [Drexel, graduate school at Drexel]
- ◇ Andrew Apollonsky (2012) [Cooper Union - NSF REU]
- ◇ Michael Miller (2012) [Goshen College - NSF REU, NSF GRFP recipient in 2015]
- ◇ Michael Sineriz (2012) [Maryland - NSF REU]
- ◇ Scott Lerner (2012-2014), [Drexel, graduate school at Drexel, NSF GRFP recipient in 2015]
- ◇ Isuru Daulagala (2012) [Drexel, graduate school at Drexel]
- ◇ Catherine Leis (2011) [Drexel, graduate school at Penn]
- ◇ Asha Habib (2011) [Bryn Mawr College - NSF REU]
- ◇ Kevin Linger (2011) [University of Virginia - NSF REU, graduate school at UC Berkeley]
- ◇ Andrew Richard Benton (2011) [Drexel STARS scholar]
- ◇ David Hocky (2011) [Drexel STARS scholar]
- ◇ Yusuf Aksehir (2010) [Sabanci University, graduate school at Sabanci]
- ◇ Abdalla Musmar (2010) [An-Najah National University - NSF REU, graduate school at Carnegie Mellon University]
- ◇ Michael Edoror (2010) [University of Maryland - NSF REU]
- ◇ Bo Hyun Kim (2010) [Carnegie Mellon University, graduate school at Columbia University]
- ◇ S. Kutal Gokce (2008) [Middle East Technical University (METU), M.S. at Koc University, Ph.D. at U of Texas-Austin]
- ◇ Can Hankendi (2008) [Sabanci University, M.S. at USC, Ph.D. at Boston University]
- ◇ Danh Nguyen (2007) [Ph.D. at Drexel University]