

Vasil Pano

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- EDUCATION
- ◇ **Ph.D., Electrical Engineering**, (expected graduation 2018).
Drexel University, Philadelphia, PA.
 - ◇ **B.S., Computer Engineering**, 2014.
Drexel University, Philadelphia, PA.
- PROFESSIONAL EXPERIENCE
- ◇ **Extreme Scale Technologies Intern**, (June 2016 – January 2017)
Intel Corporation
Hillsboro, OR, USA
 - Worked on scalable Network-on-Chip model using SystemC
 - Co-designed and implemented novel memory coherence system utilizing the NoC
 - ◇ **Ph.D. Student**, (September 2014 – current)
VLSI and Architecture Laboratory, Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA, USA
 - Ph.D. student and member of the VLSI and Architecture lab
 - Studying Computer Architecture focusing primarily on:
 - Computer memory subsystem design and cache coherence protocols
 - Network-on-Chip architectures and routing algorithms
 - Wireless on-chip communication technologies
 - Current research projects:
 - Analyzing wireless communication behavior on a NoC (using custom SystemC simulator)
 - Implementing a custom Token cache coherence protocol within Gem5 (using SLICC)
 - Implementing a novel multi-channel RAM architecture within Gem5 (using DRAMSim2)
 - Designed multiple clustered architectures within Gem5 (using Garnet/Ruby)
 - ◇ **Undergraduate Research Assistant – VLSI Laboratory**, (April 2013 – July 2014)
VLSI Laboratory, Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA, USA
 - Senior Design Project on Wireless Interconnect Design for 2D and 3D ICs
 - NoC simulation, HFSS modeling, RF and antenna modeling
 - Network-on-Chip, Computer Architecture, Custom VLSI Design, ASIC Design I/II courses
 - DragonNoC, Booksim and HNOG (OMNET++ based simulator) for NoC simulation
 - Gem5 (Ruby and Garnet) for full-system, SynchroTrace for trace-based simulation
 - Cadence: RTL Compiler, Encounter, Virtuoso
 - Synopsys: 1) DC for synthesis, 2) ICC for physical design
 - 3) Primitime for Static Timing Analysis 4) HSPICE for simulation
 - ◇ **Undergraduate Research Assistant – DPAC Laboratory**, (June 2013 – July 2014)
DPAC Laboratory, Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA, USA
 - Implemented custom barrier synchronization method to the in-house SynchroTrace simulator
 - Multi-threaded trace-based system simulation for evaluating many-core architectures and NoCs
 - Application-aware memory and NoC co-design
 - Benchmark analysis (Splash-2x and PARSEC 3.0) on Synchrotrace

- ◇ **Outage Analysis Technologies Intern**, (March 2013 – September 2013)
PJM Interconnection
Norristown, PA, USA
 - Thorough understanding of Software Development Life Cycle (SDLC) and Waterfall Methodology
 - Created and maintained database design with detailed description of logical entities and physical tables
 - Expertise in writing functional specifications and translating business requirements to technical specifications
 - Extensive experience in manual and automated testing of applications
- ◇ **Operations Planning Intern**, (April 2012 – March 2013)
PJM Interconnection
Norristown, PA, USA
 - Responsible for performing production and regression testing the proprietary software called eDART
 - Effectively coordinated with member companies and collected time sensitive information critical to reliability
 - Manually check one-line diagram information for accuracy and update databases accordingly
 - Consolidated a Software Manual and Quick Reference Guide of eDART for external and internal users

- PUBLICATIONS ◇ V. Pano, I. Yilmaz, A. More, and B. Taskin, *Energy Aware Routing of Multi-Level Network-on-Chip Traffic*, Proceedings of the IEEE International Conference on Computer Design (ICCD), pp.480-486 October 2016.
- ◇ V. Pano, I. Yilmaz, Y. Liu, B. Taskin, and K. Dandekar, *Wireless Network-on-Chip Analysis of Propagation Technique for On-chip Communication*, Proceedings of the IEEE International Conference on Computer Design (ICCD), pp.400-403 October 2016.
- ◇ Y. Liu, V. Pano, D. Patron, K. Dandekar, and B. Taskin, *Innovative Propagation Mechanism for Inter-chip and Intra-chip Communication*, Proceedings of the IEEE Wireless and Microwave Technology Conference (WAMICON), pp.1-6 April 2015.

- PRESENTER ◇ V. Pano, and B. Taskin, *SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multicore Simulation*, Poster presented at Design Automation Conference (DAC), June 2016.
- ◇ V. Pano, M. Lui, M. Hempstead and B. Taskin, *Sigil and SynchroTrace: Communication-Aware Workload Profiling and Memory-NoC Simulation*, Tutorial presented at IEEE International Conference on Computer Design (ICCD), October 2015.
- ◇ V. Pano, S. Lerner, and B. Taskin, *Wireless Network-on-Chip*, Poster presented at American Society for Engineering Education (ASEE), November 2014.

- GRADUATE COURSEWORK ◇ High Performance Computer Architecture, Parallel Computer Architecture, Network-on-a-Chip (NoC)
- ◇ EDA for VLSI I & II, ASIC Design I & II, Custom VLSI
- ◇ Data Structures and Algorithms, Systems Programming, Internet Architecture and Protocols I & II

- TEACHING ASSISTANT COURSEWORK ◇ High Performance Computer Architecture, Spring 2015-2016, Graduate Level Class
- ◇ Systems Programming, Summer 2014-15 & Winter 2015-2016, Junior Level Class
- ◇ Computation Lab I & II, Fall & Winter 2015-2016, Freshmen Level Class
- ◇ Introduction to Parallel Computer Architecture, Fall 2015-16, Graduate Level Class
- ◇ Digital Systems Projects, Spring 2014-15, Junior Level Class
- ◇ Internet Architecture and Protocols, Winter 2014-15, Junior Level Class
- ◇ Digital Logic Design, Fall 2014-15, Sophomore Level Class
- ◇ ASIC Design II, Spring 2013-14, Graduate Level Class
- ◇ Network-on-chip I, Fall 2013-14, Graduate Level Class

- VOLUNTEER ACTIVITIES
- ◇ Intern Supervisor (Isikcan Yilmaz) - Gem5 memory study (using Ruby)
Drexel University, 2015-16
 - ◇ Senior Design Mentor - Wireless DRAM Solution
Drexel University, 2015-16
 - ◇ STAR Mentor (Eonides Neto) - Router architecture for Network-on-Chip
Drexel University, 2015
 - ◇ Freshman Design Mentor - Wireless HDMI
Drexel University, 2013-14
- SKILLS
- ◇ C, C++, SystemC, Verilog HDL
 - ◇ Pthread, OpenMP, CUDA
 - ◇ Python, Matlab, \LaTeX
 - ◇ Synopsys – Design Compiler, IC Compiler, HSpice
Cadence – RTL Compiler, Encounter, Virtuoso Suite
- ACADEMIC HONORS AND AWARDS
- ◇ Dean’s List, 2009, 2010, 2011, 2012, 2013, 2014
 - ◇ Dean’s Scholarship, Drexel University, September 2009 – June 2014
 - ◇ DU Endowed Scholarship, Drexel University, September 2009 – June 2014
- REFERENCES
- ◇ **Dr. Baris Taskin**
Associate Professor, Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA
E-mail: taskin@coe.drexel.edu
 - ◇ **Dr. Ankit More**
Research Scientist, Extreme Scale Technologies
Intel Corporation, Hillsboro, OR
E-mail: ankitmore@gmail.com
 - ◇ **Dr. Mark Hempstead**
Associate Professor, Department of Electrical and Computer Engineering
Tufts University, Medford, MA
E-mail: mark.hempstead@tufts.edu