Vasil Pano

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EDUCATION

- **Ph.D., Electrical Engineering**, (expected graduation June 2019).
  Drexel University, Philadelphia, PA.
- **B.S., Computer Engineering**, 2014.
  Drexel University, Philadelphia, PA.

PROFESSIONAL EXPERIENCE

- **Extreme Scale Technologies Graduate Intern**, (June 2016 – January 2017)
  Intel Corporation
  Hillsboro, OR, USA

  – Worked on scalable Network-on-Chip model using SystemC
  – Co-designed and implemented novel memory coherence system utilizing the NoC

- **Ph.D. Candidate**, (September 2014 – current)
  VLSI and Architecture Laboratory, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA, USA

  – Ph.D. Candidate and member of the Drexel VLSI and Architecture Laboratory (VANDAL)
  – Studying Computer Architecture focusing primarily on:
    – Computer memory subsystem design and cache coherence protocols
    – Network-on-Chip architectures and routing algorithms
    – Wireless on-chip communication technologies
    – Extreme scale NoCs and memory models
  – Current research projects:
    – Analyzing wireless communication behavior on a NoC (using custom SystemC simulator)
    – Implementing a novel multi-chip wireless infrastructure (using novel propagation technique on HFSS)
    – Implementing a custom memory model using the Token cache coherence protocol within Gem5
    – Designed multiple clustered architectures within Gem5 (using Garnet/Ruby)
    – Implementing custom thread mapping solution using Sigil2.0 and Synchrotrace (in-house tools)

- **Undergraduate Research Assistant – VLSI Laboratory**, (April 2013 – July 2014)
  VLSI Laboratory, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA, USA

  – Senior Design Project on Wireless Interconnect Design for 2D and 3D ICs
    – NoC simulation, HFSS modeling, RF and antenna modeling
  – Network-on-Chip, Computer Architecture, Custom VLSI Design, ASIC Design I/II courses
    – DragonNoC, Booksim and HNOC (OMNET++ based simulator) for NoC simulation
    – Gem5 (Ruby and Garnet) for full-system, SynchroTrace for trace-based simulation
    – Cadence: RTL Compiler, Encounter, Virtuoso
    – Synopsys: 1) DC for synthesis, 2) ICC for physical design
    – 3) Primetime for Static Timing Analysis 4) HSPICE for simulation

- **Undergraduate Research Assistant – DPAC Laboratory**, (June 2013 – July 2014)
  DPAC Laboratory, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA, USA

  – Implemented custom barrier synchronization method to the in-house SynchroTrace simulator
  – Executed multi-threaded trace-based system simulation for evaluating many-core architectures and NoCs
  – Application-aware memory and NoC co-design
  – Performed benchmark analysis (Splash-2x and PARSEC 3.0) on Synchrotrace

◇ **Operations Planning Intern**, (April 2012 – September 2013)
PJM Interconnection
Norristown, PA, USA

– Thorough understanding of Software Development Life Cycle (SDLC) and Waterfall Methodology
– Created and maintained database design with detailed description of logical entities and physical tables
– Expertise in writing functional specifications and translating business requirements to technical specifications
– Extensive experience in manual and automated testing of applications
– Responsible for performing production and regressing testing the proprietary software called eDART
– Effectively coordinated with member companies and collected time sensitive information critical to reliability

PUBLICATIONS

Journal Publications

◇ A. More, V. Pano, and B. Taskin, *Vertical Arbitration-free 3D NoCs*, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), Vol. 37, No. 9, pp. 1853–1866, September 2018.

Conference Publications

◇ V. Pano, S. Lerner, Isikcan Yilmaz, Michael Lui, and B. Taskin, *Workload-Aware Routing (WAR) for Network-on-Chip Lifetime Improvement*, Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), May 2018.

◇ S. Lerner, V. Pano, and B. Taskin, *NoC Router Lifetime Improvement Using Per-Port Router Utilization*, Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), May 2018.

◇ V. Pano, Y. Liu, I. Yilmaz, A. More, B. Taskin, and K. Dandekar, *Wireless NoCs using Directional and Substrate Propagation Antennas*, Proceedings of the IEEE International Symposium on VLSI (ISVLSI), pp. 188-193, July 2017.

◇ V. Pano, I. Yilmaz, A. More, and B. Taskin, *Energy Aware Routing of Multi-Level Network-on-Chip Traffic*, Proceedings of the IEEE International Conference on Computer Design (ICCD), pp. 480-486, October 2016.

◇ V. Pano, I. Yilmaz, Y. Liu, B. Taskin, and K. Dandekar, *Wireless Network-on-Chip Analysis of Propagation Technique for On-chip Communication*, Proceedings of the IEEE International Conference on Computer Design (ICCD), pp. 400-403, October 2016.

◇ Y. Liu, V. Pano, D. Patron, K. Dandekar, and B. Taskin, *Innovative Propagation Mechanism for Inter-chip and Intra-chip Communication*, Proceedings of the IEEE Wireless and Microwave Technology Conference (WAMICON), pp. 1-6, April 2015.

PRESENTER

◇ V. Pano, and B. Taskin, *SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multicore Simulation*, Poster presented at Design Automation Conference (DAC), June 2016.

◇ V. Pano, M. Lui, M. Hempstead and B. Taskin, *Sigil and SynchroTrace: Communication-Aware Workload Profiling and Memory–NoC Simulation*, Tutorial presented at IEEE International Conference on Computer Design (ICCD), October 2015.

◇ V. Pano, S. Lerner, and B. Taskin, *Wireless Network-on-Chip*, Poster presented at American Society for Engineering Education (ASEE), November 2014.

TEACHING ASSISTANT COURSEWORK

◇ *High Performance Computer Architecture*, Spring 2015-2016, Graduate Level Class

◇ *Systems Programming*, Summer 2014-15 & 2016-2017 & Winter 2015-2016 , Junior Level Class

◇ *Computation Lab I & II*, Fall & Winter 2015-2016 & Winter 2017-2018, Freshmen Level Class

◇ *Parallel Computer Architecture*, Fall 2015-16 & Winter 2016-2017, Graduate Level Class

- ◇ *Digital Systems Projects*, Spring 2014-15 & Fall 2017-2018, Junior Level Class
- ◇ *Internet Architecture and Protocols*, Winter 2014-15, Junior Level Class
- ◇ *Digital Logic Design*, Spring 2016-2017, & Fall 2018-2019, Sophomore Level Class

VOLUNTEER ACTIVITIES

- ◇ Graduate Student Supervisor (Isikcan Yilmaz) - Gem5 & NoC research
  Drexel University, 2015-18
- ◇ Senior Design Mentor - Wireless DRAM Solution
  Drexel University, 2015-16
- ◇ STAR Mentor (Eonides Neto) - Router architecture for Network-on-Chip
  Drexel University, 2015
- ◇ Freshman Design Mentor - Wireless HDMI
  Drexel University, 2013-14

SKILLS

- ◇ C, C++, SystemC, Verilog HDL, HFSS
- ◇ Pthread, OpenMP, CUDA
- ◇ Python, Matlab, LaTeX
- ◇ Synopsys – Design Compiler, IC Compiler, HSpice
  Cadence – RTL Compiler, Encounter, Virtuoso Suite

ACADEMIC HONORS AND AWARDS

- ◇ Drexel College of Engineering Oustanding Mentorship Award, 2018
- ◇ Drexel ECE Nihat Bilgutay Award (High Academic Achievement), 2017, 2018
- ◇ Drexel College of Engineering Dean's List, 2009–2014
- ◇ Drexel College of Engineering Dean's Scholarship, September 2009 – June 2016
- ◇ DU Drexel University Endowed Scholarship, Drexel University, September 2009 – June 2014

REFERENCES

- ◇ **Dr. Baris Taskin**
  Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  E-mail: taskin@coe.drexel.edu
- ◇ **Dr. Ankit More**
  Research Scientist, Data Center Group
  Intel Corporation, Hillsoboro, OR
  E-mail: ankit.more@intel.com
- ◇ **Dr. Nagarajan Kandasamy**
  Professor and Associate Department Head for Undergraduate Affairs
  Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  E-mail: kandasamy@coe.drexel.edu
- ◇ **Dr. Ibrahim Tekin**
  Professor, Department of Electronics Engineering
  Sabanci University, Istanbul, Turkey
  E-mail: tekin@sabanciuniv.edu