

# Vasil Pano

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- EDUCATION
- ◇ **Ph.D., Electrical Engineering**, 2019.  
Drexel University, Philadelphia, PA.
  - ◇ **B.S., Computer Engineering**, 2014.  
Drexel University, Philadelphia, PA.
- PROFESSIONAL EXPERIENCE
- ◇ **Post Doctoral Researcher**, (September 2019 – current)  
Drexel Wireless Systems Laboratory, Department of Electrical and Computer Engineering  
Drexel University, Philadelphia, PA, USA
    - Post Doctoral Researcher and Manager of the Drexel Wireless Systems Laboratory (DWSL)
    - Current research projects:
      - Analyzing wireless communication behavior on a Multi-Die System
      - Evaluating novel TSV-based antenna for on-package wireless communication
      - Investigating a novel multi-die topologies and routing algorithms infrastructure
  - ◇ **Ph.D. Candidate**, (September 2014 – August 2019)  
VLSI and Architecture Laboratory, Department of Electrical and Computer Engineering  
Drexel University, Philadelphia, PA, USA
    - Ph.D. Candidate and member of the Drexel VLSI and Architecture Laboratory (VANDAL)
    - Studying Computer Architecture focusing primarily on:
      - Wireless on-chip communication technologies
      - Network-on-Chip architectures and routing algorithms
      - Computer memory subsystem design and cache coherence protocols
      - Extreme scale NoCs and memory models
    - Current research projects:
      - Analyzing wireless communication behavior on a NoC (using custom SystemC simulator)
      - Evaluating novel TSV-based antenna for next generation on-chip wireless communication
      - Implementing a novel multi-chip wireless infrastructure (using novel propagation technique on HFSS)
      - Designed multiple clustered architectures within Gem5 (using Garnet/Ruby)
      - Implementing custom thread mapping solution using Sigil2.0 and Synchrotrace (in-house tools)
  - ◇ **Extreme Scale Technologies Graduate Intern**, (June 2016 – January 2017)  
Intel Corporation  
Hillsboro, OR, USA
    - Enhanced scalable Network-on-Chip model for high-performance computing using SystemC
    - Co-designed and implemented novel memory coherence system utilizing the NoC
  - ◇ **Undergraduate Research Assistant – VLSI Laboratory**, (April 2013 – July 2014)  
VLSI Laboratory, Department of Electrical and Computer Engineering  
Drexel University, Philadelphia, PA, USA
    - Senior Design Project on Wireless Interconnect Design for 2D and 3D ICs
      - NoC simulation, HFSS modeling, RF and antenna modeling
    - Network-on-Chip, Computer Architecture, Custom VLSI Design, ASIC Design I/II courses
      - DragonNoC, Booksim and HNOG (OMNET++ based simulator) for NoC simulation
      - Gem5 (Ruby and Garnet) for full-system, SynchroTrace for trace-based simulation
      - Cadence: RTL Compiler, Encounter, Virtuoso
      - Synopsys: 1) DC for synthesis, 2) ICC for physical design
      - 3) Primitime for Static Timing Analysis 4) HSPICE for simulation

- ◇ **Undergraduate Research Assistant – DPAC Laboratory**, (June 2013 – July 2014)  
DPAC Laboratory, Department of Electrical and Computer Engineering  
Drexel University, Philadelphia, PA, USA
  - Implemented custom barrier synchronization method to the in-house SynchroTrace simulator
  - Executed multi-threaded trace-based system simulation for evaluating many-core architectures and NoCs
  - Application-aware memory and NoC co-design
  - Performed benchmark analysis (Splash-2x and PARSEC 3.0) on Synchrotrace
- ◇ **Operations Planning Intern**, (April 2012 – September 2013)  
PJM Interconnection  
Norristown, PA, USA
  - Thorough understanding of Software Development Life Cycle (SDLC) and Waterfall Methodology
  - Created and maintained database design with detailed description of logical entities and physical tables
  - Expertise in writing functional specifications and translating business requirements to technical specifications
  - Extensive experience in manual and automated testing of applications
  - Responsible for performing production and regression testing the proprietary software called eDART
  - Effectively coordinated with member companies and collected time sensitive information critical to reliability

## PUBLICATIONS **Journal Publications**

- ◇ V. Pano, I. Tekin, Y. Liu, K. Dandekar, and B. Taskin, *TSV-Based Antenna for On-Chip Wireless Communication*, under review for IET Microwaves, Antennas & Propagation (IET-MAP).
- ◇ V. Pano, I. Tekin, I. Yilmaz, Y. Liu, K. Dandekar, and B. Taskin, *TSV Antennas for Multi-Band Network-on-Chip*, under review for IEEE Journal on Emerging and Selected Topics in Circuits and Systems (IEEE JETCAS).
- ◇ R. Kuttappa, A. Balaji, V. Pano, B. Taskin, and H. Mahmoodi, *RotaSYN: Rotary Traveling Wave Oscillator SYNthesizer*, IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I), January 2019.
- ◇ A. More, V. Pano, and B. Taskin, *Vertical Arbitration-free 3D NoCs*, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), Vol. 37, No. 9, pp. 1853–1866, September 2018.

### **Conference Publications**

- ◇ V. Pano, R. Kuttappa, I. Tekin, B. Taskin, and K. Dandekar, *Wireless Communication for Multi-Die Systems*, under review for the Design Automation Conference (DAC), July 2020.
- ◇ V. Pano, R. Kuttappa, and B. Taskin *3D NoCs with Active Interposer for Multi-Die Systems*, Proceedings of the IEEE/ACM International Symposium on Networks-on-Chip (NOCS), October 2019.
- ◇ R. Kuttappa, B. Taskin, S. Lerner, V. Pano, and I. Savidis *Robust Low Power Clock Synchronization for Multi-Die Systems*, Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), July 2019.
- ◇ V. Pano, I. Tekin, Y. Liu, K. Dandekar, and B. Taskin *In-Package Wireless Communication with TSV-based Antenna*, Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), May 2019.
- ◇ V. Pano, S. Lerner, Isikcan Yilmaz, Michael Lui, and B. Taskin, *Workload-Aware Routing (WAR) for Network-on-Chip Lifetime Improvement*, Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), May 2018.
- ◇ S. Lerner, V. Pano, and B. Taskin, *NoC Router Lifetime Improvement Using Per-Port Router Utilization*, Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), May 2018.

- ◇ V. Pano, Y. Liu, I. Yilmaz, A. More, B. Taskin, and K. Dandekar, *Wireless NoCs using Directional and Substrate Propagation Antennas*, Proceedings of the IEEE International Symposium on VLSI (ISVLSI), pp. 188-193, July 2017.
- ◇ V. Pano, I. Yilmaz, A. More, and B. Taskin, *Energy Aware Routing of Multi-Level Network-on-Chip Traffic*, Proceedings of the IEEE International Conference on Computer Design (ICCD), pp. 480-486, October 2016.
- ◇ V. Pano, I. Yilmaz, Y. Liu, B. Taskin, and K. Dandekar, *Wireless Network-on-Chip Analysis of Propagation Technique for On-chip Communication*, Proceedings of the IEEE International Conference on Computer Design (ICCD), pp. 400-403, October 2016.
- ◇ Y. Liu, V. Pano, D. Patron, K. Dandekar, and B. Taskin, *Innovative Propagation Mechanism for Inter-chip and Intra-chip Communication*, Proceedings of the IEEE Wireless and Microwave Technology Conference (WAMICON), pp. 1-6, April 2015.

- TEACHING ASSISTANT COURSEWORK
- ◇ *High Performance Computer Architecture*, Spring 2015-2016, Graduate Level Class
  - ◇ *Systems Programming*, Summer 2014-15 & 2016-2017 & Winter 2015-2016, Junior Level Class
  - ◇ *Computation Lab I & II*, Fall & Winter 2015-2016 & Winter 2017-2018, Freshmen Level Class
  - ◇ *Parallel Computer Architecture*, Fall 2015-16 & Winter 2016-2017, Graduate Level Class
  - ◇ *Digital Systems Projects*, Spring 2014-15 & Fall 2017-2018, Junior Level Class
  - ◇ *Internet Architecture and Protocols*, Winter 2014-15, Junior Level Class
  - ◇ *Digital Logic Design*, Spring 2016-2017, & Fall 2018-2019, Sophomore Level Class
- VOLUNTEER ACTIVITIES
- ◇ Reviewer - ACM Journal on Emerging Technologies in Computing Systems; Elsevier Microelectronics Journal; IEEE International Symposium on Nanoelectronic and Information Systems; Elsevier Integration Journal, IEEE International Symposium on Circuits and Systems;
  - ◇ Graduate Student Supervisor (Angela Wei) - Interconnect Modeling for Multi-Die Systems Drexel University, 2019-20
  - ◇ Senior Design co-advisor - The VarIoT Hub - Drexel University, 2019-20
  - ◇ Senior Design co-advisor - Radio Arena - Drexel University, 2019-20
  - ◇ Senior Design co-advisor - SDR for Anti-Jamming - Drexel University, 2019-20
  - ◇ Graduate Student Supervisor (Isikcan Yilmaz) - Gem5 & NoC research Drexel University, 2015-18
  - ◇ Senior Design Mentor - Wireless DRAM Solution Drexel University, 2015-16
  - ◇ STAR Mentor (Eonides Neto) - Router architecture for Network-on-Chip Drexel University, 2015
  - ◇ Freshman Design Mentor - Wireless HDMI Drexel University, 2013-14
- SKILLS
- ◇ C, C++, SystemC, Verilog HDL, HFSS
  - ◇ Pthread, OpenMP, CUDA
  - ◇ Python, Matlab, L<sup>A</sup>T<sub>E</sub>X
  - ◇ Synopsys – Design Compiler, IC Compiler, HSpice  
Cadence – RTL Compiler, Encounter, Virtuoso Suite
- ACADEMIC HONORS AND AWARDS
- ◇ Drexel College of Engineering Outstanding Mentorship Award, 2018
  - ◇ Drexel ECE Nihat Bilgutay Award (High Academic Achievement), 2017, 2018

- ◇ Drexel College of Engineering Dean's List, 2009–2014
- ◇ Drexel College of Engineering Dean's Scholarship, September 2009 – June 2016
- ◇ DU Drexel University Endowed Scholarship, Drexel University, September 2009 – June 2014

REFERENCES ◇ **Dr. Baris Taskin**

Professor, Department of Electrical and Computer Engineering  
Drexel University, Philadelphia, PA  
E-mail: [taskin@coe.drexel.edu](mailto:taskin@coe.drexel.edu)

◇ **Dr. Kapil R. Dandekar**

Professor, Department of Electrical and Computer Engineering  
Associate Dean for Enrollment Management and Graduate Education  
Drexel University, Philadelphia, PA  
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◇ **Dr. Ankit More**

Research Scientist, Data Center Group  
Intel Corporation, Hillsboro, OR  
E-mail: [ankit.more@intel.com](mailto:ankit.more@intel.com)

◇ **Dr. Ibrahim Tekin**

Professor, Department of Electronics Engineering  
Sabanci University, Istanbul, Turkey  
E-mail: [tekin@sabanciuniv.edu](mailto:tekin@sabanciuniv.edu)

◇ **Dr. Nagarajan Kandasamy**

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