Vasil Pano

Philadelphia, PA | 215-512-1519 | vasilpano@gmail.com | linkedin.com/in/vasilpano

EDUCATION

◇ **Ph.D. — Electrical Engineering** **September 2019**
Drexel University Philadelphia, PA
Thesis: Wireless Network-on-Chip for Multi-Die Systems

◇ **B.S. — Computer Engineering** **June 2014**
Drexel University Philadelphia, PA

EXPERIENCE

◇ **Post Doctoral Researcher** **September 2019 – Present**
Drexel University Wireless Systems Laboratory (DWSL) Philadelphia, PA

– Investigating novel heterogeneous multi-die architectures and adaptive cross-chiplet routing algorithms
– Implementing custom methodology for optimized mapping of chiplets on a multi-die system utilizing:
  – Event-driven application profiling and characterization framework Prism for workload trace generation
  – gem5-based simulation framework SynchroTrace for design-space exploration of non-uniform topologies
– Evaluating novel TSV-based antenna for efficient and long-distance on-package wireless communication
  – US Patent Application 16/719,536 - "TSV-based on-chip antennas, measurement, and evaluation"
– Contributed in joint effort on NSF award CNS Core: Small: Wireless Interconnect Networks for Multi-Die Systems.
– Research coordinator and manager of DWSL providing support and expertise to undergraduate and graduate researchers

◇ **Ph.D. Candidate** **September 2014 – August 2019**
Drexel University VLSI and Architecture Laboratory (VANDAL) Philadelphia, PA

– Designed and evaluated novel TSV antenna (TSV_A) within a simulated IC environment
  – Targeting the mmWave frequency range (30GHz up to 80GHz evaluated with ANSYS HFSS)
– Fabricated and tested TSV_A PCB prototype to verify functionality and validate HFSS simulation results
– Implemented novel NoC architecture that establishes multi-band wireless communication with TSV_As
– Investigated the scalable interconnect infrastructure of non-monolithic Multi-Die Systems
  – Proposed novel multi-die 3D NoC topology that utilizes the active interposer for die-to-die communication

◇ **Graduate Technical Intern** **June 2016 – January 2017**
Intel Corporation Data Center Group Hillsboro, OR

– Contributed in development of Network on Chip simulator for design exploration of on-chip networks and memory.
– Co-designed and implemented novel memory coherence protocol for large scale multi-processor systems
  – An ACK-less mechanism for software visibility of Store instructions
  – Implemented novel routing algorithm to optimize network performance

◇ **Undergraduate Research Assistant** **June 2013 – July 2014**
Drexel University VLSI & Power-Aware Computing Laboratories Philadelphia, PA

– Optimized multi-threaded performance of benchmark suite Splash2x and generated workload traces using Sigil
– Performed design-space exploration and analyzed system performance using the SynchroTrace trace replay tool

SKILLS

◇ Digital Design, Computer Architecture, Performance and Energy Modeling, Hardware/Software Co-design
◇ C, C++, SystemC, VHDL, SystemVerilog, Python, HFSS, Design Compiler, IC Compiler, Virtuoso, HSpice

PUBLICATIONS

Journal Publications

◇ V. Pano, I. Tekin, I. Yilmaz, Y. Liu, K. Dandekar, and B. Taskin, "TSV Antennas for Multi-Band Wireless Communication," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, vol. 10, no. 1, pp. 100–113, 2020

◇ V. Pano, I. Tekin, Y. Liu, K. Dandekar, and B. Taskin, "Tsv-based antenna for on-chip wireless communication," *IET Microwaves, Antennas & Propagation (IET-MAP)*, vol. 14, no. 4, pp. 302–307, 2019

◇ R. Kuttappa, A. Balaji, V. Pano, B. Taskin, and H. Mahmoodi, "Rotasyn: Rotary Traveling Wave Oscillator SYNthesizer," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 7, pp. 2685–2698, 2019

- A. More, V. Pano, and B. Taskin, "Vertical arbitration-free 3-D NoCs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 9, pp. 1853–1866, 2017

Conference Publications

- R. Kuttappa, S. Khoa, L. Filippini, V. Pano, and B. Taskin, "Comprehensive Low Power Adiabatic Circuit Design with Resonant Power Clocking," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, 2020
- V. Pano, R. Kuttappa, and B. Taskin, "3D NoCs with Active Interposer for Multi-Die Systems," in *Proceedings of the IEEE/ACM International Symposium on Networks-on-Chip (NOCS)*, pp. 1–8, 2019
- R. Kuttappa, B. Taskin, S. Lerner, V. Pano, and I. Savidis, "Robust Low Power clock Synchronization for Multi-Die Systems," in *Proceedings of the IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 1–6, 2019
- V. Pano, I. Tekin, Y. Liu, K. Dandekar, and B. Taskin, "In-Package Wireless Communication with TSV-based Antenna," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–3, May 2019
- V. Pano, S. Lerner, I. Yilmaz, M. Lui, and B. Taskin, "Workload-Aware Routing (WAR) for Network-on-Chip Lifetime Improvement," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, May 2018
- S. Lerner, V. Pano, and B. Taskin, "NoC Router Lifetime Improvement using Per-Port Router Utilization," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, May 2018
- V. Pano, Y. Liu, I. Yilmaz, A. More, B. Taskin, and K. Dandekar, "Wireless NoCs Using Directional and Substrate Propagation Antennas," in *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 188–193, July 2017
- V. Pano, I. Yilmaz, Y. Liu, B. Taskin, and K. Dandekar, "Wireless Network-on-Chip analysis of propagation technique for on-chip communication," in *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 400–403, October 2016
- V. Pano, I. Yilmaz, A. More, and B. Taskin, "Energy aware routing of multi-level Network-on-Chip traffic," in *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 480–486, October 2016
- Y. Liu, V. Pano, D. Patron, K. Dandekar, and B. Taskin, "Innovative propagation mechanism for inter-chip and intra-chip communication," in *Proceedings of the IEEE Annual Wireless and Microwave Technology Conference (WAMICON)*, pp. 1–6, April 2015

Professional Activities

- Reviewer of ACM Journal on Emerging Technologies in Computing Systems, Elsevier Microelectronics Journal, IEEE International Symposium on Nanoelectronic and Information Systems, Elsevier Integration Journal, Sustainable Computing, Informatics and Systems
- Graduate Student Supervisor (Angela Wei) - Non-uniform Wireless Multi-Die Systems 2019 - Present
- Graduate Student Supervisor (Isikcan Yilmaz) - NoC & gem5 related research 2015 - 2019
- Senior Design Projects Mentor: i) The VarIoT Hub, ii) Radio Arena, iii) DVT Prevention Device

Teaching Coursework

- High Performance Computer Architecture, Parallel Computer Architecture, Systems Programming, Digital Logic Design, Digital Systems Projects, Internet Architecture and Protocols, Computation Labs I/II

Academic Honors and Awards

- Drexel ECE Nihat Bilgutay Award ("High Academic Achievement"), 2017, 2018
- Drexel College of Engineering Oustanding Mentorship Award, 2018
- Drexel University Dean's List, Dean's Scholarship, Endowed Scholarship, (multiple instances)

References

- **Dr. Baris Taskin**
  Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  E-mail: taskin@coe.drexel.edu
- **Dr. Kapil R. Dandekar**
  Professor, Department of Electrical and Computer Engineering
  Associate Dean for Enrollment Management and Graduate Education
  Drexel University, Philadelphia, PA
  E-mail: dandekar@drexel.edu
- **Dr. Ankit More**
  Principal Engineer
  Microsoft, San Francisco, CA
  E-mail: ankitmore@gmail.com