Vasil Pano

Philadelphia, PA | vasilpano@gmail.com | 215-512-1519 | linkedin.com/in/vasilpano

Summary

Hardware architect with experience in architecture design and performance modeling at Intel Corporation. Primarily focused on the memory subsystem and interconnect network. Experience ranges from small-scale optimizations to large HW/SW co-design projects. Ability to assess and lead technical readiness of product, starting from high-level performance simulations with micro-benchmarks and 3D workloads and ending with RTL correlation and debug. Can drive solutions from ideation to prototyping and simulations, and eventually to architecture specification/definition. Excellent written and visual communication skills, enthusiasm towards tasks and engagements, great collaborator with peers, and proven mentorship abilities.

Education

Drexel University, Ph.D. – Electrical Engineering   **September 2019**
- **Thesis:** Wireless Network-on-Chip for Multi-Die Systems

Drexel University, B.S. – Computer Engineering   **June 2014**

Skills

Relevant: Computer architecture expertise, performance modeling proficiency, hw/sw co-design, performance trade-off analysis, technical writing (including high-level architecture specification), mentorship experience
Languages/Tools: Primarily working with C/C++, Golang, Python/Ruby. Familiarity with SystemC, VHDL, SystemVerilog, Cadence/Synopsys tools, HFSS

Experience

Silicon SoC Architect, Intel Corporation – Philadelphia, PA   **June 2021 – Present**
- Assessed SoC end-to-end performance readiness of Intel BMG and CLS GPUs
- Investigated, defined, developed, and proposed multiple novel memory subsystem features
    - GDDR Low Power mechanism to leverage low memory BW regions to improve power profile
    - Adaptive Flush engine to opportunistically clean dirty data during idle periods of Last-Level Cache
- Created and maintained architectural specifications (HAS) for proposed features
- Contributed to pathfinding efforts for next-generation client and datacenter Intel GPUs
- Contributed in the development of the performance model of Last-Level Cache and Fabric (Golang)
- Generated micro-benchmarks and proactively participated in RTL performance correlation and debug
- Evaluated performance at frequency and identified bottlenecks across various micros and 3D workloads

Post Doctoral Researcher, Drexel University – Philadelphia, PA   **June 2019 – June 2021**
- Investigating novel heterogeneous multi-die architectures and adaptive cross-chiplet routing algorithms
- Implementing custom methodology for optimized mapping of chiplets on a multi-die system utilizing:
    - Event-driven application characterization framework Prism for workload trace generation
    - gem5-based SynchroTrace replay tool for design-space exploration of non-uniform topologies
- Evaluating novel TSV antenna for efficient and long-distance on-package wireless communication
    - US Patent US11329362B2 - "TSV-based on-chip antennas, measurement, and evaluation"
- Contributed in joint effort on NSF award CNS Core: Small: Wireless Interconnect Networks for MDS
- Research coordinator and manager of DWSL providing support and expertise to student researchers

Graduate Research Assistant, Drexel University – Philadelphia, PA   **September 2014 – June 2019**

- Designed and evaluated novel TSV antenna (TSV_A) within a simulated IC environment
    - Targeting the mmWave frequency range (30GHz up to 80GHz evaluated with ANSYS HFSS)
- Fabricated and tested TSV_A PCB prototype to verify functionality and validate HFSS simulation results
- Implemented novel NoC architecture that establishes multi-band wireless communication with TSV_As
- Investigated the scalable interconnect infrastructure of non-monolithic Multi-Die Systems
    - Proposed novel multi-die 3D NoC topology that utilizes the active interposer for communication

Graduate Technical Intern, Intel Corporation – Hillsboro, OR   **June 2016 – January 2017**

- Co-developed Network on Chip simulator for design exploration of on-chip networks and memory
- Co-designed and implemented novel memory coherence protocol for large scale multi-processor systems
    - An ACK-less mechanism for software visibility of Store instructions
    - Implemented novel routing algorithm to optimize network performance

Undergraduate Research Assistant, Drexel University – Philadelphia, PA   **June 2013 – August 2014**

- Optimized performance of Splash2x workloads and captured traces with custom Valgrind tool
- Performed design-space exploration and analyzed performance using the SynchroTrace trace replay tool

Publications

- **Relevant Journal Publications**

    V. Pano, I. Tekin, I. Yilmaz, Y. Liu, K. Dandekar, and B. Taskin, "TSV Antennas for Multi-Band Wireless Communication," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, vol. 10, no. 1, pp. 100–113, 2020

    A. More, V. Pano, and B. Taskin, "Vertical arbitration-free 3-D NoCs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 9, pp. 1853–1866, 2017

- **Relevant Conference Publications**

    V. Pano, R. Kuttappa, and B. Taskin, "3D NoCs with Active Interposer for Multi-Die Systems," in *Proceedings of the IEEE/ACM International Symposium on Networks-on-Chip (NOCS)*, pp. 1–8, 2019

    V. Pano, S. Lerner, I. Yilmaz, M. Lui, and B. Taskin, "Workload-Aware Routing (WAR) for Network-on-Chip Lifetime Improvement," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, May 2018

    V. Pano, I. Yilmaz, Y. Liu, B. Taskin, and K. Dandekar, "Wireless Network-on-Chip analysis of propagation technique for on-chip communication," in *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 400–403, October 2016

    V. Pano, I. Yilmaz, A. More, and B. Taskin, "Energy aware routing of multi-level NoC traffic," in *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 480–486, October 2016

Mentorship Experience

- Graduate Student Supervisor (Angela Wei) - Non-uniform Wireless Multi-Die Systems   **2019 - 2021**
- Graduate Student Supervisor (Isikcan Yilmaz) - NoC & gem5 related research   **2015 - 2019**
- Senior Design Projects Mentor: The VarIoT Hub, Radio Arena, DVT Prevention Device   **2019 - 2021**

Academic Honors and Awards

- Drexel ECE Nihat Bilgutay Award ("High Academic Achievement"), 2017, 2018
- Drexel College of Engineering Oustanding Mentorship Award, 2018
- Drexel University Dean's List, Dean's Scholarship, Endowed Scholarship, (multiple instances)