

A. Can Sitik

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RESEARCH INTERESTS Design and Automation of High Performance/Low-Power Clock Distribution Networks, Clock Tree/Mesh Synthesis, VLSI Physical Design.

EDUCATION ◇ **Ph.D., Computer Engineering**, (September 2011 – current).
Drexel University, Philadelphia, PA.
Topic: Design and Automation of Low-Power Clock Distribution Networks
◇ **B.S., Electrical and Electronics Engineering**, GPA: 3.64 (with High Honors), (July 2011).
METU, Ankara, Turkey.
Concentration: Electronics/Computer Hardware

PROFESSIONAL EXPERIENCE ◇ **Research Assistant**, (September 2011 – current)
VLSI Laboratory, Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA, USA

- Electronic Design Automation (EDA) for VLSI Physical Design
- Low-Swing Clock Trees
- Clock Mesh Design for Multi-Voltage SoCs
- Multi-Corner/Multi-Mode Clocking

◇ **Teaching Assistant**, (September 2011 – current)
Department of Electrical and Computer Engineering & College of Engineering
Drexel University, Philadelphia, PA, USA

- ECEE 421, Advanced Electronics (Fall 2011)
- ECEC 304, Design with Microcontrollers (Winter 2012–2013, Summer 2012–2013)
- ENGR 231, Linear Engineering Systems (Fall 2012, Spring 2012)
- ECEC 302, Digital Systems Projects (Fall 2013, Spring 2013)

◇ **Undergraduate Research Assistant**, (September 2010 – June 2011)
DSP Laboratory, Department of Electrical and Electronics Engineering
METU, Ankara, Turkey

- Embedded Software Development for efficient implementation of DSP algorithms
- Embedded C Coding for TI's TMS3206747 DSP

◇ **Internship - Research and Development Engineering** , (June 2010 – July 2010)
ASELSAN Inc , Ankara, Turkey (Leading Defense Industry Company)

- Designed an embedded system and interface to be used in infrared night vision systems for target detection.
- Participated in the field tests and performance analysis of infrared cameras.

SELECTED PROJECTS ◇ **Clock Tree/Mesh Synthesis, Drexel University**

- Multi-Voltage Domain Clock Mesh Design & Synthesis
- Variation-Aware Clock Network Design
- Low Power CTS

- ◇ **Automation of Low Swing Clocking, Drexel University**
 - Skew-Bounded Low Swing Clock Tree Optimization
 - Buffer/Wire Modeling for Low Swing Clocks
 - Low Swing CTS
 - ◇ **Defrauder & Confuser Algorithm for Submarines, METU**
 - A smart algorithm that shuffles SONAR signals in order to cause false detection on the opposing submarines, funded by the Scientific and Technological Research Council of Turkey (NSF equivalent).
 - Implemented DSP algorithms on both TI's TMS320 processor with C, and a PC with C++.
 - ◇ **Smart Self-Parking Truck & Trailer System, Senior Design, METU**
 - A smart truck that can park forward or backward considering its passive trailer, into predefined slots on a platform.
 - Designed and implemented a parking algorithm ($\approx 2,000$ lines of C code).
 - Designed the peripheral circuitry to interface the microcontroller unit to the sensors and motors.
- RELEVANT GRADUATE COURSEWORK ◇ EDA for VLSI I & II, Deep Sub-Micron (DSM) IC Design, ASIC Design I & II, Data Structures and Algorithms I & II, Programming Tools and Environments, Applied Mathematical Programming, Custom VLSI Design, High Performance Computer Architecture, Parallel Computer Architecture, Network-on-a-Chip (NoC).
- PUBLICATIONS ◇ Can Sitik and Baris Taskin, *Iterative Skew Minimization for Low Swing Clocks*, to appear in Elsevier Integration, The VLSI Journal, November 2013.
- ◇ Can Sitik, Prawat Nagvajara and Baris Taskin, *A Microcontroller-Based Embedded System Design Course with PSoC3*, Proceedings of the IEEE International Conference on Microelectronics System Education (MSE), June 2013.
- ◇ Can Sitik and Baris Taskin, *Multi-Corner Multi-Voltage Domain Clock Mesh Design*, Proceedings of the ACM Great Lakes Symposium of VLSI (GLSVLSI), May 2013, pp. 209–214.
- ◇ Can Sitik and Baris Taskin, *Skew-Bounded Low Swing Clock Tree Optimization*, Proceedings of the ACM Great Lakes Symposium (GLSVLSI), May 2013, pp. 49–54 **Best Paper Nominee**.
- ◇ Can Sitik and Baris Taskin, *Implementation of Domain-Specific Clock Meshes for Multi-Voltage SoCs with IC Compiler*, Proceedings of the Synopsys User Group (SNUG) Conference Silicon Valley, March 2013.
- ◇ Can Sitik and Baris Taskin, *Multi-Voltage Domain Clock Mesh Design*, Proceedings of the IEEE International Conference on Computer Design (ICCD), October 2012, pp. 201–206.
- PROFESSIONAL ACTIVITIES ◇ ACM SIGDA University Booth Participation at Design Automation Conference (DAC) in Austin, Texas, 2013.
- ◇ ACM SIGDA Design Automation Summer School (DASS) Participation at Design Automation Conference (DAC) in Austin, Texas, 2013.
- SKILLS ◇ C, C++, Perl, Python, Tcl, Awk, Basic Java
- ◇ Pthread, OpenMP, CUDA
- ◇ Cadence – Virtuoso Suite, Spectre, PSpice
- ◇ Synopsys – Design Compiler, IC Compiler, StarRC, CustomSim, XA, HSpice
- ◇ VHDL, Verilog HDL
- ◇ gem5, Matlab, AMPL, LTSpice, Multisim, KeyCAD
- ◇ \LaTeX , vi, Office Suites
- ◇ Unix, Linux, Windows, DOS
- ACADEMIC HONORS AND AWARDS ◇ Best Paper Nomination at ACM International Great Lakes Symposium on VLSI (GLSVLSI) 2013 held in Paris, France (3 out of 238).

- ◇ George Hill, Jr. Fellow, Drexel University, 2012 – 2013.
- ◇ Scholarship to attend ACM SIGDA Design Automation Summer School (DASS) and ACM SIGDA University Booth at Design Automation Conference (DAC) 2013 held in Austin, Texas.
- ◇ Graduated with High Honors (top 6% of the graduating class) from the Department of Electrical and Electronics Engineering, METU, 2011.
- ◇ METU Development Foundation Scholarship, METU, 2007 – 2011.
- ◇ General Directorate of Higher Education Scholarship, Turkey, 2007 – 2011.
- ◇ Dean's List, Faculty of Engineering, METU, 2007 – 2011.

REFERENCES

- ◇ **Dr. Baris Taskin**
Associate Professor, Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA
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- ◇ **Dr. Prawat Nagvajara**
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Drexel University, Philadelphia, PA
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