Karthik Sangaiah

Ph.D. Candidate - Computer Engineering
Drexel University, Philadelphia, PA
Department of Electrical and Computer Engineering

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RESEARCH INTERESTS

Computer Engineering, Computer Architecture, Hardware-Software Co-Design, High Performance Computing, and Heterogeneous Architectures.

EDUCATION

◇ **Ph.D., Computer Engineering** — Expected Graduation, Sept. 2020
NSF GRFP Research Fellow, August 2014 – August 2017
Drexel University, Philadelphia, PA
Topic: Modeling and Simulation of CMPs and Communication Interconnects

◇ **M.S., Computer Engineering**, GPA: 3.95 — June 2012
Drexel University, Philadelphia, PA

◇ **B.S., Electrical and Electronics Engineering**, GPA: 3.95 — June 2012
Drexel University, Philadelphia, PA

PROFESSIONAL EXPERIENCE

◇ **Drexel University**, Philadelphia, PA
Department of Electrical and Computer Engineering

☐ **NSF GRFP Research Fellow & Research Assistant** — Sept. 2013 – Current
VLSI and Architecture Laboratory

- Developed modeling and simulation techniques for many-core CMPs
- Designed opportunistic computing architecture with on-chip in-network processing
- Built statistical regression framework for rapid design space exploration of CMP uncore
- Published in premier venues including: IEEE HPCA'20, ACM TACO'18, IEEE/ACM ICCAD'15

☐ **Teaching Assistant** — Sept. 2013 – Current

- Computer Organization & Architecture
- Advanced Programming for Engineers
- VLSI Digital Systems Projects

◇ **ARM Research**, Cambridge, UK

☐ **Research Intern** — June 2015 – Dec. 2015

- Investigated trace-driven simulation techniques to model ARM-based HPC CMPs
- Analyzed HPC thread behavior at scale with C++/Python gem5-based simulation tool
- Designed visualization tool to enable coarse-grained analysis of HPC thread behavior

◇ **Lockheed Martin MST**, Moorestown, NJ

☐ **Combat Systems Engineer** — July 2012 – Sept. 2013

- Designed FPGA-based solution for replacing custom VME sensor monitor embedded computer
- Performed system capacity analysis for optimizing application performance on server CMPs

☐ **R&D and Information Assurance Co-op** — March 2011 - Sept. 2011

- Evaluated Cisco Unified Computing System for combat ship system processing
- Executed vulnerability investigations and administered hardening of 60-node network

☐ **Computing and Network Infrastructure Co-op** — Sept. 2008 - Sept. 2010

- Wrote five trade studies for the customer based on research of advances in COTS hardware
- Provided network support during 12 and 24–hour stress and endurance tests of combat system
- Trained two team members in troubleshooting and designing components of combat system

SKILLS
- ◇ Architecture modeling tools: gem5, Sniper, zsim, McPAT, Orion, DSENT
- ◇ arm/x86 Assembly, C, C++, VHDL, Perl, Python, Basic Java, R
- ◇ Pthread, OpenMP, Cilk+, CUDA
- ◇ ModelSim, Xilinx ISE, EDK, System Generator, Matlab, WireShark
- ◇ LaTeX, vi, Office Suites
- ◇ Linux, Unix, Windows

SELECTED PROJECTS

◇ **SnackNoC: Opportunistic Processing in the Communication Layer**
- – Designed a dataflow-style platform for opportunistic computing within the communication layer
- – Created an ISA that leverages the traditional resources and topology of an NoC
- – Developed a cycle-accurate simulator in C++/Python
- – Modeled heterogeneous platforms of SnackNoC embedded in traditional HPC many-core CMPs
- – Publication in IEEE HPCA'20

◇ **SynchroTrace: Synchronization-Aware Traces for Simulation of Many-Core CMP Platforms**
- – Developed a fast and accurate trace-based simulator in C++/Python to model NoC-based CMPs
- – Extracted architecture-agnostic event traces to represent multi-threaded applications
- – Modeled ARM-based HPC many-core platforms
- – Investigated Static and Dynamic Thread Mapping based on application communication characterization
- – Developed a statistical regression framework to rapidly characterize the design space of the uncore
- – Publications in ACM TACO'18, IEEE/ACM ICCAD'15, IEEE ISPASS'15

◇ **Master's Thesis on Variable Fractional Delay (VFD) Filters on Reconfigurable Hardware**
- – Designed order-scalable and modular FIR filters
- – Developed hardware and software-based Lagrange coefficient computational unit
- – Tested and verified on Xilinx Virtex-6 and Spartan-6 FPGAs
- – Publication in IEEE MWSCAS'12

◇ **Evaluation of an Accelerator Architecture for Speckle Reducing Anisotropic Diffusion (SRAD)**
- – Accelerator proof-of-concept for SRAD medical imaging algorithm
- – Evaluated performance of developed SRAD accelerator against a GPU and a multi-threaded CPU
- – Publication in ACM CASES'11

◇ **Statistical Power Analysis for Estimating GPU Power Consumption via Machine Learning**
- – Online model-learning of power utilization of GPU functional units to estimate power in real-time
- – Generated GPU power and performance metrics of GPGPU benchmarks and GPU intensive applications

PUBLICATIONS
- ◇ **K. Sangaiah**, M. Lui, R. Kuttappa, B. Taskin, and M. Hempstead, "SnackNoC: Processing in the Communication Layer", *Proceedings of IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Feb. 2020.
- ◇ A. Hankin, T. Shapira, **K. Sangaiah**, M. Lui, M. Hempstead, "Evaluation of Non-Volatile Memory based Last Level Cache given Modern Use Case Behavior", *Proceedings of IEEE International Symposium on Workload Characterization (IISWC)*, Nov. 2019.
- ◇ M. Lui, **K. Sangaiah**, M. Hempstead, B. Taskin, "Towards Cross-Framework Workload Analysis via Flexible Event-Driven Interfaces", *Proceedings of IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 2018.
- ◇ **K. Sangaiah**, M. Lui, R. Jagtap, S. Diestelhorst, S. Nilakantan, A. More, B. Taskin, M. Hempstead, "SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multicore Simulation of CMP and HPC Workload", *ACM Transactions on Architecture and Code Optimization (TACO)*, Volume 15, Issue 1, April 2018.

- **K. Sangaiah**, B. Taskin, M. Hempstead, "Fast Multicore Simulation and Performance Analysis of HPC Applications with SynchroTrace", *Boston Area Architecture Workshop (BARC)*, 29 Jan. 2016.
- **K. Sangaiah**, M. Hempstead, B. Taskin, "Uncore RPD: Rapid Design Space Exploration of the Uncore via Regression Modeling", *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 7-10 Nov. 2015.
- S. Nilakantan, **K. Sangaiah**, A. More, G. Salvador, B. Taskin, M. Hempstead, "SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multi-core Simulation", *Proceedings of IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, 29-31 March 2015.
- **K. Sangaiah** and P. Nagvajara, "Variable fractional digital delay filter on reconfigurable hardware", *Proceedings of IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 5-8 August 2012, pages 430-433.
- S. Nilakantan, S. Annangi, N. Gulati, **K. Sangaiah**, M. Hempstead, "Evaluation of an accelerator architecture for Speckle Reducing Anisotropic Diffusion", *Proceedings of ACM International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, 9-14 Oct. 2011, pp.185-194.

Academic Honors and Awards

- NSF Graduate Research Fellowship Program Recipient — 2014 – 2017
  – Development of an Exascale Computing Co-Design Platform
- Drexel IEEE Graduate Forum, President — 2016 – 2017
  – IEEE Member (Member ID: 91247095)
- Drexel Fellowships Ambassador — 2015 – Current
- Weggle Family Fellowship Awardee, Drexel University — 2018
- George Hill, Jr. Fellow, Drexel University — 2014, 2015
- Graduated Summa Cum Laude with Honors, Drexel University — 2012
- Tau Beta Pi Scholar — 2011
- Dean's List, Drexel University — 2007 – 2012
- Eta Kappa Nu Vice President — 2011 – 2012
- Tau Beta Pi Vice President — 2010 – 2011

Relevant Graduate Coursework

- Network-on-Chip
- High Performance Computer Architecture
- Parallel Computer Architecture
- VLSI Design with FPGAs
- Data Structures and Algorithms
- Advanced Programming Techniques
- Embedded Systems
- Performance Analysis of Networking
- CMOS VLSI Circuit and Systems Design
- Fundamentals of Systems I & II

References

- **Dr. Baris Taskin**
  Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  E-mail: taskin@coe.drexel.edu
- **Dr. Mark Hempstead**
  Associate Professor, Department of Electrical and Computer Engineering
  Tufts University, Medford, MA
  E-mail: mark@ece.tufts.edu
- **Dr. Stephan Diestelhorst**
  System Architect
  Xilinx, Cambridge, England, United Kingdom
  E-mail: stephan.diestelhorst@gmail.com