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Leo Filippini

Summary I am a PhD student focusing on low-power VLSI systems, with a strong background in full-custom analog IC design and layout: for the past two years I've been designing CMOS circuits in deep-submicron technologies. I have cleanroom and tapeout experience and a sound understanding of transistor level design and device physics.

Experience

2013 - present **PhD candidate**, *Drexel University*, Philadelphia (PA).
My research group focuses on low-power methodologies for VLSI circuits. In particular, I am currently investigating flip-flop topologies for low-swing clock applications along with the feasibility of different adiabatic logic families.

2013 **Intern**, *Imec Belgium*, Heverlee (Belgium).
During this internship, which is also my Master's thesis, I designed an integrated transimpedance amplifier for capacitive ultrasonic transducers (CMUT).
Detailed achievements:
- Implementation of the transducer model in Cadence
- Theoretical comparison between different amplifier topologies
- Noise analysis
- Design of a topology new to the application
- Layouting and verification of a prototype IC in CMOS 180nm
- Tape-out

2010 **Intern**, *University of Brescia – Physics Department*, Brescia (Italy).
For four months I worked on my Bachelor's thesis: *Synthesis and integration of quantum dot semiconductors in third generation excitonic solar cells.* Along with my supervisors, we chemically synthesized different types of quantum-dots and realized many cells. I, in particular, took care of the substrate deposition and characterization, of the construction of the cells, and of their optical and electrical characterization. To do so, I used the following instruments: electronic load with 4-point probe, solar simulator, monochromator, lock-in amplifier (in order to measure cells' IPCE).

Education

2010 – 2013 **Master Degree**, *University of Brescia*, Brescia (Italy), *summa cum laude*.
Electronics Engineering

2011 **Erasmus program**, *Koç University*, Istanbul (Turkey), *GPA 4.0*.
Fall semester as an exchange student

2006 – 2010 **Bachelor Degree**, *University of Brescia*, Brescia (Italy), *91/110*.
Information Engineering

Computer skills

Cadence Virtuoso, Assura, Spectre, Encounter

Synopsys Custom Designer, DC, ICC

Programming Matlab, Python, Mathematica, LaTeX, Objective-C, Bash

Other GNU/Linux, Calibre, git, Agilent ADS

Relevant projects

Brescia – 2012 **Design and layout of a Recycling Folded Cascode (RFC) in CMOS 180 nm**.

Starting from the original RFC, I worked to reduce the voltage supply from 1.8 V to 1.2 V. I slightly modified the topology to fit the new supply voltage and I added a sub-circuit in order to increase the input common mode swing. Detailed achievements:

- Theoretical analysis of input and output swing, bias voltages, and gain
- Design of the circuit and corner analysis
- Hierarchical layout
- DRC, LVS, and extraction
- Simulation of the extracted view

Brescia – 2012 **Design and realization of a feedback circuit for precise capacitance measurement**.

In this work I designed a system for capacitance measurement and realized it on a double sided PCB. The circuit, running at 10 kHz, uses synchronous modulation to compare the device under test with a reference capacitor of known value. The range of the circuit goes from 10 pF to 10 nF. The measure is provided through a DC voltage that is linear with the unknown capacitance.

Istanbul – 2011 **Design, fabrication, and stress measurement of electroplated nickel cantilevers**.

The goal of the project was to familiarize with cleanroom operation and with several micro-fabrication steps. After drawing the mask layout with *Tanner EDA L-Edit*, I assisted with several procedures:

- Wafer preparation
- Sputtering of seed layer (Gold)
- Photoresist spin coating
- Lithography
- Nickel electroplating
- Photoresist strip

This represented a great experience and taught me how to behave in a cleanroom.

Brescia – 2009 **Characterization of an amplifier using Automatic Test Equipment**.

During this project I designed and realized an instrumentation amplifier based on three $\mu A741$ operational amplifiers. Since the goal of the project was to get acquainted with ATE instrumentation, I realized a virtual instrument in *Labview SignalExpress* in order to automatically measure gain, bandwidth, and CMRR over the amplifier's bandwidth. The work was carried out using a *National Instruments PXI* platform.

Languages

Italian Native

English TOEFL iBT: 107/120

GRE Revised: quantitative 163 (88%), verbal 160 (83%)

Honors

2011 Winner of European *Lifelong Learning Program* scholarship

Publications

Can Sitik, Leo Flippini, Emre Salman, and Baris Taskin, *"High Performance Low Swing Clock Tree Synthesis with Custom D Flip-Flop Design"*, ISVLSI 2014