Karthik Sangaiah

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RESEARCH INTERESTS

Heterogeneous computing platforms, communication interconnects, high performance computing, and resource-efficient computer architecture.

EDUCATION

- **Ph.D., Computer Engineering**, September 2013 – Current.
  NSF GRFP Research Fellow, August 2014 – August 2017
  Drexel University, Philadelphia, PA.
  Topic: Design of Interconnects and Heterogeneous Architectures
- **M.S., Computer Engineering**, GPA: 3.95, June 2012.
  Drexel University, Philadelphia, PA.
- **B.S., Electrical and Electronics Engineering**, GPA: 3.95, June 2012.
  Summa Cum Laude
  Drexel University, Philadelphia, PA.

PUBLICATIONS

- K. Sangaiah, M. Lui, R. Kuttappa, B. Taskin, and M. Hempstead, "SnackNoC: Processing in the Communication Layer", *Proceedings of IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Feb. 2020.
- A. Hankin, T. Shapira, K. Sangaiah, M. Lui, M. Hempstead, "Evaluation of Non-Volatile Memory based Last Level Cache given Modern Use Case Behavior", *Proceedings of IEEE International Symposium on Workload Characterization (IISWC)*, Nov. 2019.
- M. Lui, K. Sangaiah, M. Hempstead, B. Taskin, "Towards Cross-Framework Workload Analysis via Flexible Event-Driven Interfaces", *Proceedings of IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 2018.
- K. Sangaiah, M. Lui, R. Jagtap, S. Diestelhorst, S. Nilakantan, A. More, B. Taskin, M. Hempstead, "SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multicore Simulation of CMP and HPC Workload", *ACM Transactions on Architecture and Code Optimization (TACO)*, Volume 15, Issue 1, April 2018.
- K. Sangaiah, B. Taskin, M. Hempstead, "Fast Multicore Simulation and Performance Analysis of HPC Applications with SynchroTrace", *Boston Area Architecture Workshop (BARC)*, 29 Jan. 2016.
- K. Sangaiah, M. Hempstead, B. Taskin, "Uncore RPD: Rapid Design Space Exploration of the Uncore via Regression Modeling", *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 7-10 Nov. 2015.
- S. Nilakantan, K. Sangaiah, A. More, G. Salvador, B. Taskin, M. Hempstead, "SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multi-core Simulation", *Proceedings of IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, 29-31 March 2015.
- K. Sangaiah and P. Nagvajara, "Variable fractional digital delay filter on reconfigurable hardware", *Proceedings of IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 5-8 August 2012, pages 430-433.
- S. Nilakantan, S. Annangi, N. Gulati, K. Sangaiah, M. Hempstead, "Evaluation of an accelerator architecture for Speckle Reducing Anisotropic Diffusion", *Proceedings of ACM International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, 9-14 Oct. 2011, pp.185-194.

PROFESSIONAL EXPERIENCE

◇ **NSF GRFP Research Fellow & Research Assistant**, (Sept. 2013 – current)
VLSI Laboratory, Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA, USA

– Architecture of in-network processing and heterogeneous platforms
– Modeling and simulation techniques for massively many-core architectures
– Regression techniques for design space exploration of the chip multiprocessor uncore
– Application-aware memory and NoC co-design

◇ **Research Internship**, (June. 2015 – Dec. 2015)
ARM Research
Cambridge, UK

– Extension of PhD project SynchroTrace to support ARM-based CMPs
– Exploration of HPC platforms with SynchroTrace
– Design of visualization tool to enable coarse-grained analysis of HPC thread behavior

◇ **Teaching Assistant**, (Sept. 2013 – current)
Department of Electrical and Computer Engineering & College of Engineering
Drexel University, Philadelphia, PA, USA

– Computer Organization & Architecture
– Design with Microcontrollers & Embedded Design
– Advanced Programming for Engineers
– Digital Systems Projects

◇ **Combat Systems Engineer**, (July 2012 – Sept. 2013)
Lockheed Martin MST
Moorestown, NJ

◇ **R&D and Information Assurance (IA) Co-op**, (March 2011 - Sept. 2011)
Lockheed Martin MST
Moorestown, NJ

◇ **Computing and Network Infrastructure (CNI) Co-op**, (Sept. 2008 - Sept. 2010)
Lockheed Martin MST
Moorestown, NJ

SELECTED PROJECTS

◇ **SnackNoC**
– Proposed an area-efficient dataflow-style platform for computing within the communication layer
– Created an ISA that leverages the traditional resources and topology of an NoC
– Developed a cycle-accurate simulation model in C++/Python, within the gem5 framework
– Modeled heterogeneous platforms of SnackNoC embedded in traditional HPC many-core CMPs

◇ **SynchroTrace**
– Developed a fast and accurate trace-based simulator in C++/Python to model full-system NoC-based CMPs
– Extracted event traces of multi-threaded applications to drive the gem5-based model
– Supported modeling ARM-based HPC many-core platforms
– Investigated static and Dynamic Thread Mapping based on application communication characterization
– Developed a regression model framework for rapid design space exploration of the NoC-based uncore

◇ **Master's Thesis on Variable Fractional Delay (VFD) Filters on Reconfigurable Hardware**
– Based on order-scalable and modular FIR filters
– Developed hardware and software-based Lagrange coefficient computational unit
– Tested and verified on Xilinx Virtex-6 and Spartan-6 FPGAs

◇ **Evaluation of an Accelerator Architecture for Speckle Reducing Anisotropic Diffusion (SRAD)**
– Accelerator proof of concept for SRAD medical imaging algorithm
– Compared performance of in-lab developed SRAD accelerator with a massively parallel GPU and multi-threaded CPU SRAD algorithm

◇ **Statistical Power Analysis for Estimating GPU Power Consumption via Machine Learning**
– Online statistical model-learning of power utilization of GPU functional units to estimate power utilization in real-time
– Empirical data generated by GPGPU benchmarks and GPU intensive applications

ACADEMIC HONORS AND AWARDS

◇ NSF Graduate Research Fellowship Program Recipient, 2014.
◇ Drexel IEEE Graduate Forum, President, Fall 2016 – Fall 2017.
– IEEE Member (Member ID: 91247095), Winter 2011 – Present
◇ Weggle Family Fellowship Awardee, Drexel University, 2017 – 2018.
◇ George Hill, Jr. Fellow, Drexel University, 2013 – 2014, 2014 – 2015.
◇ Drexel Fellowships Ambassador, Fall 2015 – Present.
◇ Graduated Summa Cum Laude from the Department of Electrical and Computer Engineering, Drexel University, 2012.
◇ Tau Beta Pi Scholar, Spring 2011.
◇ Dean's List, Drexel University, 2007 – 2012.
◇ Eta Kappa Nu Vice President, Spring 2011 – Spring 2012.
◇ Tau Beta Pi Vice President, Fall 2010 – Fall 2011.

SKILLS

◇ Architecture modeling tools: gem5, Sniper, zsim, McPAT, Orion, DSENT
◇ arm/x86 Assembly, C, C++, VHDL, Perl, Python, Basic Java, R
◇ Pthread, OpenMP, Cilk+, CUDA
◇ ModelSim, Xilinx ISE, EDK, & System Generator, Matlab, WireShark
◇ LaTeX, vi, Office Suites
◇ Unix, Linux, Windows, DOS

RELEVANT GRADUATE COURSEWORK

◇ Network-on-a-Chip (NoC), High Performance Computer Architecture, Parallel Computer Architecture, VLSI Design with FPGAs, Data Structures and Algorithms, Advanced Programming Techniques, Embedded Systems, Performance Analysis of Computer Networking, CMOS VLSI Circuit and Systems Design, Fundamentals of Systems I & II.

REFERENCES

◇ **Dr. Baris Taskin**
Professor, Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA
E-mail: taskin@coe.drexel.edu

◇ **Dr. Mark Hempstead**
Associate Professor, Department of Electrical and Computer Engineering
Tufts University, Medford, MA
E-mail: mark@ece.tufts.edu

◇ **Dr. Stephan Diestelhorst**
System Architect
Xilinx, Cambridge, England, United Kingdom
E-mail: stephan.diestelhorst@gmail.com