Scott P. Lerner

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EDUCATION

- **Ph.D., Electrical Engineering**, GPA: 4.0, (expected graduation 2018).
  Drexel University, Philadelphia, PA.
- **B.S., Electrical Engineering**, GPA: 3.5, 2014.
  Drexel University, Philadelphia, PA.
- **B.S., Computer Engineering**, GPA: 3.5, 2014.
  Drexel University, Philadelphia, PA.

PROFESSIONAL EXPERIENCE

- **Research Fellow / PhD Student**, (September 2014 – current)
  VLSI Laboratory, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA, USA

  – PhD student and member of the VLSI lab
  – **NSF GRFP** recipient for research on Hardware resilience
  – Published about linear timing models for clock buffers
  – Studying Low-power circuits using the following techniques:
    – Clock Gating with delay estimates and optimal sizing
    – Low-power, high-performance enabled by low-swing circuits
  – Investigating Physical Design resilience by using Software workload-awareness

- **Undergraduate Research Assistant – VLSI Laboratory**, (January 2012 – August 2014)
  VLSI Laboratory, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA, USA

  – NSF Research Experience for Undergraduate (REU) grant
  – Clock tree mesh optimization algorithms (500 lines C++)
  – Implemented an advanced algorithm for clock buffer sizing (700 lines C++)
  – Custom VLSI Design, ASIC Design I/II, Network-on-Chip, Computer Architecture courses
    – Cadence: RTL Compiler, Encounter, Virtuoso, Spectre
    – Synopsys: 1) DC for synthesis, 2) ICC for physical design floorplanning, placement, routing, CTS,
    – 3) Primetime for Static Timing Analysis 4) HSPICE for simulation
    – BookSim, HNoC for Network-on-Chip simulation
  – Senior Design Project on Wireless Interconnect Design for 2D and 3D ICs
    – NoC simulation, HFSS modeling, RF and Antenna modeling

- **Undergraduate Research Assistant – DPAC Laboratory**, (January 2012 – August 2014)
  DPAC Laboratory, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA, USA

  – Validated binary instrumentation error compared to full-system simulation
  – Network-on-Chip design space exploration of resource optimization
  – Automated verification testing for CPU event traces

- **Co-op Technical Senior**, (April 2013 – September 2013)
  Lockheed Martin
  Cherry Hill, NJ, USA

  – Optimized software defined radios for spectrum denial capabilities
  – Formulated programs to allow for large data sets to be analyzed quickly
  – Obtained and maintained a **Secret level security clearance**

◇ **Software Developer**, (January 2012 – September 2012)
Software Support-PMW
Sewell, NJ, USA

– Designed five iPhone/iPad applications targeted for commercial sales
– Implemented a point-of-sale system on the iOS platform
– Maintained backend database communication to apache server

◇ **DRAM Product Engineer**, (March 2011 – September 2011)
Micron Technologies Inc.
Boise, ID, USA

– Performed functional testing and verification on packaged and bare memory die
– Diagnosed part failures for physical design and signal integrity issues
– Worked with a team to brainstorm and apply innovative fixes to new products

PUBLICATIONS

◇ C. Sitik, W. Liu, S. Lerner, E. Salman, and B. Taskin, *Low Swing Clock Tree Synthesis with Local Gate Clusters*, in preparation for a journal submission.

◇ S. Nilakantan, S. Lerner, M. Hempstead and B. Taskin, *Can you trust your memory trace?: A comparison of memory traces from binary instrumentation and simulation*, Nominated for best paper at the IEEE International Conference VLSID, pp.135-140 January 2015.

◇ Can Sitik, Scott Lerner and Baris Taskin, *Timing Characterization of Clock Buffers for Clock Tree Synthesis*, Proceedings of the IEEE International Conference on Computer Design (ICCD), pp.230-236 October 2014.

CLASS PROJECTS

◇ **Custom VLSI OpenSPARC Implementation, VLSI 2**
– Design Compiler used to synthesize an OpenSPARC core for 90nm
– Placed and routed the design in ICC using SAED libraries
– Achieved ultra low-power by experimenting with design parameters

◇ **Boolean SAT Solver, EDA 1**
– Implemented a boolean SAT solver in C++ (1000 lines)
– DPLL and 2-literal watching used for speedup
– Variable weighting using JW-score
– 100 variable SAT benchmarks solved in 15ms

◇ **Unate Recursive Tautology Code, EDA 1**
– Implemented unate tautology in C++ (200 lines)
– Shannon Expansion used to recursively determine tautology

PRESENTATIONS

◇ C. Sitik, S. Lerner, and B. Taskin, *Timing Characterization of Clock Buffers for Clock Tree Synthesis*, Presentation given at IEEE International Conference on Computer Design (ICCD), Oct 2014.

◇ S. Lerner, V. Pano, and B. Taskin, *Wireless Network on Chip*, Poster presented at Mid-Atlantic ASEE, November 2014.

◇ S. Lerner, *Arduino Robotics in the Classroom*, Poster presented at Mid-Atlantic ASEE, November 2014.

◇ S. Lerner, and B. Taskin, *Low-Power Clock Network Designs*, Poster presented at IEEE Design Automation Conference, June 2014.

◇ Scott Lerner, R. Welliver, B. Derveni, C. Schoenfield, I. Yilmaz , *MotionExplorer, A Leap Motion-Controlled Electric Wheelchair*, presented at Philly Codefest, February 2014.

◇ Can Sitik, Scott Lerner, and Baris Taskin, *Low-Power/High-Performance Clock Network Design for Microprocessors*, Poster presented at Upsilon Pi Epsilon Research Reception, February 2013.

TEACHING ASSISTANT COURSEWORK

- Advanced Programming, Winter 2014-15, Junior Level Class
- Embedded Systems, Fall 2014-15, Junior Level Class
- Introduction to Computer Networks, Fall 2014-15, Junior Level Class
- Design with Microcontrollers, Summer 2013-14 Junior Level Class
- Network-on-chip I, Fall 2013-14, Graduate Level Class
- ASIC Design II, Spring 2013-14, Graduate Level Class

PROFESSIONAL ACTIVITIES

- Technical Chair - Drexel IEEE Graduate Society 2014-Current
- Member - Drexel IEEE Undergraduate 2013, 2014
- Student Member - Institute of Electrical and Electronics Engineers 2010-Current

VOLUNTEER ACTIVITIES

- STAR Mentor - Low-power Circuit Design, Drexel University 2013-14
- Freshman Design Mentor - Wireless HDMI, Drexel University 2013-14
- TechGirlz Workshop held in Philadelphia, PA
- SeaPerch Underwater Robotics Challenge 2014 held in Philadelphia, PA
- Biomedical Sciences and Professional Studies Graduate Orientation 2014 held in Philadelphia, PA
- City Year Park Cleanup in Philadelphia, PA

SKILLS

- C, C++, Python, Objective-C (10,000+ lines written)
- Pthread, OpenMP, Tcl, Assembly (MIPS), SystemC (1,000+ lines written)
- Verilog HDL, Matlab, Arduino, LaTeX (1,000+ lines written)
- Synopsys – Design Compiler, IC Compiler, HSpice
  Cadence – RTL Compiler, Encounter, Virtuoso Suite, Spectre, PSpice
- vi, Office Suites
- Unix, Linux, Windows, DOS

ACADEMIC HONORS AND AWARDS

- NSF Graduate Research Fellowship (GRFP) Program Recipient, 2015.
- National Defense Science & Engineering Graduate (NDSEG) Fellowship Recipient, 2015.
- NSF Research Experience for Undergraduate (REU) Grant 2014
- A. Richard Newton Young Fellow Award 2014
- Dean's Choice Award at Philly Codefest for MotionExplorer 2014 held in Philadelphia, PA.
- NextFab Innovation Award at Philly Codefest for MotionExplorer 2014 held in Philadelphia, PA.
- Doctor Thomas Moore Endowed Grant 2014
- Dean's List, 2009, 2010, 2011, 2012, 2013, 2014.

REFERENCES

- **Dr. Baris Taskin**
  Associate Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  E-mail: taskin@coe.drexel.edu
- **Dr. Mark Hempstead**
  Assistant Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  E-mail: mhempstead@coe.drexel.edu