A. Can Sitik

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RESEARCH INTERESTS

Low Power Circuits and Architectures, Design and Automation Algorithms for Clocking, System-on-Chip (SoC) Design.

EDUCATION

- **Ph.D., Computer Engineering**, September 2011 – Current (expected December 2015).
  Drexel University, Philadelphia, PA.
  Topic: Design and Automation of Low-Power Clock Distribution Networks
- **M.S., Computer Engineering**, GPA: 3.86, December 2013.
  Drexel University, Philadelphia, PA.
  Concentration: Computer Architecture, Algorithms.
- **B.S., Electrical and Electronics Engineering**, GPA: 3.64 (with High Honors), July 2011.
  METU, Ankara, Turkey.
  Concentration: Computer Architecture, VLSI.

PROFESSIONAL EXPERIENCE

- **Research Assistant**, (September 2011 – March 2014, September 2014 – current)
  VLSI Laboratory, Department of ECE, Drexel University, Philadelphia, PA, USA
  - Developed power and timing optimization algorithms
  - Developed methodologies for physical design of SoCs
  - Explored EDA techniques for logical and physical synthesis
- **Graduate Technical Intern**, (March 2014 – September 2014)
  PrimeTime R&D Team, Synopsys Inc, Mountain View, CA, USA
  - Directly contributed to an ongoing project to enhance clock timing (≈20,000 lines of C code)
  - Generated related test cases for debugging and verification (≈5,000 lines of Tcl script)
- **Teaching Assistant**, (September 2011 – March 2014, January 2015 – current)
  Department of ECE & College of Engineering, Drexel University, Philadelphia, PA, USA
  - ECEC 671: EDA for VLSI I (Winter 2015)
  - ECEC 304: Design with Microcontrollers (Winter 2012–2014, Summer 2012,2013)
  - ECEC 302: Digital Systems Projects (Fall 2013, Spring 2013)
  - ECEE 421: Advanced Electronics (Fall 2011)
  - ENGR 231: Linear Engineering Systems (Fall 2012, Spring 2012)
- **Undergraduate Research Assistant**, (September 2010 – June 2011)
  DSP Laboratory, Department of EE, METU, Ankara, Turkey
  - Embedded Software Development for efficient implementation of DSP algorithms
  - Embedded C Coding for TI's TMS3206747 DSP
- **Undergraduate R&D Intern**, (June 2010 – July 2010)
  ASELSAN Inc, Ankara, Turkey (Leading Defense Industry Company)
  - Developed an embedded software for target detection in infrared cameras (≈1,000 lines of C code).
  - Participated in the field tests and performance analysis of infrared cameras.

SELECTED PROJECTS

◇ **Clock Tree/Mesh Synthesis, Drexel University**
– Multi-voltage domain clock mesh design (integrated into IC Compiler physical design flow)
– Software-application-aware clock gating
– Interconnect-driven CTS for CMOS and FinFET technologies

◇ **Automation of Low Swing Clocking, Drexel University**
– Skew minimization for low swing clocking (integrated into IC Compiler physical design flow)
– Power and timing characterization of clock buffers under variations
– Low swing CTS tool (≈1,000 lines of Perl script)

◇ **Defrauder & Confuser Algorithm for Submarines, METU**
– A smart algorithm that shuffles SONAR signals in order to cause false detection on the opposing submarines, funded by the Scientific and Technological Research Council of Turkey (NSF equivalent).
– Implemented DSP algorithms on both TI's TMS320 processor using C/C++.

◇ **Smart Self-Parking Truck & Trailer System, Senior Design, METU**
– A smart truck that can park forward or backward considering its passive trailer, into predefined slots on a platform.
– Designed and implemented a parking algorithm (≈2,000 lines of C code).
– Designed the peripheral circuitry to interface the microcontroller unit to the sensors and motors.

RELEVANT GRADUATE COURSEWORK

High Performance Computer Architecture, Parallel Computer Architecture, Network-on-a-Chip (NoC), Data Structures and Algorithms I & II, Programming Tools and Environments, Applied Mathematical Programming, EDA for VLSI I & II, ASIC Design I & II.

PUBLICATIONS

Journals

[J2] Can Sitik, Emre Salman, Leo Filippini, Sung Jun Yoon and Baris Taskin, *FinFET-Based Low Swing Clocking*, (accepted to) ACM Journal of Emerging Technologies in Computing (JETC), 2015.

[J1] Can Sitik and Baris Taskin, *Iterative Skew Minimization for Low Swing Clocks*, Elsevier Integration, The VLSI Journal, Vol. 47, No. 3, pp. 356–364, June 2014.

Conferences

[C10] Mallika Rathore, Emre Salman, Can Sitik and Baris Taskin, *A Novel Static D Flip-Flop Topology for Low Swing Clocking*, to appear in the Proceedings of ACM Great Lakes Symposium on VLSI (GLSVLSI), May 2015.

[C9] Weicheng Liu, Emre Salman, Can Sitik and Baris Taskin, *Clock Skew Scheduling in the Presence of Heavily Gated Clock Networks*, to appear in the Proceedings of ACM Great Lakes Symposium on VLSI (GLSVLSI), May 2015.

[C8] Weicheng Liu, Emre Salman, Can Sitik and Baris Taskin, *Enhanced Level Shifter for Multi-Voltage Operation*, to appear in the Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), May 2015.

[C7] Can Sitik, Scott Lerner and Baris Taskin, *Timing Characterization of Clock Buffers for Clock Tree Synthesis*, Proceedings of the IEEE International Conference on Computer Design (ICCD), October 2014, pp. 230–236.

[C6] Can Sitik, Leo Filippini, Emre Salman and Baris Taskin, *High Performance Low Swing Clock Tree Synthesis with Custom D Flip-Flop Design*, Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July 2014, pp. 498–503.

[C5] Can Sitik, Prawat Nagvajara and Baris Taskin, *A Microcontroller-Based Embedded System Design Course with PSoC3*, Proceedings of the IEEE International Conference on Microelectronics System Education (MSE), June 2013, pp. 28–31.

[C4] Can Sitik and Baris Taskin, *Multi-Corner Multi-Voltage Domain Clock Mesh Design*, Proceedings of the ACM Great Lakes Symposium of VLSI (GLSVLSI), May 2013, pp. 209–214.

[C3] Can Sitik and Baris Taskin, *Skew-Bounded Low Swing Clock Tree Optimization*, Proceedings of the ACM Great Lakes Symposium (GLSVLSI), May 2013, pp. 49–54 **Best Paper Nominee**.

[C2] Can Sitik and Baris Taskin, *Implementation of Domain-Specific Clock Meshes for Multi-Voltage SoCs with IC Compiler*, Proceedings of the Synopsys User Group (SNUG) Conference Silicon Valley, March 2013.

[C1] Can Sitik and Baris Taskin, *Multi-Voltage Domain Clock Mesh Design*, Proceedings of the IEEE International Conference on Computer Design (ICCD), October 2012, pp. 201–206.

PROFESSIONAL ACTIVITIES

- Reviewer at Journal of Circuits, Systems and Computers (JCSC), 2014.
- ACM SIGDA University Booth Participation at Design Automation Conference (DAC) in Austin, Texas, 2013.
- ACM SIGDA Design Automation Summer School (DASS) Participation at Design Automation Conference (DAC) in Austin, Texas, 2013.

SKILLS

- C, C++, Perl, Python, Tcl
- gem5, Matlab, AMPL
- Pthread, OpenMP, CUDA
- Synopsys – Design Compiler, IC Compiler, HSPICE, PrimeTime Suite, StarRC, CustomSim, XA Cadence – Virtuoso Suite, Spectre, PSpice
- VHDL, Verilog HDL
- LaTeX, Unix, Linux

ACADEMIC HONORS AND AWARDS

- Best Paper Nomination at ACM International Great Lakes Symposium on VLSI (GLSVLSI) 2013 held in Paris, France (3 out of 238).
- ACM SIGDA travel grant for SIGDA University Booth presentation at Design Automation Conference (DAC) 2013 held in Austin, Texas.
- Leroy L. Rosser Fellowship, College of Engineering, Drexel University, 2013 – 2014, awarded to 1 graduate student per department based on academic merit.
- Allen Rothwarf Fellowship, Department of ECE, Drexel University, 2013 – 2014, awarded to 2 graduate students based on academic merit.
- George Hill, Jr. Fellowship, College of Engineering, Drexel University, 2012 – 2013, awarded to 1 graduate student per department based on academic merit.
- Graduated with High Honors (top 6% of the graduating class) from the Department of Electrical and Electronics Engineering, METU, 2011.
- METU Development Foundation Scholarship, METU, 2007 – 2011.
- General Directorate of Higher Education Scholarship, Turkey, 2007 – 2011.

PATENTS

- Baris Taskin and Can Sitik, *Methods and Computer-Readable Media for Synthesizing a Multi-Corner Mesh-Based Clock Distribution Network for a Multi-Voltage Domain and Clock Meshes and Integrated Circuits*, U.S. Patent Application No. 61/985,657 filed on 04/29/2014.

REFERENCES

- **Dr. Baris Taskin**
  Associate Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  E-mail: taskin@coe.drexel.edu
- **Dr. Prawat Nagvajara**
  Associate Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
  E-mail: nagvajara@ece.drexel.edu