

# Vasil Pano

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- EDUCATION
- ◇ **Ph.D., Electrical Engineering**, (expected graduation 2018).  
Drexel University, Philadelphia, PA.
  - ◇ **B.S., Computer Engineering**, 2014.  
Drexel University, Philadelphia, PA.
- PROFESSIONAL EXPERIENCE
- ◇ **Research Fellow / Ph.D. Student**, (September 2014 – current)  
VLSI and Architecture Laboratory, Department of Electrical and Computer Engineering  
Drexel University, Philadelphia, PA, USA
    - Ph.D. student and member of the VLSI and Architecture lab
    - Studying Computer Architecture focusing primarily on:
      - Computer memory subsystem design and cache coherence protocols
      - Network-on-Chip topologies and routing algorithms
    - Current research projects:
      - Implementing a novel multi-channel DRAM architecture within Gem5 (using DRAMSim2)
      - Implementing a custom Token cache coherence protocol within Gem5 (using SLICC)
      - Designed multiple clustered architectures within Gem5 (using Garnet/Ruby)
  - ◇ **Undergraduate Research Assistant – VLSI Laboratory**, (April 2013 – July 2014)  
VLSI Laboratory, Department of Electrical and Computer Engineering  
Drexel University, Philadelphia, PA, USA
    - Senior Design Project on Wireless Interconnect Design for 2D and 3D ICs
      - NoC simulation, HFSS modeling, RF and antenna modeling
    - Network-on-Chip, Computer Architecture, Custom VLSI Design, ASIC Design I/II courses
      - DragonNoC, Booksim and HNOG (OMNET++ based simulator) for NoC simulation
      - Gem5 (Ruby and Garnet) for full-system, SynchroTrace for trace-based simulation
      - Cadence: RTL Compiler, Encounter, Virtuoso
      - Synopsys: 1) DC for synthesis, 2) ICC for physical design
      - 3) Primitime for Static Timing Analysis 4) HSPICE for simulation
  - ◇ **Undergraduate Research Assistant – DPAC Laboratory**, (June 2013 – July 2014)  
DPAC Laboratory, Department of Electrical and Computer Engineering  
Drexel University, Philadelphia, PA, USA
    - Implemented custom barrier synchronization method to the in-house SynchroTrace simulator
    - Multi-threaded trace-based system simulation for evaluating many-core architectures and NoCs
    - Application-aware memory and NoC co-design
    - Benchmark analysis (Splash-2x and PARSEC 3.0) on Synchrotrace

- ◇ **Outage Analysis Technologies Intern**, (March 2013 – September 2013)  
PJM Interconnection  
Norristown, PA, USA
  - Thorough understanding of Software Development Life Cycle (SDLC) and Waterfall Methodology
  - Created and maintained database design with detailed description of logical entities and physical tables
  - Expertise in writing functional specifications and translating business requirements to technical specifications
  - Extensive experience in manual and automated testing of applications
- ◇ **Operations Planning Intern**, (April 2012 – March 2013)  
PJM Interconnection  
Norristown, PA, USA
  - Responsible for performing production and regression testing the proprietary software called eDART
  - Effectively coordinated with member companies and collected time sensitive information critical to reliability
  - Manually check one-line diagram information for accuracy and update databases accordingly
  - Consolidated a Software Manual and Quick Reference Guide of eDART for external and internal users

PUBLICATIONS ◇ Y. Liu, V. Pano, D. Patron, K. Dandekar and B. Taskin, *Innovative Propagation Mechanism for Inter-chip and Intra-chip Communication*, Proceedings of the IEEE Wireless and Microwave Technology Conference (WAMICON), pp.1-6 April 2015.

GRADUATE COURSEWORK ◇ High Performance Computer Architecture, Parallel Computer Architecture, Network-on-a-Chip (NoC)  
 ◇ EDA for VLSI I & II, ASIC Design I & II, Custom VLSI  
 ◇ Data Structures and Algorithms, Systems Programming, Internet Architecture and Protocols I & II

#### PRESENTATIONS

- ◇ V. Pano, M. Lui, M. Hempstead and B. Taskin, *Sigil and SynchroTrace: Communication-Aware Workload Profiling and Memory-NoC Simulation*, Tutorial presented at IEEE International Conference on Computer Design (ICCD), 2015.
- ◇ V. Pano, S. Lerner, and B. Taskin, *Wireless Network-on-Chip*, Poster presented at American Society for Engineering Education (ASEE), November 2014.

TEACHING ASSISTANT COURSEWORK ◇ Computation Lab I, Fall 2015-2016, Freshmen Level Class  
 ◇ Introduction to Parallel Computer Architecture, Fall 2015-16, Graduate Level Class  
 ◇ Systems Programming, Summer 2014-15, Junior Level Class  
 ◇ Digital Systems Projects, Spring 2014-15, Junior Level Class  
 ◇ Internet Architecture and Protocols, Winter 2014-15, Junior Level Class  
 ◇ Digital Logic Design, Fall 2014-15, Sophomore Level Class  
 ◇ ASIC Design II, Spring 2013-14, Graduate Level Class  
 ◇ Network-on-chip I, Fall 2013-14, Graduate Level Class

VOLUNTEER ACTIVITIES ◇ Senior Design Mentor - Wireless DRAM Solution, Drexel University 2015-16  
 ◇ Intern Supervisor (Isikcan Yilmaz) - Gem5 memory study (using Ruby), Drexel University 2015  
 ◇ STAR Mentor (Eonides Neto)- Router Architecture for Network-on-Chip, Drexel University 2015  
 ◇ Freshman Design Mentor - Wireless HDMI, Drexel University 2013-14

- SKILLS ◇ C, C++, SystemC, Python  
◇ Pthread, OpenMP, CUDA  
◇ Verilog HDL, Matlab, L<sup>A</sup>T<sub>E</sub>X  
◇ Synopsys – Design Compiler, IC Compiler, HSpice  
Cadence – RTL Compiler, Encounter, Virtuoso Suite

- ACADEMIC ◇ Dean's List, 2009, 2010, 2011, 2012, 2013, 2014  
HONORS AND ◇ Dean's Scholarship, Drexel University, September 2009 – June 2014  
AWARDS ◇ DU Endowed Scholarship, Drexel University, September 2009 – June 2014

- REFERENCES ◇ **Dr. Baris Taskin**  
Associate Professor, Department of Electrical and Computer Engineering  
Drexel University, Philadelphia, PA  
E-mail: [taskin@coe.drexel.edu](mailto:taskin@coe.drexel.edu)
- ◇ **Dr. Mark Hempstead**  
Associate Professor, Department of Electrical and Computer Engineering  
Tufts University, Medford, MA  
E-mail: [mark.hempstead@tufts.edu](mailto:mark.hempstead@tufts.edu)