Vinayak Honkote

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EDUCATION

- **Ph.D., Electrical Engineering**, (2006 – 2010).
  Drexel University, Philadelphia, PA, USA.
  Topic: Design Automation and Analysis of Resonant Clocking Technologies.
- **M.S., Electrical Engineering**, (2004 – 2006).
  Drexel University, Philadelphia, PA, USA.
- **B.E., Electronics and Communications Engineering**, (1999 – 2003).
  Bangalore Institute of Technology, Visvesvaraya Technological University, Bangalore, India.

RESEARCH INTERESTS

Electronic design automation (EDA) and VLSI physical design in general including clock network design, routing, design for manufacturing (DFM), digital integrated circuits, low power VLSI circuits, emerging technologies, interconnects and clocking for SOCs and multi-core systems.

PROFESSIONAL EXPERIENCE

- **Freshman Design Fellow**, (09/2009 – 09/2010)
  Co-teaching (with a faculty instructor) engineering design laboratory sequence
  for 4 freshman sections, each consisting of 32 students.
  Drexel University, Philadelphia, PA
- **Adjunct Primary Instructor**, (Summer 2009 and Summer 2008)
  Richard C. Goodwin College of Professional Studies, Drexel University, Philadelphia, PA
- **Research Assistant and Teaching Assistant**, (08/2006 – 11/2010)
  Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA
- **Internship - Junior Project Manager**, (06/2005 – 12/2005)
  Siemens Medical Solutions, Malvern, PA, USA
  – Responsibilities included decision making, performance analysis, module testing.
  – Hands-on experience with project management tools.
- **Full-time Engineer**, (07/2003 – 08/2004)
  Larsen & Toubro Infotech Ltd., Bangalore, India
  – Worked on wireless CDMA systems.
  – Developed and tested the ATM base station server modules in C++ (15,000 lines of C++).
  – Research work on CDMA and ATM networks.

SELECTED PROJECTS

- **Custom Rotary Clock Router**
  – Clock routing and physical design for non-regular rotary rings
  – 10,000 lines of C++, routing, timing algorithms
  – Simulation of rotary rings in hspice
- **Skew and Wirelength Analysis for Resonant Clocking Technologies**
  – Zero clock skew synchronization with rotary clocking
  – 20,000 lines of C++, wire routing, placement algorithms
  – Skew and wirelength analysis for rotary clocking and standing wave technologies
- **Optimization Algorithms for Resonant Clocking Technologies**
  – Capacitance balancing algorithms for rotary clocking and standing wave technologies
  – Linear programming, integer programming, heuristic, statistics, large-scale optimization
  – Simulation of capacitance load balanced rotary rings in hspice
- **Statistical Timing Analysis Tool** [Course Project - CAD for VLSI design]
- **Implementation of Advanced Filters on FPGA** [Course Project - Advanced VLSI Design]
- **VHDL Implementation of an 8-Bit Microprocessor** [Course Project - VHDL]
- **TMS320C6713 MP Based Image Processing System** [Course Project - Advanced Micro-controllers]

PUBLICATIONS

Selected Publications out of 4 Journal and 12 Conference Proceedings

- V. Honkote and B. Taskin, "ZeROA: Zero Clock Skew Rotary Oscillatory Array", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* (in review).
- V. Honkote and B. Taskin, "CROA: Design and Analysis of the Custom Rotary Oscillatory Array", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* (in pre-print).
- V. Honkote, A. More, Y. Teng, J. Lu and B. Taskin, "Interconnect Modeling, Synchronization and Power Analysis for Custom Rotary Rings", in *IEEE International Conference on VLSI Design (VLSID)*, Jan. 2011 (accepted).
- V. Honkote and B. Taskin, "Skew-Aware Capacitive Load Balancing for Low-Power Zero Clock Skew Rotary Oscillatory Array", in *IEEE International Conference on Computer Design (ICCD)*, Oct. 2010.
- V. Honkote and B. Taskin, "PEEC Based Parasitic Modeling for Power Analysis on Custom Rotary Rings", in *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, Aug. 2010, pp. 111–116.
- V. Honkote and B. Taskin, "Design Automation and Analysis of Resonant Rotary Clocking Technology", in *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Jul. 2010, pp. 471–472.
- V. Honkote and B. Taskin, "Skew Analysis and Bounded Skew Constraint Methodology for Rotary Clocking Technology", in *IEEE International Symposium on Quality Electronic Design (ISQED)*, Mar. 2010, pp. 413–417.
- V. Honkote and B. Taskin, "Analysis, Design and Simulation of Capacitive Load Balanced Rotary Oscillatory Array", in *IEEE International Conference on VLSI Design (VLSID)*, Jan. 2010, pp. 218–223.
- V. Honkote and B. Taskin, "Zero Clock Skew Synchronization with Rotary Clocking Technology", in *IEEE International Symposium on Quality Electronic Design (ISQED)*, Mar. 2009, pp. 588–593.
- V. Honkote and B. Taskin, "Custom Rotary Clock Router", in *IEEE International Conference on Computer Design (ICCD)*, Oct. 2008, pp. 114–119.

SKILLS

- C, C++, Perl, Unix Shell Scripting, Basic Java
- Cadence – Virtuoso Suite, Spectre
  Mentor – HDL Designer, Modelsim, Leonardo Spectrum
  Synopsys – Design Compiler, PrimeTime, HSPICE
  Xilinx – Spartan 3, Virtex 5
- VHDL, SystemC, Spice, Matlab, Simulink, Maple, Labview
- Cplex, Glpk, Lp Solve
- LaTeX, XEmacs, vi, Office Suites
- Unix, Linux, Mac OS, MS Windows, DOS

ACADEMIC HONORS AND AWARDS

- Finalist in the Best Ph.D. Dissertation Competition at the IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July 5-7, 2010.
- Recipient of "Nihat Bilgutay Fellowship" in recognition of academic merit in the Department of Electrical and Computer Engineering, Drexel University, February 17, 2010.
- Awarded one of the nine (9) Freshman Design Fellowships (2009) by the College of Engineering, covering full tuition and stipend, including career development for academic/research positions.
- Participated in ACM/SIGDA Ph.D. forum at DAC 2009.
- Participated in ACM/SIGDA CADathlon programming contest at ICCAD 2009, 2008.
- Recipient of "A. Richard Newton Graduate Scholarship" at DAC 2007, for the *Routing for Resonant Clocking Technology in Multi-GHz range* project.
- Awarded a fellowship to attend the Design Automation Summer School (DASS) held at DAC 2007.
- Awarded the Dean's Fellowship for graduate study at Drexel University (2004 – 2006).
- Secured 14th rank in 10th grade out of 600,000 students, Karnataka, India in 1997.

RELEVANT COURSEWORK

- CMOS VLSI design, computer architecture, embedded microprocessors, VHDL, CAD for VLSI design I and II, deep submicron systems, data structures and algorithms, stochastic systems, DSP.