Wireless Interconnects for Inter-tier Communication on 3D ICs

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***Abstract*— The feasibility of on-chip antennas for inter-tier communication on a 3D integrated circuit (IC) stack is shown for two different 3D integration processes. The on-chip antennas for inter-tier wireless interconnects are proposed to be used in conjunction with through silicon vias (TSVs) for global communication in 3D ICs. A 3D finite element method (FEM) based full wave electro-magnetic analysis of two different 3D IC models is presented: a fully depleted silicon on insulator (FD-SOI) oxide-oxide bonding 3D circuit integration technology and a complimentary metal oxide semiconductor (CMOS) silicon on insulator (SoI) Benzocyclobutene (BCB) polymer adhesive bonding 3D circuit integration technology. It is shown that the selected transmitting and receiving antennas provide a strong signal coupling at a radiation frequency of 10GHz for both 3D integration processes. In particular, the transmission gains between the antenna pair are -6.92 dB and -5.23 dB for communication between the first and the third IC tiers of a 3D IC for the oxide-oxide and the BCB polymer adhesive bonding techniques, respectively.**

I. Introduction

The advancements in semiconductor process technologies have enabled an increase in the speed and performance of the complimentary metal oxide semi-conductor (CMOS) planar integrated circuits (ICs) through reduction in the size of the metal oxide semi-conductor field effect transistor (MOSFET) devices. However, this reduction in the MOSFET device sizes has been accompanied by a proportional reduction in the cross-sectional area of the metal interconnects used for communication on an IC die. The increased system complexity, density and die size of a typical planar IC, coupled with the reduction in the cross-sectional area of metal interconnects, have increased the parasitic effects associated with the interconnects. The global metal interconnect lines are now considered as a bottleneck to the increase in IC speed as the delay due to the interconnects is higher than the delay due to the MOSFETs [1].

Certain conventional design approaches used by the semiconductor industry to mitigate this problem include increasing the interconnect width (i.e. reverse scaling of the interconnects) and changing the inter layer dielectrics (ILD) on the die to low κ dielectric materials [1]. However, these design approaches only increase the life time of the global interconnect system by a few technology generations [2].

In contemporary design approaches, 3D integrated circuits (3D ICs) are considered as a viable solution to alleviate the problems posed by the scaling of metal interconnects in planar integrated circuits (ICs). IC die stacking in 3D ICs reduces the length of the interconnects between two communication end-points thereby reducing the interconnect delay as illustrated in Figure 1 [3]. 3D ICs also provide opportunities for integration of planar wafers manufactured using different processes (e.g. logic elements using 90 nm technology process and memory elements using 45 nm technology process) and a true system-on-a-chip (SoC).

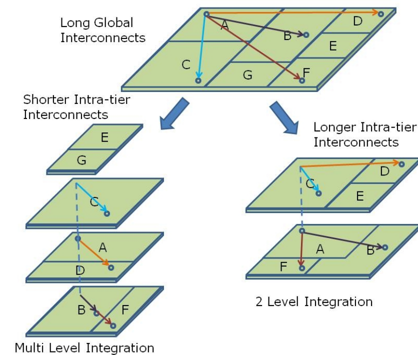

Fig. 1. Comparison of planar 2D and 3D ICs.

Various integration processes are being developed for 3D integration of planar wafers into tiers of a 3D IC [3]. The different 3D integration process sequences utilize three major technologies [3]:

1) Formation of inter-tier communication channels,
2) IC wafer thinning,
3) Wafer alignment and bonding.

The most important among these technologies is the formation of inter-tier communication channels between the IC tiers of a 3D IC. Efficient and dense through silicon vias (TSVs) are instrumental in this aspect to provide a good inter-tier communication channel as illustrated in Figure 2 [3, 4]. However, the TSVs suffer from a considerable utilization of the wiring footprint of the individual tiers of the 3D IC stack, leaving less area for intra-tier routing [3]. Further, the process of making TSVs for a multi-tier (more than 2 tiers) interconnection on a 3D stack is more difficult for some TSV technologies and entirely prohibited for certain others [3]. Moreover, if two laterally separated communication end-points on two separate tiers are to be connected, then intra-tier routing is necessary—thereby increasing the interconnect length.

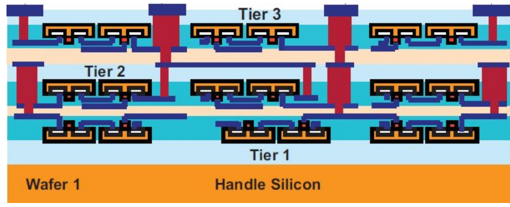

Fig. 2. MIT Lincoln Laboratory's 3D IC 3-tier integration structure [4].

This work proposes the use of on-chip meander dipole antennas for inter-tier communication on a 3D IC. The feasibility and characterization of on-chip antennas for inter-tier communication on a 3D IC are analyzed from a signal coupling point of view. Since the on-chip meander dipole antennas have a substantial footprint, they are proposed to be used in conjunction with TSVs. Three (3) significant advantages of wireless interconnects for inter-tier communication are:

1) Permitting a communication channel between non-adjacent IC tiers,
2) Providing the flexibility to place the communication channel end-points (i.e. antennas) on separate tiers without a perfect vertical alignment,
3) Providing larger lateral separation between communication end points (for an antenna pair).

The feasibility of on-chip antennas for intra-chip communication on planar ICs has been shown in [5, 6]. High-speed operation capabilities of deep sub-micron devices have enabled circuits to operate at frequencies above 10 GHz. Since the physical dimension of an antenna is inversely proportional to its operating frequency, it is possible to fabricate antennas on chip using standard CMOS foundry processes.

The on-chip antennas can be potentially used for any of the 3D wafer integration techniques. In this paper, the performance of on-chip antennas is investigated when used in 3D ICs built with:

1) Oxide-oxide IC tier bonding, embodied in fully depleted silicon on insulator (FDSOI) [4],
2) Polymer adhesive IC tier bonding, embodied in silicon on insulator (SoI) [7].

The performance of on-chip antennas for the different metal bonding styles will have to be further investigated as the presence of metal structures can affect the performance of the antennas [8]. In addition, a number of other items must be researched, such as power dissipation, temperature profiles and the performance of on-chip antennas compared to TSVs. The focus of this paper is a full wave electromagnetic analysis of the signal coupling for inter-tier communication between on-chip antennas placed on different IC tiers of a 3D IC stack.

II. Wireless Interconnect Analysis

The on-chip antennas are simulated for inter-tier communication on a two tier and a three tier 3D IC stack. The oxide-oxide IC tier bonding 3D IC die is modeled according to MIT-Lincoln Laboratory's fully depleted silicon on insulator (FD-SOI) 3D circuit integration technology design parameters [4].

TABLE I
Material characteristics of different regions on a die [4, 10].

Material	Conductivity (S/m)	Relative Permittivity
Silicon Dioxide	0.00	3.70
2000 Ω-cm Silicon Substrate	0.05	11.90
P-type Epitaxial Silicon	3636.36	11.90
N-type Epitaxial Silicon	1818.18	11.90
Benzocyclobutene (BCB)	0.00	2.65

The polymer adhesive IC tier bonding style is modeled according to the Rensselaer 3D integration process [3]. The adhesive IC tier bonding style uses Benzocyclobutene (BCB) (Cyclotene 3022-35) polymer as the bonding agent between the different IC tiers [7]. Both these selected processes utilize the CMOS silicon on insulator (SoI) technology. The SoI processes are selected as it is known that the transmission gain of the antennas is the highest for high resistivity silicon substrate [5, 6].

The presence of a high-conductivity epitaxial layer shifts the operating frequency to a lower range. Hence, in order to develop an accurate simulation model, the conductivity parameters for the different materials on the die are used. These parameters are listed in Table I. The conductivity values are calculated from the parameters provided in [4] and doped semiconductor material resistivity data provided in [9].

The simulations are performed in Ansoft HFSS (High Frequency Structure Simulator), a 3D finite element method (FEM) based full-wave electro-magnetic simulator [11]. Meander dipole antennas are used in the simulation model as these antennas are more compatible with conventional CMOS technologies in having 90° bend angles. The antennas are designed to operate at 17 GHz with a total arm length (including the length of the meander segments) of 2.4 mm according to the parameters presented in [12]. The parameters presented in [12] do not include a high conductivity epitaxial layer under the antennas. However, the presence of a high conductivity epitaxial can reduce the radiation frequency. The die size is 6×4 mm^2 as shown in Figure 3. Two sets of simulations are performed for each of the two (2) bonding styles:

1) Transmitting and receiving antennas vertically aligned and on different IC tiers,
2) Transmitting and receiving antennas non-vertically aligned and on different IC tiers,

In the vertically aligned case the transmitting antenna is placed on IC tier 1 and the receiving antenna is placed vertically above on IC tier 3. For the second simulation set, the transmitting antenna is placed on IC tier 1 and the receiving antenna is placed on IC tier 2 with a varying level of lateral separation from the transmitting antenna. In addition to these simulations, for the oxide-oxide bonding technique a simulation is performed where in the transmitting antenna is placed on IC tier 2, with the receiving antennas placed simultaneously on IC tier 1 and IC tier 3. The frequency range of the simulation is from 5 GHz to 20 GHz.

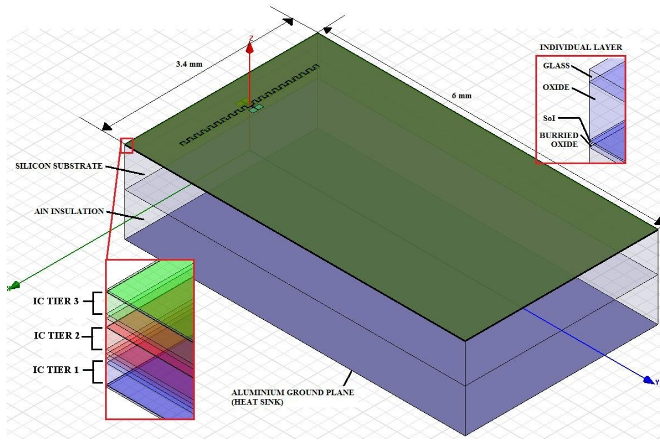

Fig. 3. Simulated structure for an inter-tier wireless interconnect system in 3D ICs.

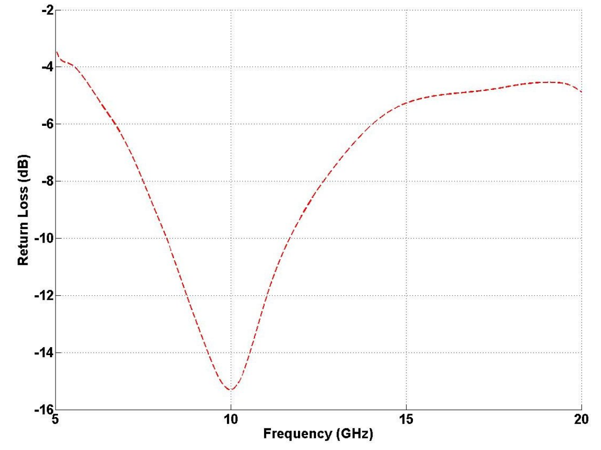

Fig. 4. Return loss S_{11} at the transmitting antenna.

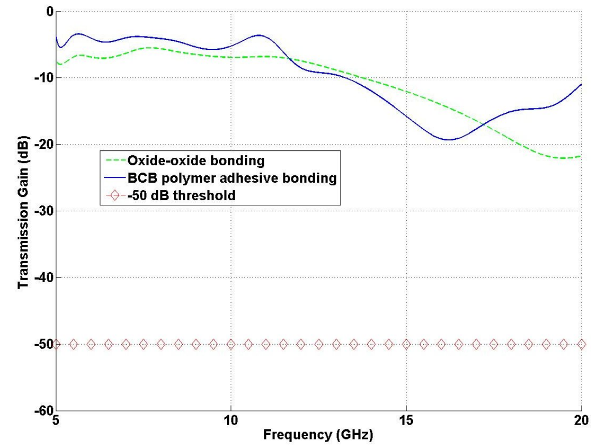

Fig. 5. Transmission gain G_a between transmitting and receiving antenna on different IC tiers (vertically aligned) for the two IC tier bonding techniques.

III. Results and Discussions

In experimentation, the scattering parameter (s-parameter) matrix $\overline{S}$ between the transmitting and receiving antennas is collected. The scattering parameter (s-parameter) matrix of a network characterizes the coupling between the ports of a network [13]. Hence, the s-parameter matrix is used to characterize the operation and efficiency of the inter-tier wireless communication system.

The radiation frequency of the antenna (based on the frequency at which the return loss is the highest) is expected to be at 17 GHz according to the parameters presented in [12]. However, as discussed in Section II, the presence of a thin high-conductivity epitaxial layer under the antenna structure shifts the radiation frequency. The higher the conductivity of the epitaxial layer, the larger is the reduction in the radiation frequency. Hence, as shown in Figure 4, the radiation frequency of the transmitting antenna in this environment is 10 GHz because the s-parameter S_{11} is the least at this frequency. This shift in the radiation frequency of the transmitting antenna should be accounted for in designing on-chip antennas and should be done so before designing the required circuitry. Since the length of the meander antennas is inversely proportional to the frequency of operation, the dimensions of both the transmitting and the receiving antenna can be reduced to increase the operating frequency to the desired range, providing a more compact antenna design.

The figure of merit used for the antenna pair is the transmission gain between the transmitting and receiving antenna. The transmission gain, G_a of the antenna pair is computed using the following formula:

$$G_a = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)} \tag{1}$$

where S_{21} is the forward transmission, S_{11} is the reflection of the electric field at the transmitting antenna and S_{22} is the reflection of the electric field at the receiving antenna. All three parameters S_{11}, S_{21}, and S_{22} are obtained from the s-parameter matrix $\overline{S}$.

The computed transmission gains G_a—based on the simulation results between the transmitting and receiving antennas with vertical alignment—for both the IC tier wafer bonding techniques is shown in Figure 5. The high value of the transmission gain indicates a good signal coupling. For an effective communication, it is required that the gain of the antenna is higher than the gain that can be provided using a low noise amplifier (LNA) at the receiving end. CMOS integrated LNAs are capable of providing gains as high as 50 dB [14]. The transmission gain G_a for the receiving antenna placed on IC tier 3 of the 3D IC stack for the oxide-oxide bonding technique and the BCB polymer adhesive bonding technique is found to be -6.921 dB and -5.227 dB, respectively, at the radiating frequency of 10 GHz. Hence, a strong signal coupling between the IC tiers of a 3D IC using either of the two IC tier bonding techniques is feasible using on-chip antennas.

The computed transmission gain G_a for the simulation case with 3 mm lateral separation between the transmitting antenna and the receiving antenna for both the IC tier wafer bonding techniques is shown in Figure 6. This experiment is performed to demonstrate the advantage of wireless interconnects on 3D ICs in providing the flexibility to place the communication

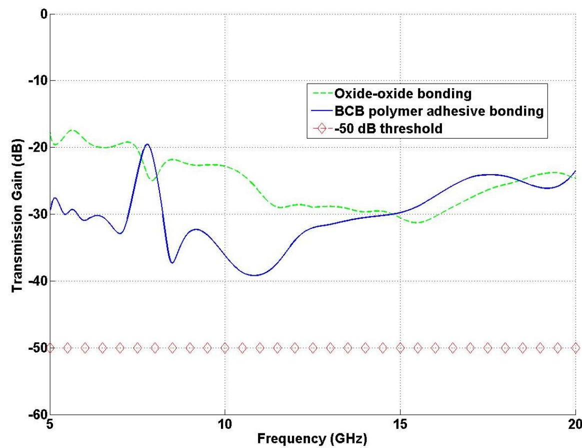

Fig. 6. Transmission gain G_a between transmitting and receiving antenna on different IC tiers with 3 mm lateral separation between the antennas for the two IC tier bonding techniques.

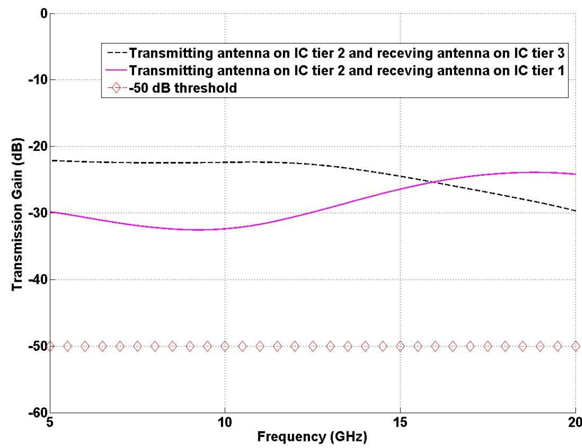

Fig. 7. Transmission gain G_a between transmitting and receiving antennas placed on two diagonally opposite corners of an oxide-oxide bonding technique 3D IC stack.

channel end points on separate tiers without a perfect vertical alignment (unlike TSVs). The results shown in Figure 6 also indicate that at the desired frequency the transmission gain is higher than -50 dB (the threshold for successful communication based on achievable LNA gain). Therefore, it is possible to have a lateral separation as high as 3 mm which is not feasible for TSVs even with additional inter-tier routing. However, an increase in the lateral separation between the antenna pair is expected to decrease the transmission gain, while the transmission gain would be higher for a smaller lateral separation.

The transmission gains between the receiving and transmitting antennas for the simulation case with two receiving antennas and a single transmitting antenna placed on different IC tiers are shown in Figure 7. The receiving antennas are placed on diagonally opposite corners of the 3D IC stack each with a 2.5 mm lateral separation from the transmitting antenna. This experiment demonstrates the feasibility of distributing a signal to two diagonally opposite communication end-points on a 3D IC using wireless interconnects. To perform a similar multi-end point communication using TSVs would necessitate long lengths of intra-tier metal interconnects on both sides of the communication point. The parasitics of both branches will add up thereby increasing the delay to both the communication end-points.

IV. Conclusion

In this work, the feasibility of using on-chip antennas for wireless communication between the IC tiers of a 3D integrated circuit is shown. It is shown that it is possible to have a strong signal coupling for antennas placed vertically above each other on different IC tiers of the die. It is also shown that it is possible to communicate wirelessly between two IC tiers where the communication points are separated from each other laterally up to 3 mm. The feasibility of multi-point communication on a 3D IC stack using wireless interconnects is shown. However, the performance and efficiency of the wireless interconnects is still to be investigated. The presence of metal structures has adverse affects on the transmission gain of the antennas and their performance under such conditions also needs to be evaluated. Since the antennas and the associated circuitry are expected to occupy a considerable amount of space, they are intended to be used in conjunction with TSVs, especially for multi-tier (more than two IC tiers) global communication.

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