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Leo Filippini

Summary I am a PhD candidate focusing on charge recovery logic and low-power VLSI systems, with a strong background in analog IC design and layout in deep-submicron CMOS. I have cleanroom and tapeout experience and a sound understanding of transistor level design and device physics.

Education

Present **PhD candidate**, *Drexel University*, Philadelphia (PA).
Electronics Engineering

2013 **Master Degree**, *University of Brescia*, Brescia (Italy), *summa cum laude*.
Electronics Engineering

2010 **Bachelor Degree**, *University of Brescia*, Brescia (Italy).
Information Engineering

Experience

Present **Research Assistant**, *Drexel University*, Philadelphia, PA (USA).
My research is focused on low-power methodologies for VLSI circuits. I am currently investigating novel implementations of charge-recovery logic, power-clock generation, and modeling of such systems.

2013 **Intern**, *Imec*, Heverlee (Belgium).
For my Master's thesis I spent six months designing an integrated transimpedance amplifier for capacitive micromachined ultrasonic transducers (CMUT). Detailed achievements:
- Implementation of the transducer model, with extensive noise analysis
- Design of a topology new to the application
- Tape-out in CMOS 180nm

2010 **Intern**, *University of Brescia – Physics Department*, Brescia (Italy).
For four months I worked on my Bachelor's thesis: *Synthesis and Integration of Quantum Dot Semiconductors in Third Generation Excitonic Solar Cells.* Along with my supervisors, we chemically synthesized different types of quantum-dots and built many solar cells. I, in particular, took care of the substrate deposition and characterization, the construction of the cells and their optical and electrical characterization.

Languages

Italian Native

English Proficient — TOEFL iBT: 107/120

Publications & Awards

2016 Leo Filippini and Baris Taskin, *"Charge Recovery Logic for Thermal Harvesting Applications"*, ISCAS, May 2016

2015 Leo Filippini, Emre Salman, and Baris Taskin, *"A Wirelessly Powered System with Charge Recovery Logic"*, ICCD, October 2015

2014 Can Sitik, Sungjun Yoon, Leo Filippini, Emre Salman, and Baris Taskin, *"FinFET-Based Low Swing Clocking"*, JETC, August 2015

2014 Can Sitik, Leo Filippini, Emre Salman, and Baris Taskin, *"High Performance Low Swing Clock Tree Synthesis with Custom D Flip-Flop Design"*, ISVLSI, July 2014

2011 Winner of European *Lifelong Learning Program* (LLP) scholarship