Ragh Kuttappa

Department of Electrical and Computer Engineering
Drexel University, Bossone 405, 3141 Chestnut Street
Philadelphia, PA 19104-2875

Phone: (415)-439-9584
E-mail: ragh@drexel.edu
url: `vlsi.ece.drexel.edu`

Education

Ph.D., Electrical Engineering, GPA: 3.95 (expected graduation 2019)
Drexel University, Philadelphia, PA.

M.S., Electrical and Computer Engineering, GPA: 3.8 August 2015
San Francisco State University, San Francisco, CA.

B.E., Electronics and Communication, GPA:3.5 July 2012
Visvesvaraya Technological University, Karnataka, India.

Professional Experience

Ph.D. Candidate, September 2015 - present
VLSI and Architecture Laboratory, Drexel University
Advisor: Dr. Baris Taskin

- Design of transistor level and gate level low power circuits using cadence suite.
- Implementation of Verilog-A models for emerging optoelectronic components for CMOS integration.
- Development of backend automation flow using Cadence EDI,
  -Custom design for resonant rotary clocks.
- Custom methodology for frequency division of resonant clocks, ranging for MHz to GHz.
- Physical digital design and optimization of resonant and PLL-based designs.
  -Floorplan, Placement, Clock tree Synthesis and Routing of resonant-based circuits.

Ph.D. Intern, Samsung Austin Research Center (SARC) April 2017 - Sept. 2017
CAD Internship

- Standard cell characterization and timing correlation.
- Signoff for latest CPU, RTL to GDS.
- Metal stack evaluation for lower process nodes.

Masters Student, August 2013 - August 2015
Nano-electronics and Computing Research Laboratory, San Francisco State University
Advisor: Dr. Hamid Mahmoodi

- Reliability Analysis of Spin Transfer Torque (STT) based circuits.
- Low power design methodologies for reconfigurable logic using Look Up Tables (LUT).
- Developed circuit architectures for reconfigurable STT based LUTs.
- Thesis: Circuit Reliability Analysis under Variations in Nano-Scale CMOS.

Publications

- Ragh Kuttappa and Baris Taskin, "Low Frequency Rotary Traveling Wave Oscillators", in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018.
- Ragh Kuttappa, Baris Taskin, Lunal Khuon and Bahram Nabet, "Optoelectronic Capacitor Threshold Logic Gates", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)* - in review.

- Ragh Kuttappa, Leo Filippini, Scott Lerner and Baris Taskin, " Stability of Rotary Traveling Wave Oscillators under Process Variations and NBTI", in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2017.
- Ragh Kuttappa, Lunal Khuon, Bahram Nabet and Baris Taskin, "Reconfigurable Threshold Logic Gates using Optoelectronic Capacitors", in *Proceedings of the Design, Automation and Test in Europe (DATE),* March 2017.
- Ragh Kuttappa, Houman Homayoun, Hassan Salmani and Hamid Mahmoodi, "Comparative Analysis of Robustness of Spin Transfer Torque based Look Up Tables under Process Variations", in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016.
- Ragh Kuttappa, Houman Homayoun, Hassan Salmani and Hamid Mahmoodi, "Reliability Analysis of Spin Transfer Torque based Look up Tables under Process Variations and NBTI Aging", *Elsevier Microelectronics Reliability Journal*, March 2016.

Graduate Level Coursework

CMOS VLSI Design, Custom VLSI Design I/II, Advanced VLSI Design, Advanced Digital Design, Nano-Scale Circuits and Systems, Advanced Microprocessor Architecture, Parallel Computer Architecture.

Graduate Level Projects

Custom VLSI Design I: Design of 64x32 bit SRAM

- Design of full custom 64x32 bit SRAM schematic, layout, DRC, LVS and StarRc.
- Optimizing the design for speed, area, stability, dynamic and static power consumption.
- Optimized the circuit by smart controller logic design resulting in 1.8GHz clock frequency and 23% area reduction.

Custom VLSI Design II: On-chip two level power distribution network in IBM 180 nm technology

- Design of power distribution network while analyzing noise sources and techniques for noise reduction.
- Implementation of a two-level interdigitated grid topology and analysis of Power Distribution Noise with Switched Decoupling Capacitors.
- Power gating implemented and effect on noise in different local grids are studied.

IC Design using Synopsys Tools

- Defined core, placement row structure and inserted filler pad cells and macros and analyzed congestion, timing, power and IR drop using Power Network Analysis.
- Generated and analyzed clock tree skew and timing reports to determine CTS QoR using Synopsys and optimized the design for better area and performed routing the clock nets.
- Analyzed the design for timing, logical and physical DRC and LVS violations and reduced critical areas by wire spreading.
- Designed an IC and performed floor planning, placement, CTS, routing and chip finishing and streamed out GDSII data.

Static Timing Analysis of ORCA using Synopsys Prime Time

- Analyzed a timing report from input and output ports for setup and hold and generated summary reports for the violations in ORCA.

- Created a setup file for PrimeTime that includes aliases and useful TCL procedures.
- Debugged hold violation using SPEF parasitics.

Digital Design: Design of full search motion estimator used in Low power H.264 Video Compression Architectures

- The aim of this project is to find motion vectors between two successive motion frames by motion estimation.
- Bottom-up design approach is followed and each module is tested before top level integration with memory modules resulting in stable efficient design.
- Verilog RTL design, simulation, synthesis and timing analysis.

Skills

- Synopsys - Custom Designer, Design Compiler, IC Compiler I/II, PrimeTime
  Cadence - Virtuoso Suite, Encounter, RTL Compiler
- C, C++, Perl, TCL, SKILL, Verilog, VHDL, LaTeX

Teaching Assistant Coursework

- Computational Lab I/II, F'15 - W'16, F'17 - W'18 Freshman Level Class
- Analog Electronics Lab, F'15, Junior Level Class
- Micro-controller Design, W'16 - S'16, Winter 2018 Junior Level Class
- Digital Logic Design, S'16, F'16, Sophomore Level Class
- Digital Design Projects, S'16, Junior Level Class
- ASIC Design I/II, F'16 - W'17, Graduate Level Class
- Custom VLSI Design I, W'18, Graduate Level Class

References

- **Dr. Baris Taskin**
  Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
- **Dr. Ioannis Savidis**
  Assistant Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
- **Dr. Hamid Mahmoodi**
  Professor, Department of Computer Engineering
  San Francisco State University, Philadelphia, PA