The Adiabatically Driven StrongARM Comparator

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***Abstract*—Adiabatic logic, also known as charge recovery logic, is subject to active research in the field of low-energy computation. Although the principles of adiabatic operation are well understood in digital circuits, analog and mixed-signal circuit implementations are largely unexplored. This work shows that the strongARM comparator can take advantage of adiabatic principles by i) being powered by a sine-wave, the power-clock, rather than the conventional DC power supply, V_{DD}, and ii) using an adiabatic buffer as the output stage, rather than an SR-latch. Post-layout simulations in a 65nm technology show that the adiabatically driven strongARM has similar characteristics to the traditional strongARM: +2% noise, +0.1% input offset voltage, and the same regeneration time-constant, while only consuming between 28% and 55% of the energy of the traditional strongARM, in the typical case.**

***Index Terms*—Comparator, ADC, charge recovery comparator, adiabatic comparator, adiabatic logic, charge recovery logic, charge recovery circuits.**

I. Introduction

In modern integrated circuits, digital data is represented as a set of node voltages that change state thanks to the movement of electric charge. A logic gate is responsible to charge, or discharge, a given node (output), depending on the charge distribution of a set of other nodes (inputs). The energy dissipated on the transistors, acting as switches, is converted to heat through Joule effect. Adiabatic logic achieves energy reduction with respect to static CMOS by i) gradually charging output nodes and ii) recycling the charge that is used to store information on node capacitances. In order to do so, time varying signals, called power-clock (PC), usually sine-waves, are both responsible for supplying energy and timing to each logic gate. Depending on the logic family, there can be two, four, or more power-clock signals that need to be synchronized between each other, hence the common definition of two- or four-phase logic family.

Recently, adiabatic principles were used for the first time to design mixed-signal circuits, in the form of two different topologies of comparators [1], [2]. The development of an adiabatic comparator, a fundamental building block of many analog-to-digital converters (ADC), enables the design of fully adiabatic ADC, which in turn makes it possible to design a fully adiabatic System-on-Chip. In this work, the principles of adiabatic logic are used to decrease the energy consumption of the strongARM comparator [3], by way of using a power-clock signal instead of the traditional V_{DD} power supply. The engineering research of generating and synchronizing the power-clock signals, such as in [4], is known for all adiabatic circuits in literature, and not exclusive to the proposed adiabatically driven comparator in this brief. From a performance analysis point of view, an adiabatic system will have the power-clock signals routed globally on chip, and the effects of routing the power-clock are excluded from the performance analysis of individual components in literature. The performance of a system-level implementation will ultimately depend on the combined energy and energy efficiency of the adiabatically driven (mixed-signal and/or digital) circuit components, as well as those of the global power and clock distribution networks. The results presented in this brief are very encouraging, and purposefully defer power-clock considerations to system-level analyses and implementations. As a reference point, the energy efficiencies of power-clock generation and distribution are reported up to $90\,\%$ in experimental results [5].

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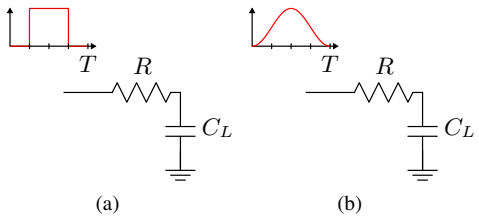


Fig. 1. Charging a capacitance (a) abruptly, and (b) adiabatically.

II. Adiabatic Principles

Figure 1 shows two different ways of charging and discharging a capacitance C_L through a resistance R: abruptly (with a square-wave) or adiabatically (with a sine-wave). In the first case, Figure 1(a), the energy E_C dissipated is:

$$E_C = C_L V_{DD}^2 \tag{1}$$

where V_{DD} is the magnitude of the square-wave. On the other hand, the energy E_A dissipated in Figure 1(b) is:

$$E_A = \frac{\pi^2}{2} \frac{C_L^2 V_{DD}^2 R}{T} \tag{2}$$

where V_{DD} and T are the peak-to-peak voltage and the period of the sine-wave, respectively. For $T \rightarrow \infty$, the energy dissipated on the resistance R becomes zero: that is the reason why the term *adiabatic* is used for this energy profile. Equation (1) describes the dynamic energy consumption of static CMOS, domino logic, and other traditional logic families, while Equation (2) is the dynamic energy consumption of charge recovery logic, also known as adiabatic logic [6]. In order for the adiabatic charge method to consume less energy than the abrupt charge method, the ratio E_A/E_C must be < 1:

$$\frac{E_A}{E_C} = \frac{\pi^2}{2} \frac{C_L R}{T} < 1. \tag{3}$$

Inequality (3) shows how, given the technology and design dependent values C_L and R, the appropriate period can be chosen. One of the primary challenges of adiabatic logic implementations has been the scaling of frequency subject to this equation, while preserving the low-energy characteristics over traditional CMOS implementations [6].

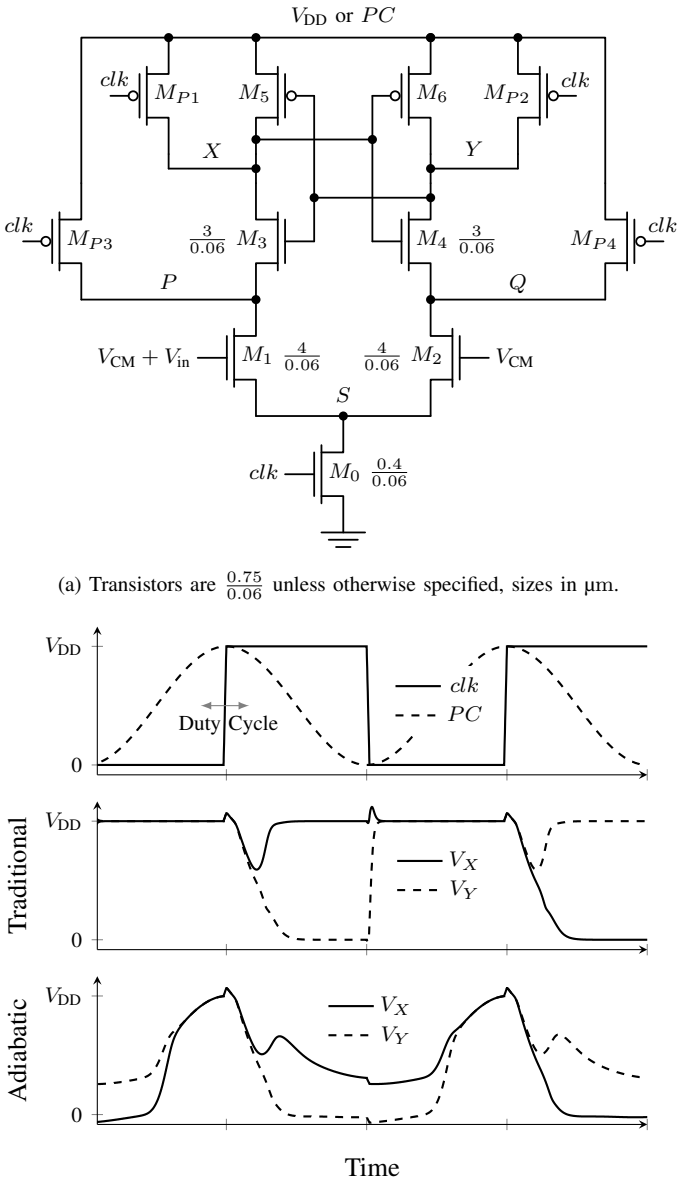
III. THE TRADITIONAL STRONGARM (SA)

The operation of the traditional strongARM (SA) shown in Figure 2, can be divided in two phases: precharge and evaluation. During precharge, the clk signal is low, and transistors M_{P1}, M_{P2}, M_{P3}, and M_{P4} charge nodes X, Y, P, and Q to V_{DD}. Transistor M_0 is off, so the only path to ground is open. During the evaluation phase, when clk goes high, transistors M_{P1}, M_{P2}, M_{P3}, and M_{P4} turn off, and transistor M_0 starts to conduct. Transistors M_3, M_4, M_5, and M_6 are initially off, because their drain to source voltages are zero. Transistors M_1 and M_2 are conducting, discharging nodes P and Q at different rates, depending on V_{in}. Once P and Q are at $V_{\text{DD}}-V_{TN}$, where V_{TN} is the threshold voltage of the NMOS, M_3 and M_4 start conducting as well, introducing feedback and increasing the gain of comparator. The charge on nodes X and Y can now flow towards ground, and when the voltages of X and Y are at $V_{\text{DD}}-V_{TP}$, where V_{TP} is the threshold voltage of the PMOS, transistors M_5 and M_6 start conducting as well. The two back-to-back inverters realized by transistors M_3, M_4, M_5, and M_6 settle on one of the two stable states: $V_X = V_{\text{DD}}$ and $V_Y = 0$, or vice versa.

From Equation (1), assuming that the comparator is symmetrical and ignoring the charge deposited on node S, the dynamic energy dissipated by the strongARM comparator, E_{SA}, during every cycle is:

$$E_{\text{SA}} = (C_{X,Y} + 2C_{P,Q})V_{\text{DD}}^2 \tag{4}$$

where $C_{X,Y}$ is the capacitance on nodes X and Y, and $C_{P,Q}$ is the capacitances on nodes P and Q. Unlike $C_{P,Q}$, capacitance $C_{X,Y}$ is not multiplied by 2 because during the evaluation phase, only X or Y is discharged to ground.



(a) Transistors are $\frac{0.75}{0.06}$ unless otherwise specified, sizes in µm.

(b) StrongARM behavior when traditionally driven and adiabatically driven

Fig. 2. The strongARM comparator: (a) schematic and (b) its operation.

IV. THE ADIABATICALLY DRIVEN STRONGARM (ADSA)

The key idea of the proposed methodology is to use an adiabatic precharge in order to decrease the energy consumption of the strongARM comparator. In order to do so, a sinusoidal signal PC is introduced and replaces V_{DD}, as shown in Figure 2. The operation of the ADSA can again be divided in two phases: precharge and evaluation. In the precharge phase, the clk signal is low, and transistors M_{P1}, M_{P2}, M_{P3}, and M_{P4} are conducting. Thanks to the slope of the rising edge of PC, nodes X, Y, P, and Q are adiabatically charged to V_{DD}. Transistor M_0 is off, so there is no path to ground. The evaluation phase begins when clk goes high, similar to the SA. Signal clk is synchronized such that as soon as PC reaches V_{DD}, clk goes high: transistors M_{P1}, M_{P2}, M_{P3}, and M_{P4} turn off, and transistor M_0 starts to conduct. Transistors M_1 and M_2 discharge nodes P and Q at different rates. Once P and Q are at $V_{\text{DD}}-V_{TN}$, M_3 and M_4 start conducting, and the charge on nodes X and Y discharges to ground. When the voltages of nodes X and Y are at $V_{\text{DD}}-V_{TP}$, transistors M_5 and M_6 start conducting as well. The two inverters realized by transistors M_3, M_4, M_5, and M_6 settle on one of the two stable states: $V_X = PC$ and $V_Y = 0$, or vice versa. The outputs of the ADSA, when operating at frequencies close to its maximum, are not rail-to-rail, but look like the signals of Figure 2(b). Because of that, the outputs of the ADSA are not suitable to drive adiabatic logic directly. In order to address this issue, a buffer must be used, not dissimilarly from the SR-latch needed for the traditional strongARM [3].

The energy savings with respect to the SA comparator are primarily due to the precharge. In Figure 2(b), both X and Y are initially at zero, and thanks to M_{P1} and M_{P2}, both follow PC, hence charging adiabatically. When PC is at its highest magnitude, namely V_{DD}, clk goes high and starts the evaluation phase. At this point, the adiabatically driven strongARM behaves just like the traditional strongARM: node X is driven

high while node Y is driven low. It is important to note that nodes Y, P, and Q are discharged to ground, abruptly, through transistors M_{3-4}, M_{1-2}, and M_0, while node X is discharged adiabatically through M_5, until $V_X \approx V_{\text{TP}}$.

Since the ADSA has an adiabatic precharge and also an abrupt discharge component, the dynamic energy consumption is a mix of the two energy profiles of Equations (1) and (2). The adiabatic component $E_{\text{ADSA,A}}$ is due to all the nodes being adiabatically charged to V_{DD} during the precharge phase, and that one output node is adiabatically discharged after the evaluation phase. Hence, following Equation (2):

$$E_{\text{ADSA,A}} = \frac{\pi^2}{4}(3C_{X,Y} + 2C_{P,Q})^2 V_{\text{DD}}^2 R_{\text{on}}/T \qquad (5)$$

where R_{on} is the equivalent resistance of transistors M_{P1}, M_{P2}, M_{P3}, M_{P4}, M_5, and M_6. T is the period of signals PC and clk. The non-adiabatic dynamic energy consumption $E_{\text{ADSA,NA}}$, following Equation (1), is:

$$E_{\text{ADSA,NA}} = \frac{1}{2}(C_{X,Y} + 2C_{P,Q})V_{\text{DD}}^2. \qquad (6)$$

For the sake of simplicity, it is assumed that $C_{X,Y} = 2C_{P,Q} = C_L$, so that the ratio of the total dynamic energy consumption of the adiabatically driven strongARM, E_{ADSA}, and the traditional strongARM, E_{SA}, is:

$$\frac{E_{\text{ADSA}}}{E_{\text{SA}}} = \frac{E_{\text{ADSA,NA}} + E_{\text{ADSA,A}}}{E_{\text{SA}}} = 0.5 + 2\pi^2 \frac{C_L R_{\text{on}}}{T}. \qquad (7)$$

The result of Equation (7) is a lower bound for the normalized dynamic energy consumption. In the best-case scenario, i.e. $2\pi^2 C_L R_{\text{on}}/T \ll 0.5$, the ADSA consumes only $50\,\%$ of the traditional strongARM. In practice, there are two other effects that further decrease the total energy consumption of the adiabatically driven strongARM with respect to the traditional strongARM: i) the leakage, short-circuit, and kickback currents are modulated by PC, and ii) at high frequencies, the outputs of the ADSA are not rail-to-rail. The first effect comes from the fact that the adiabatically driven strongARM is powered by a sinusoidal signal with a DC component of $V_{\text{DD}}/2$, hence it is expected that the impact of leakage currents be smaller, since the average voltage that causes them is $V_{\text{DD}}/2$. When clk transitions from high to low, transistors M_{P3}, M_1, and M_0 provide a path from V_{DD} to ground. When adiabatically driven, the strongARM presents the same path between PC and ground, but since PC is low at that time, it prevents short-circuit energy consumption. The second effect occurs because the output of the ADSA that is driven high is not charged to V_{DD}, but to PC. Depending on the operating frequency, by the time the evaluation phase is concluded, PC can be at a lower voltage, hence the output node is not fully driven to V_{DD}. With reference to Figure 2(b), during the first evaluation phase the voltage of node X decreases until transistors M_3–M_5 turn on, then it is driven to PC, which at that point is $\approx 2/3V_{\text{DD}}$. Though this effect lowers the energy consumption, it also signals the fact that the ADSA is operating close to its maximum frequency limit.

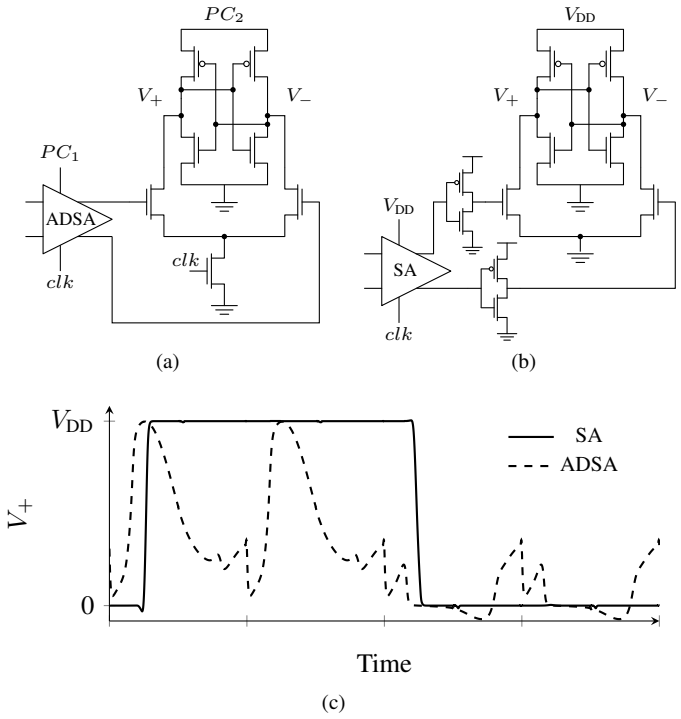


Fig. 3. Adjusting the output, (a) adiabatically driven strongARM and output buffer, (b) traditional strongARM and SR-latch, and (c) V_+ nodes.

V. DRIVING THE OUTPUT

As mentioned in Section III, the traditional strongARM comparator needs a circuit to convert its outputs to suitable signals. The outputs of the SA are rail-to-rail but cannot be used directly to drive CMOS logic because during precharge the outputs are both at V_{DD}, hence invalid. In order to convert the outputs to signals that are valid at all times, an SR-latch can be used [3]. On the other hand, the outputs of the adiabatically driven strongARM are not rail-to-rail at higher frequencies, and need to be recovered to full-swing by using an adiabatic buffer. Figure 3 shows the buffer and the SR-latch for the adiabatically driven strongARM and the traditional strongARM, respectively. For the ADSA, Figure 3(a), the outputs of the comparator are connected to a circuit based on the PAL2N buffer [7], with the addition of a footer NMOS transistor connected to the clk signal, in order to reduce short circuit currents. The buffer of the ADSA is connected to another phase of the power-clock, PC_2, as typically available in adiabatic logic [6]. By recovering the ADSA output voltage to full-swing, the adiabatic buffer extends the operating frequency of the ADSA, in contrast to the SR-latch for the SA, which only ensures that the outputs are logically valid. Figure 3(c) shows the outputs of the buffered ADSA and of the latched traditional strongARM. The former signal is suitable to drive an adiabatic logic gate, while the latter is suitable to drive a static CMOS logic gate. The energy consumption and other characteristics of the output buffer and SR-latch are not reported as they are negligible compared to those of the strongARM comparator.

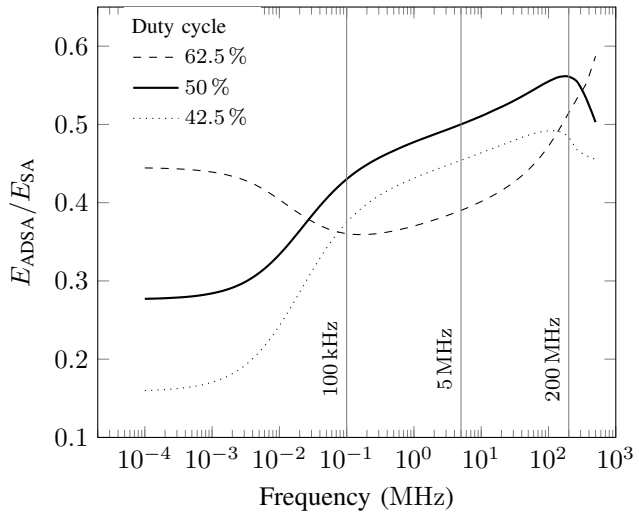


Fig. 4. Energy per conversion of the adiabatically driven strongARM (ADSA) normalized over the traditional strongARM (SA) comparator.

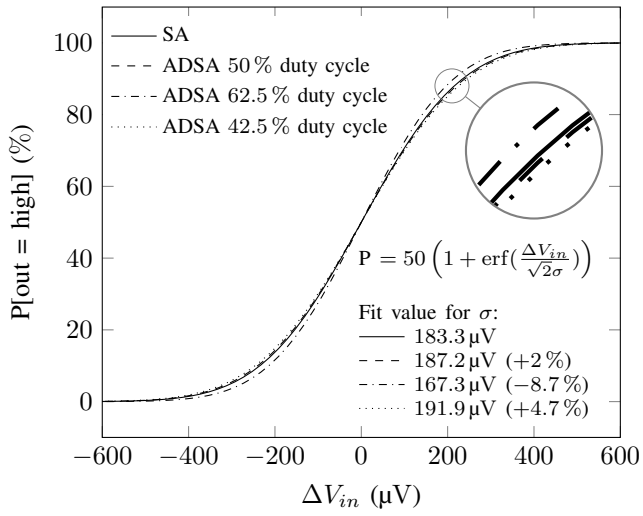


Fig. 5. Cumulative noise distribution at 500 MHz and with $V_{\mathrm{CM}} = 0.6\,\mathrm{V}$.

VI. EXPERIMENTAL RESULTS

The strongARM comparator of Figure 2 is implemented in a 65 nm technology with a nominal voltage of $V_{\mathrm{DD}} = 1.2\,\mathrm{V}$. The layout, with transistors M_1 and M_2 interdigitated and inside a guard-ring, has an area of $36\,\mu\mathrm{m}^2$. The following data is obtained with extracted circuits, unless otherwise specified. Prior to demonstrating performance, experiments are performed in order to identify the limits on operating conditions of the ADSA. Simulations on the circuit of Figure 2 show that the region of functionality of the ADSA across PV corners, at the maximum operating frequency of 500 MHz, and at the worst-case temperature of $-25\,^{\circ}\mathrm{C}$, is with a duty cycle of clk between 42.5 % and 62.5 % (a total variation of ±10 %). In other words, for the adiabatically driven strongARM to function properly, the rising edge of the clk signal has to arrive between $-0.125 \cdot T$ and $0.075 \cdot T$ of the peak of the power-clock PC, Figure 2(b).

Figure 4 shows the normalized energy consumption of the adiabatically driven strongARM (ADSA), per conversion, for different clk frequencies and for different values of duty cycle. For all frequencies, independently of the duty cycle, the ADSA consumes only up to 60 % of the energy consumed by the traditional strongARM. To understand the behavior of the ADSA, the nominal case (50 % duty cycle) of Figure 4 is analyzed in depth. For low frequencies, namely $< 100\,\mathrm{kHz}$, the normalized energy consumption converges to ≈ 0.28. The energy consumption at such low frequencies is dominated by leakage currents. As such, it is postulated that the ADSA has only 28 % of the leakage energy consumption with respect to the SA, thanks to the modulation effect of PC mentioned earlier. In the range between 100 kHz and 5 MHz, the leakage is not the primary component of the total energy consumption and the normalized energy consumption rises with the frequency. Although this behavior is to be expected, the normalized energy consumption is less than the 0.5 minimum dictated by Equation (7). This fact signifies that in the 100 kHz to 5 MHz range, the energy consumption is not dominated by the dynamic energy component analyzed in Section IV, but rather by energy consumption arising from kickback currents. Kickbacks currents are one of the main drawbacks of the strongARM topology and arise from the parasitic capacitors that couple the input nodes and nodes P, Q, and S [3]. For frequencies between 5 MHz and 200 MHz, the dynamic energy consumption becomes the dominant component, and the total energy consumption follows Equation (7). Over 200 MHz, the energy of the ADSA decreases, due to the fact that the outputs are not rail-to-rail at such high frequencies. Shortly after that, both the SA and the ADSA reach their limit frequency of 500 MHz. Interestingly, for larger values of duty cycle (e.g. 62.5 %) the ADSA consumes about 45 % of the energy of the SA at low-frequencies, because the clk signal, rising earlier than it is supposed to, increases the energy lost by leakage current. In the latter case, the rising edge of the clk arrives before PC has reached its peak, hence the outputs are always rail-to-rail and the energy consumption keeps rising with frequency. On the other hand, for smaller values of duty cycle (e.g. 42.5 %), the ADSA consumes only 16 % of the energy of the SA, as the modulation effect of the leakage currents is even more pronounced.

To show the noise behavior of the ADSA, the comparator is simulated with transient noise analysis for 1000 clk cycles, for different values of V_{in}, as in [8]. The data is then used to find the parameters of the best-fit Gaussian distribution whose standard deviation is the RMS value of the input referred noise (IRN) [3]. The best-fit curves, along with the distribution model, are shown in Figure 5 for the SA and ADSA for different duty cycle values. The extrapolated standard deviations σ are within ±10 % of each other. In particular, the input referred noise (σ) of the ADSA in the case when the duty cycle is 62.5 %, is 8.7 % lower than the IRN of the SA. This can be attributed to the fact that, as the clk rising edge arrives before the power-clock PC has peaked, the noise accumulated on nodes P and Q during precharge [3] is decreased.

The method proposed in [9] is used to estimate the input offset voltage on the pre-layout netlist, through Monte Carlo

TABLE I
INPUT OFFSET VOLTAGE V_{OFF}

	SA	ADSA		
duty cycle		50 %	62.5 %	42.5 %
σ (mV)	4.63	4.64 (+0.2 %)	4.66 (+0.7 %)	4.65 (+0.4 %)

simulations. Table I shows the results of 1000 Monte Carlo simulations of the SA and ADSA, operating at their maximum frequency of 500 MHz, for different values of duty cycle. The values in Table I show that the input offset voltage of the strongARM comparator, when driven adiabatically, changes by less than 0.6 %, regardless of the duty cycle.

The delay t_d of the comparators, for different values of the input signal V_{in}, is shown in Figure 6 for the pre-layout netlist, at 10 MHz. Both the traditional strongARM (SA) and the adiabatically driven strongARM (ADSA) present the same behavior, with a regeneration time-constant $\tau = 30.4\,\text{ps}$, when the duty cycle is 50 %. For a 42.5 % duty cycle, the regeneration time-constant τ increases by 7.2 %, while for a 62.5 % duty cycle, τ increases by 34.9 %. For duty cycles between 45 % and 55 % (not shown in Figure 6 for clarity), the regeneration time-constant τ increases less than 2.3 %. The regeneration time-constant τ is extracted at 10 MHz so that the equation to predict metastability [10] can still be used:

$$\Delta V_{in,min} = V_{\text{DD}} \cdot \mathrm{e}^{-(T_{conv}-t_0)/\tau} \tag{8}$$

where $\Delta V_{in,min}$ is the minimum differential voltage at the input nodes for which the comparator evaluates to full-swing output after a T_{conv} time. For the traditional strongARM (SA), for a clock with period T and 50 % duty cycle, the conversion time is $T_{conv} = T/2$. For the adiabatically driven strongARM (ADSA), with the same clock signal, the conversion time cannot be half of the clock cycle, as the power-clock PC has fallen to zero when the evaluation phase is over. Depending on the amplification provided by the adiabatic buffer of Figure 3(a), the minimum output differential voltage ΔV_{out} value for the ADSA can be found. For example, the adiabatic buffer of Figure 3(a) is able to amplify signals of about 120 mV, or $V_{\text{DD}}/10$. Since for the ADSA $T_{conv} < T/2$, the adiabatically driven strongARM presents a higher $\Delta V_{in,min}$ than the SA. The ADSA cannot differentiate as small a voltage as the SA, which makes the ADSA suitable for low-resolution ADCs. This difference, however, is negligible unless the comparator is strongly matched and active offset cancellation techniques are used [3]. The strongARM designed in this brief has an input offset voltage of approximately 4.6 mV, limiting a prospective ADC to a resolution of 8bits over the 1.2 V supply.

Latched comparators such as the strongARM have their initial state reset at every sampling cycle. For this reason, if the reset time is long enough to fully discharge internal capacitances, hysteresis is negligible. Simulations for both the SA and ADSA did not show significant hysteresis, even at the maximum operating frequency of 500 MHz.

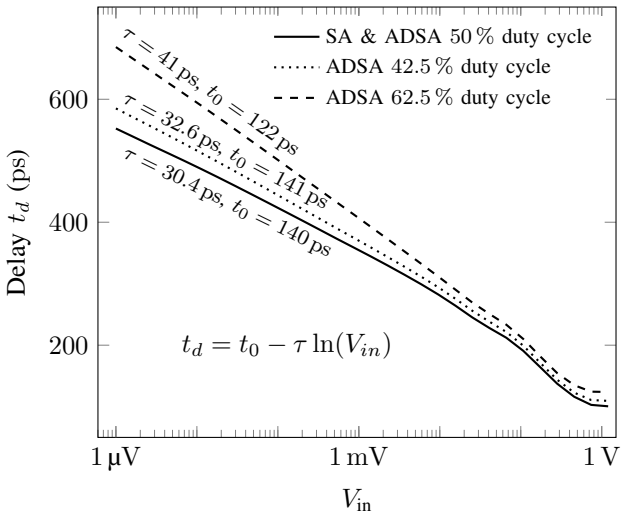


Fig. 6. Delay as function of the input signal, for $V_{\text{CM}} = 0.6\,\text{V}$ at 10 MHz.

VII. CONCLUSIONS

This brief presents an analysis of the adiabatically driven strongARM comparator (ADSA), which consumes between 28 % and 55 % of the energy of the traditional strongARM (SA), in the typical case, while presenting the same characteristics in terms of noise and input offset voltage. For a large duty cycle (62.5 %) the regeneration time-constant is the only performance metric that degrades significantly (+34.9 %), and can easily be controlled with a more precise clock: a duty cycle between 45 % and 55 % results in a maximum increment of 2.3 % of the regeneration time-constant. With efficiencies of power-clock generators of 90 % as reported in the literature, the proposed ADSA is projected to consume between 31 % and 61 % of the energy of the traditional strongARM.

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