Simulation Based Feasibility Study of Wireless RF Interconnects for 3D ICs

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***Abstract*—A feasibility study of inter-tier wireless interconnects to be used in conjunction with through silicon vias (TSVs) for global communication in 3D ICs is presented. The feasibility is shown by performing a full wave electromagnetic analysis of on-chip communicating antennas on a 3D IC, modeled according to a fully-depleted silicon on insulator (FDSOI) 3D circuit integration technology. It is shown that the selected transmitting and receiving antennas provide a strong signal coupling at the adjacent (-6.67 dB) and the non-adjacent (-6.93 dB) tiers of the 3D IC at a radiation frequency of 10GHz. In addition to permitting non-adjacent tier communication, wireless interconnects are superior to TSVs in permitting non-vertically aligned connections between IC tiers.**

I. Introduction

Scaling of semiconductor devices has increased the speed and performance of integrated circuits (ICs). However this technology scaling has also been accompanied by a proportional reduction in the cross-sectional area of the metal interconnects between the devices. The increased parasitics due to the technology scaling have caused the global interconnect lines to become a bottleneck to the increase in speed, as the delay due to these interconnects is becoming higher than the gate delay [1]. In addition, the system complexity and the die size of a typical IC have increased significantly. Hence, the global interconnect networks such as the clock distribution networks suffer from skew, jitter, power dissipation and area consumption [2]. 3D integrated circuits (3D ICs) can alleviate the problems of skew, jitter and delay caused by scaling of metal interconnects in planar ICs. 3D ICs also provide opportunities for integration of wafers manufactured using different manufacturing processes and a true system-on-a-chip (SoC) [3].

Various processes are being developed for 3D integration of planar wafers [3]. The different 3D integration process sequences utilize three major technologies [3]:

1) Formation of inter-tier communication channels,
2) IC wafer thinning,
3) Wafer alignment and bonding.

Among these technologies, the formation of inter-tier communication channels is the most crucial in terms of dictating the performance and operation of the system. The 3D integration processes are focussed on methods to form efficient and dense through silicon vias (TSVs) to provide a good inter-tier communication channel [3]. However, the TSVs suffer from a considerable utilization of the wiring footprint of the individual tiers of the 3D IC leaving less area for intra-tier routing [3]. Moreover, the process of making TSVs for a multi-tier (more than 2 tiers) interconnection on a 3D IC is difficult for some TSV technologies and entirely prohibited for certain others [3]. Further, if two (2) laterally separated communication end-points on two (2) separate tiers are to be connected, then intra-tier routing is necessary—thereby increasing the interconnect length.

This work proposes the use of on-chip antennas for inter-tier communication inside a 3D IC. The feasibility of on-chip antennas for intra-chip communication on planar ICs has been shown in [4, 5]. High-speed operation capabilities of deep sub-micron devices have enabled operation frequencies above 10 GHz. Since the physical dimension of an antenna is inversely proportional to its operating frequency, it is possible to have very small antennas fabricated on chip using standard CMOS foundry processes. Similar to the targeted wireless RF intra-chip interconnects, RF microstrip intra-chip interconnects have been proposed in [6]. Although neither of these interconnects are in use in mainstream ICs yet, the emerging complexities of IC implementation in multi-processor system on chip (MPSoC) and 3D ICs are inviting to the integration of these interconnect technologies. To this end, the use of a wireless communication to transmit test data and control signals to solve the core accessibility problem of high density SoCs is presented in [7]. Such design solutions can also be extended to 3D ICs without any major modifications.

In this paper, on-chip antennas for wireless inter-tier communication on a 3D IC are proposed and their performance is simulated in order to characterize the level of signal coupling between the inter-tier antennas. The simulation structure is modeled using a fully depleted silicon on insulator (FDSOI) 3D circuit integration technology [8]. Simulation models for the other technologies can be derived similarly.

The on-chip antennas are proposed to be used in conjunction with TSVs. TSVs are advantageous for shorter, vertically aligned communication points between immediately adjacent tiers on a 3D IC. Two significant advantages of the proposed wireless interconnects are:

1) Permitting a communication channel between non-adjacent IC tiers,
2) Providing the flexibility to place the communication channel ports (i.e. antennas) on separate tiers without a perfect vertical alignment.

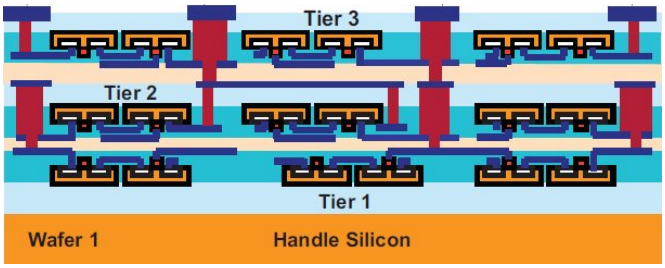

Fig. 1. MIT Lincoln Laboratory's 3D IC 3-tier integration structure [8].

TABLE I
MATERIAL CHARACTERISTICS OF DIFFERENT SILICON REGIONS ON A DIE.

Material	Conductivity (S/m)	Relative Permittivity
Silicon Dioxide	0.00	3.7
2000 Ω-cm Silicon Substrate	0.05	11.9
P-type Epitaxial Silicon	3636.36	11.9
N-type Epitaxial Silicon	1818.18	11.9

II. Wireless Interconnect Analysis

The on-chip antennas are simulated for inter-tier communication on a two tier and a three tier 3D IC. The on-chip antennas can potentially be used for any of the 3D IC wafer integration techniques. In this work, the 3D IC die is modeled according to MIT-Lincoln Laboratory's fully depleted silicon on insulator (FDSOI) 3D circuit integration technology design parameters [8]. The transmission gain is the highest for the high resistivity silicon substrate of the silicon on insulator (SoI) die [4, 5]. The cross-sectional view of the FDSOI 3D IC 3-tier integration structure is illustrated in Figure 1.

The simulations are performed in Ansoft HFSS (High Frequency Structure Simulator), a 3D finite element method (FEM) based full-wave electromagnetic simulator [9]. Meander dipole antennas are used in the simulation model as these antennas are more compatible with conventional CMOS technologies in having 90° bend angles. The antennas are designed to operate at 17 GHz with a total arm length (including the length of the meander segments) of 2.4 mm according to the parameters presented in [10]. The parameters presented in [10] do not include a high conductivity epitaxial layer under the antennas. However it is shown in [11], that the presence of a high conductivity epitaxial layer can reduce the radiation frequency. Hence, to accurately model the environment of operation for the on-chip antennas, the conductivity parameters for the different materials on the die are used. These parameters are listed in Table I. The conductivity values are calculated from the parameters provided in [8] and doped semiconductor material resistivity data provided in [12]. The dimensional parameters for the meander dipole antennas are provided in Table II. The die size is a generic 6×3.4 mm^2 as shown in Figure 2.

Different wireless interconnect network topologies are possible based on the placement of the proposed on-chip antennas.The simulations are performed for the following possible

TABLE II
DIMENSIONAL PARAMETERS OF THE MEANDER DIPOLE ANTENNA.

Design Parameter	Magnitude
Arm Length (excluding bend lengths)	1.2 mm
Arm Run Length (including bend lengths)	2.4 mm
Bend Element Width	10 μm
Bend Element Length	60 μm
Antenna Thickness	630 nm

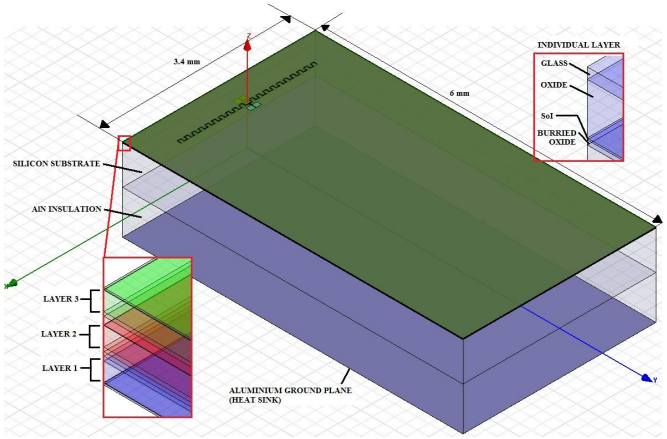

Fig. 2. Simulated 3D IC model for an inter-tier wireless interconnect system.

wireless interconnect network topologies of the communication end-points:

1) Vertically aligned—transmitting and receiving antennas vertically aligned on different IC tiers,
2) Non-vertically aligned—transmitting and receiving antennas laterally displaced on different IC tiers.
   a) Point-to-point communication,
   b) Multi-point communication.

The frequency range for all the simulation cases is from 5 GHz to 20 GHz, based on the frequency range achievable with the meander dipole antenna sites in Figure 2.

III. Results and Discussions

In experimentation, the scattering parameter (s-parameter) matrix $\overline{S}$ between the antenna pair is collected. The scattering parameter (s-parameter) matrix of a network characterizes the coupling between the ports of a network. An element S_{ij} of the s-parameter matrix $\overline{S}$ is the ratio of the normalized output power at port i due to the normalized input power at port j [13]. Hence, the s-parameter matrix is used to characterize the operation and efficiency of the inter-tier wireless communication system.

The simulation model is a two (2) port network, with the transmitting and receiving antennas designated as ports 1 and 2, respectively. The s-parameter S_{11}, also defined as the return loss, is used to determine the radiation frequency of the transmitting antenna. The s-parameter S_{21} characterizes the signal coupling between the radiating and the transmitting antennas. Hence, the s-parameter S_{21} is used to characterize the strength of the wireless link between the transmitting and receiving antennas.

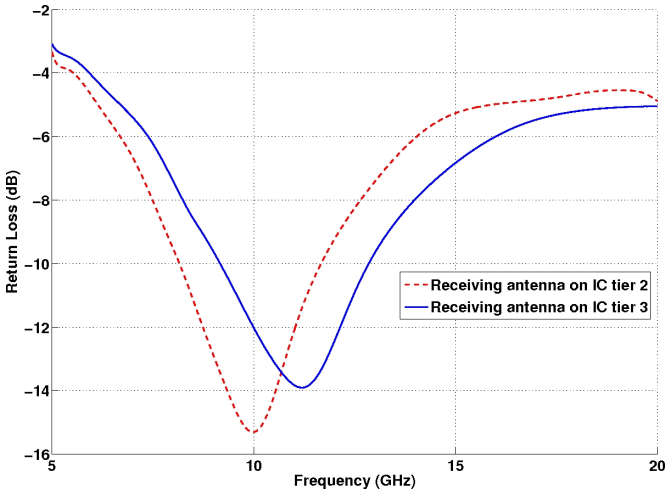

Fig. 3. Return loss S_{11} at the transmitting antenna.

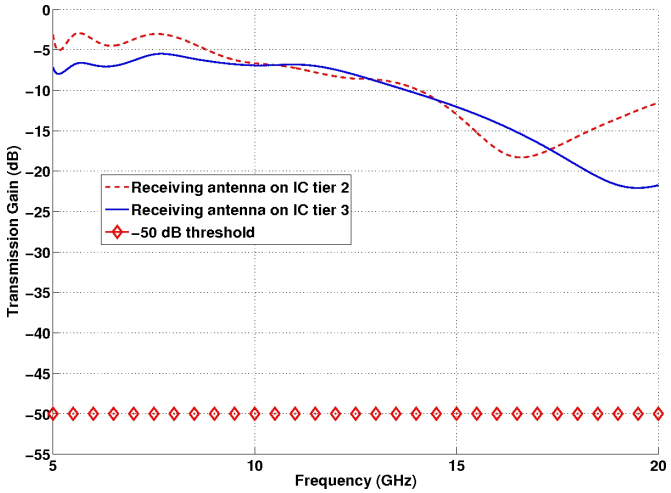

Fig. 4. Transmission gain G_a between transmitting and receiving antenna on different IC tiers (vertically aligned).

The radiation frequency of the antenna (based on the frequency at which the absolute value of the return loss is the highest) is expected to be at 17 GHz according to the parameters presented in [10]. However, as discussed in Section II, the presence of a thin high-conductivity epitaxial layer under the antenna structure shifts the radiation frequency. The higher the conductivity of the epitaxial layer, the larger is the reduction in the radiation frequency [11]. Hence, as shown in Figure 3, the radiation frequency of the transmitting antenna in this environment is 10 GHz (because the absolute value of the s-parameter S_{11} is the highest at this frequency). This shift in the radiation frequency of the transmitting antenna (compared to the estimate in [10]) is not critical for the wireless interconnect design. However, the frequency shift should be accounted for in designing on-chip antennas and should be done so before designing the required circuitry. Since the length of an antenna is inversely proportional to the frequency of operation, the dimensions of both the transmitting and the receiving antenna can be reduced to increase the operating frequency to the desired range, providing a more compact antenna design.

The figure of merit for the antenna pair is the transmission gain between the transmitting and receiving antenna. The transmission gain, G_a of the antenna pair is computed using the following formula:

$$G_a = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \quad (1)$$

where S_{21} is the forward transmission, S_{11} is the reflection of the electric field at the transmitting antenna and S_{22} is the reflection of the electric field at the receiving antenna. All three parameters S_{11}, S_{21}, and S_{22} are obtained from the s-parameter matrix $\overline{S}$.

A. Vertically Aligned Communication End-points

In the vertically aligned case, the transmitting antenna is placed on IC tier 1 and the receiving antenna is placed vertically above on IC tier 2 and on IC tier 3. The transmission gain G_a—based on the simulation results between the transmitting and receiving antennas with vertical alignment—is shown in Figure 4. The high value of the transmission gain indicates a good signal coupling. For an effective communication, it is required that the gain of the antenna be higher than the gain that can be provided using a low noise amplifier (LNA) at the receiving end. LNAs are capable of providing gains as high as 50 dB [14]. The transmission gain G_a for the receiving antenna placed on IC tier 2 and on IC tier 3 of the 3D IC is found to be -6.67 dB and -6.93 dB, respectively, at the radiating frequency of 10 GHz. Hence, a strong communication channel is established between the IC tiers of a 3D IC using on-chip antennas.

B. Non-vertically Aligned Communication End-points

In the non-vertically aligned point-to-point communication case, the transmitting antenna is placed on IC tier 2 and the receiving antenna is placed on IC tier 1 and on IC tier 3 with a varying level of lateral separation. In the non-vertically aligned multi-point communication case, the transmitting antenna is placed on IC tier 2 (at the center of the die) and the receiving antennas placed simultaneously on IC tier 1 and IC tier 3 (on the opposite edges of the die).

1) Point-to-point Communication: The computed transmission gain G_a for the non-vertically aligned point-to-point communication simulation case is shown in Figure 5. This experiment is performed to demonstrate the advantage of wireless interconnects on 3D ICs in providing the flexibility to place the communication channel end points on separate tiers without a perfect vertical alignment (unlike TSVs). The results shown in Figure 5 also indicate that, at the desired frequency, the transmission gain is higher than -50 dB (the threshold for successful communication based on achievable LNA gain). Therefore, it is possible to have a lateral separation as high as 3 mm (which is not feasible for TSVs even with additional inter-tier routing). Since the transmission gain is much higher than the threshold for successful communication (based on achievable LNA gain), it is possible to have 3D IC die sizes

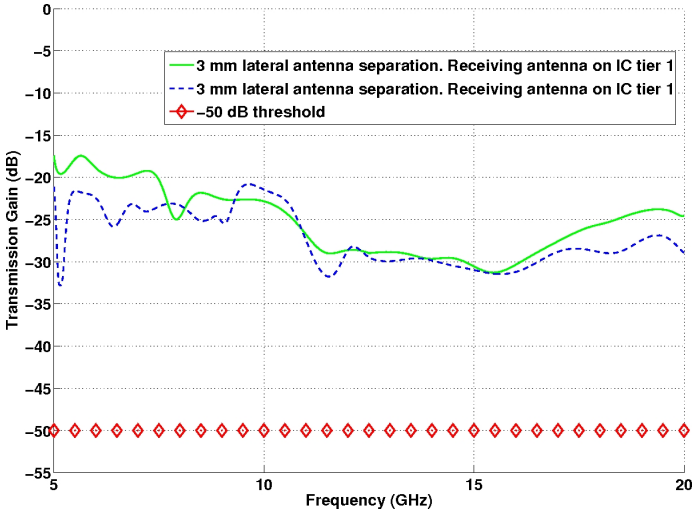

Fig. 5. Transmission gain G_a between transmitting and receiving antenna on different IC tiers with 3 mm lateral separation between the antennas.

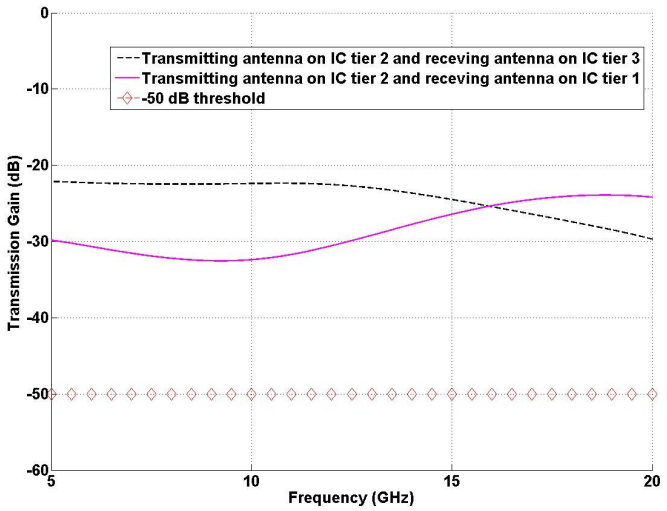

Fig. 6. Transmission gain G_a between transmitting and receiving antennas placed on two diagonally opposite corners of a 3D IC.

of higher than the 6×3.4 mm^2 die used in these experiments. However, an increase in the lateral separation between the antenna pair is expected to decrease the transmission gain, while the transmission gain would be higher for a smaller lateral separation.

2) Multi-point Communication: The transmission gains between the receiving and transmitting antennas for the non-vertically aligned multi-point communication simulation case are shown in Figure 6. The receiving antennas (on IC tier 1 and 3) are placed on diagonally opposite corners of the 3D IC each with a 2.5 mm lateral separation from the transmitting antenna (on IC tier 2). This experiment demonstrates the feasibility of distributing a signal to two diagonally opposite communication end-points on a 3D IC using wireless interconnects. A similar multi-end point communication using TSVs would necessitate long lengths of intra-tier metal interconnects on both sides of the signal source (location of the transmitting antenna). The parasitics of both the branches would be parallel to each other and therefore add up, which increases the delay to both the communication end-points.

IV. Conclusion

In this work, the feasibility of using on-chip antennas for wireless communication between the IC tiers of a 3D integrated circuit is shown. It is shown that for antennas placed vertically above each other—vertically aligned communication end-points—on different IC tiers of the die, it is possible to have strong signal coupling. It is also shown that it is possible to communicate wirelessly between two (2) IC tiers where the communication end-points are separated from each other laterally up to 3 mm. Since the antennas and the associated circuitry are expected to occupy a considerable amount of space, they are better suited to be used in conjunction with TSVs, especially for multi-tier [more than two (2) IC tiers] global communication.

This work shows the feasibility of on-chip antennas for inter-tier communication from a signal coupling point of view. A number of other items must be researched, such as power dissipation, temperature profiles and the quality of the communication channel compared to TSVs.

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