Vinayak Honkote

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RESEARCH INTERESTS

Cyber-physical systems (CPS), human computer interaction (HCI), computer vision, display technologies, electronic design automation (EDA) and VLSI physical design in general including clock network design, routing, design for manufacturing (DFM), low power VLSI circuits, near threshold supply voltage (NTV) circuits, high frequency circuit design, emerging technologies, 3-D ICs, interconnects and clocking for SoCs and multi-core systems.

EDUCATION

- **Ph.D., Electrical and Computer Engineering**, (2006 – 2010).
  Drexel University, Philadelphia, PA.
  Topic: Design Automation and Analysis of Resonant Clocking Technologies.
- **M.S., Electrical Engineering**, (2004 – 2006).
  Drexel University, Philadelphia, PA.
- **B.E., Electronics and Communications Engineering**, (1999 – 2003).
  Bangalore Institute of Technology, Visvesvaraya Technological University,
  Bangalore, India.

PROFESSIONAL EXPERIENCE

- **Research Scientist**, (03/2011 – current)
  Intel Corporation, Intel Labs-SoC Design Lab, Bangalore, Karnataka, India
  – Worked on enhanced display algorithms for tablets/PCs and smart-phones.
  – Worked on PLL integration for SoCs.
  – Worked on clocking methodologies for Intel based products.
  – Worked on floating point unit (FPU) validation engine for ubiquitous high performance computing (UHPC) systems.
- **Research Assistant and Teaching Assistant**, (08/2006 – 10/2010)
  Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA, USA
- **Freshman Design Fellow**, (09/2009 – 09/2010)
  Co-teaching (with a faculty instructor) engineering design laboratory sequence
  for 4 freshman sections, each consisting of 32 students.
  Drexel University, Philadelphia, PA, USA
- **Adjunct Primary Instructor**, (Summer 2009 and Summer 2008)
  Richard C. Goodwin College of Professional Studies, Drexel University, Philadelphia, PA, USA
- **Internship - Junior Project Manager**, (06/2005 – 12/2005)
  Siemens Medical Solutions, Malvern, PA, USA
  – Responsibilities included decision making, performance analysis, module testing.
  – Hands–on experience with project management tools.
- **Design Engineer**, (07/2003 – 08/2004)
  Larsen & Toubro Infotech Ltd., Bangalore, India
  – Worked on wireless CDMA systems.
  – Developed and tested the ATM base station server modules in C++ (15,000 lines of C++).
  – Research work on CDMA and ATM networks.

TEACHING EXPERIENCE

- **Freshman Design Fellow**, (09/2009 – 09/2010)
  Co-teaching (with a faculty instructor) the engineering design laboratory sequence,
  Drexel University, Philadelphia, PA
- **Adjunct Primary Instructor**, (Summer 2009)
  ECE C304 Design with Micro-controllers, undergraduate level,
  Richard C. Goodwin College of Professional Studies, Drexel University, Philadelphia, PA
- **Adjunct Primary Instructor**, (Summer 2008)
  ECE C394 Computer Structures, undergraduate level,
  Richard C. Goodwin College of Professional Studies, Drexel University, Philadelphia, PA
- **Teaching Assistant**, (03/2005 – 09/2010)
  ECE C302 Digital Systems Projects, undergraduate level,
  ECE C304 Design with Micro-controllers, undergraduate level,
  ECE 200 Fundamentals of Intelligent Systems, undergraduate level,
  ECE C301 Advanced Programming for Engineers, undergraduate level,
  ECE C356 Embedded Systems, undergraduate level,
  Department of Electrical and Computer Engineering,
  Drexel University, Philadelphia, PA

HONORS AND AWARDS

- Spontaneous Recognition Awards (SRA) for demonstrating values such as, *Results Orientation*, *Quality*, *Risk Taking*, Intel Corporation, 2011, 2012.
- Finalist in the Best Ph.D. Dissertation Competition at the IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July 5-7, 2010.
- Recipient of "Nihat Bilgutay Fellowship" in recognition of academic merit in the Department of Electrical and Computer Engineering, Drexel University, February 17, 2010.
- Awarded one of the nine (9) Freshman Design Fellowships (2009-10) by the College of Engineering, covering full tuition and stipend, including career development for academic/research positions.
- Participated in ACM/SIGDA CADathlon programming contest at ICCAD 2009, 2008.
- Recipient of "Richard A. Newton Graduate Scholarship" at ACM/IEEE Design Automation Conference (DAC) 2007, for the *Routing for Resonant Clocking Technology in Multi-GHz range* project.
- Awarded fellowships to attend *NANOARCH 2006*, Design Automation Summer School (DASS) held at DAC 2007, ACM/SIGDA University Booth at DAC 2008 and IEEE International Conference on VLSI Design (VLSID), 2010, 2011, 2012.
- Awarded the Dean Fellowship for graduate study at Drexel University (September 2004 onwards).
- Secured 14th rank in 10th grade out of 600,000 students, Karnataka, India in 1997.

PROFESSIONAL ACTIVITIES

- **Technical Program Committee Member**
  – IEEE International Conference on VLSI Design (VLSID), 2014
  – IEEE International Symposium on Electronic System Design (ISED), 2013
- **Reviewer**
  – IEEE International Solid-State Circuits Conference (ISSCC), 2012, 2013
  – IEEE International Conference on VLSI Design (VLSID), 2013
  – IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2012
  – IEEE International Symposium on Electronic System Design (ISED), 2012
  – International Symposium on Quality Electronic Design (ISQED), 2010
  – ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI), 2008
  – IEEE International Conference on Midwest Circuits and Systems (MWSCAS), 2008, 2009, 2010
- **External Reviewer**
  – IEEE/ACM Design Automation Conference (DAC), 2013

PUBLICATIONS

Refereed Journal Publications and Submissions

6 Vinayak Honkote, Renuka Devi Nagarajan and Anuradha Srinivasan, *Process Variation Sensitivities of Rotary Traveling Wave and Mobius Standing Wave Oscillators*, (in review).

5 Jianchao Lu, Vinayak Honkote, Xin Chen and Baris Taskin, *Steiner Tree Based Rotary Clock Routing with Bounded Skew and Capacitive Load Balancing*, (in review).

4 Vinayak Honkote, Ankit More and Baris Taskin, *Interconnect Modeling and Power Analysis on Custom Rotary Oscillatory Array*, (in review).

3 Vinayak Honkote and Baris Taskin, *Timing Analysis and Optimization on Mobius Implementation of Resonant Standing Wave Oscillator*, (in review).

2 Vinayak Honkote and Baris Taskin, *ZeROA: Zero Clock Skew Synchronization and Load balancing with Rotary Oscillatory Array*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 20, No. 8, pp. 1528–1532, August 2012.

1 Vinayak Honkote and Baris Taskin, *CROA: Design and Analysis of the Custom Rotary Oscillatory Array*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 10, pp. 1837–1847, October 2012.

Refereed Conference Publications and Submissions

16 Vinayak Honkote, Renuka Devi Nagarajan, Anuradha Srinivasan, *Process Variation Sensitivities of Rotary Traveling Wave and Mobius Standing Wave Oscillators*, (submitted).

15 Matthew Guthaus, Baris Taskin and Vinayak Honkote, *High-Performance, Low-Power Resonant Clocking*, presented in the embedded tutorial at the IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 2012.

14 Vinayak Honkote, Ankit More and Baris Taskin, *3-D Parasitic Modeling for Rotary Interconnects* in IEEE International Conference on VLSI Design (VLSID), January 2012, pp. 137–142.

13 Jianchao Lu, Vinayak Honkote, Xin Chen and Baris Taskin, *Steiner Tree Based Rotary Clock Routing with Bounded Skew and Capacitive Load Balancing* in *Design, Automation and Test in Europe (DATE)*, March 2011, pp. 455–460.

12 Vinayak Honkote, Ankit More, Ying Teng, Jianchao Lu and Baris Taskin, *Interconnect Modeling, Synchronization and Power Analysis for Custom Rotary Rings*, in IEEE International Conference on VLSI Design (VLSID), January 2011.

11 Vinayak Honkote and Baris Taskin, *Skew-Aware Capacitive Load Balancing for Low-Power Zero Clock Skew Rotary Oscillatory Array*, in *IEEE International Conference on Computer Design (ICCD)*, October 2010.

10 Vinayak Honkote and Baris Taskin, *PEEC Based Parasitic Modeling for Power Analysis on Custom Rotary Rings*, Proceedings of the IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 2010, pp. 111–116.

9 Vinayak Honkote and Baris Taskin, *Design Automation and Analysis of Resonant Rotary Clocking Technology*, Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July 2010, pp. 471–472.

8 Vinayak Honkote and Baris Taskin, *Skew Analysis and Bounded Skew Constraint Methodology for Rotary Clocking Technology*, Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED), March 2010, pp. 413–417.

7 Vinayak Honkote and Baris Taskin, *Analysis, Design and Simulation of Capacitive Load Balanced Rotary Oscillatory Array*, Proceedings of the IEEE International Conference on VLSI Design (VLSID), January 2010, pp. 218–223.

6 Vinayak Honkote and Baris Taskin, *Skew Analysis and Design Methodologies for Improved Performance of Resonant Clocking*, Proceedings of the IEEE International SoC Design Conference (ISOCC), November 2009, pp. 165–168 (invited to special session).

5 Vinayak Honkote and Baris Taskin, *Capacitive Load Balancing for Mobius Implementation of Standing Wave Oscillator*, Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS), August 2009, pp. 232–235.

4 Vinayak Honkote and Baris Taskin, *Design Automation Scheme for Wirelength Analysis of Resonant Clocking Technologies*, Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS), August 2009, pp. 1147–1150.

3 Vinayak Honkote and Baris Taskin, *Zero Clock Skew Synchronization with Rotary Clocking Technology*, Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED), March 2009, pp. 588–593.

2 Vinayak Honkote and Baris Taskin, *Custom Rotary Clock Router*, Proceedings of the IEEE International Conference on Computer Design (ICCD), October 2008, pp. 114–119.

1 Vinayak Honkote and Baris Taskin, *Maze Router Based Scheme for Rotary Clock Router*, Proceedings of the IEEE International Conference on Midwest Circuits and Systems (MWSCAS), August 2008, pp. 442–445.

PATENTS

Patents

1 Vinayak Honkote, Anuradha Srinivasan, Nimmagadda Mallikarjuna Rao and Ravi Theja Nalamary, *Smart Display: Enabling and Enhancing Display Capabilities on Any Surface*, January 2013.

SELECTED PROJECTS

◇ **Enhanced Display Algorithms for Tablets/PCs and Smartphones**
– Worked on gesture recognition algorithms for enhancing display quality
– Implemented the real time video processing algorithms on Xilinx 7 FPGA
– Worked on alternative display concepts

◇ **PLL Integration in Intel SoC**
– Integrated SBPLL into 22 nm Intel SoC test-chip
– Designed the PLL wrapper for RTL simulations
– Worked on clock divider design and sync signal generation

◇ **Floating Point Unit (FPU) Validation Engine for Ubiquitous High Performance Computing (UHPC) Systems**
– Delivered a C++ based framework for FPU validation
– Provisions to set the required rounding modes and to capture the exception flags
– Implemented a random test pattern generation scheme based on Mersenne Twister pseudo-random number generator

◇ **Variation Sensitivities of Resonant Clocking Technologies**
– Variation analysis for rotary clocking and standing wave based clocking
– Variation effects due to parasitics and transmission line parameters
– Monte-Carlo simulations for variation analysis

◇ **A Basic Validation Framework for Verification Environment**
– Worked as a part of a team on the verification environment that is scalable and is capable of generating random stimulus through classes
– Responsible for the creation of generic data classes and randomization of the inputs
– Responsible for the template creation for testcase.sv which can be used for FUB/interface testing

◇ **Custom Rotary Clock Router**
– Clock routing and physical design for non-regular rotary rings
– 10,000 lines of C++, routing, timing algorithms
– Simulation of rotary rings in hspice

◇ **Skew and Wirelength Analysis for Resonant Clocking Technologies**
– Zero clock skew synchronization with rotary clocking
– 20,000 lines of C++, wire routing, placement algorithms
– Skew and wirelength analysis for rotary clocking and standing wave technologies

◇ **Optimization Algorithms for Resonant Clocking Technologies**
– Capacitance balancing algorithms for rotary clocking and standing wave technologies
– Linear programming, integer programming, heuristic, statistics, large-scale optimization
– Simulation of capacitance load balanced rotary rings in hspice

◇ **Selected Projects During Graduate Studies**
– Statistical Timing Analysis Tool [Course Project - CAD for VLSI design]
– Implementation of Advanced Filters on FPGA [Course Project - Advanced VLSI Design]
– VHDL Implementation of an 8-Bit Microprocessor [Course Project - VHDL]
– TMS320C6000 MP Based Image Processing System [Course Project - Advanced Micro-controllers]

SKILLS
◇ C, C++, Perl, Unix Shell Scripting, Basic Java

◇ Cadence – Virtuoso Suite, Spectre
Mentor – HDL Designer, Modelsim, Leonardo Spectrum
Synopsys – Design Compiler, HSPICE
Xilinx – Spartan 3, Virtex 5

◇ VHDL, SystemC, Matlab, Maple, Labview

◇ Cplex, Glpk, Lp Solve

◇ LaTeX, XEmacs, vi, Office Suites

◇ Unix, Linux, Mac OS, MS Windows, DOS

RELEVANT COURSEWORK
◇ CMOS VLSI design, computer architecture, embedded microprocessors, VHDL, CAD for VLSI design I and II, deep submicron systems, algorithms and data structures, stochastic systems, digital signal processing (DSP).